Originally IBM used Emitter Coupled Logic (ECL) in their CPUs (Yikes!!!)

These chips ran hot and were error prone

The S/390 (G5) was their first CMOS machine

- It’s capable of detecting and protecting from soft errors in logic
- It does this through “extensive error checking in all functional elements”
The 9X2 CPU Series

- Used ECL, a current steering technology
  - Really fast, REALLY power intensive
- They had leftover logic for error checking and functional redundancy
  - Approximately 30% overhead total
  - For example they used in-line parity, which calculated quickly due to ECL’s high fan-in and fan-out
Error Checking in the G5

- Design was done by hand and design checking was done by hand as well!
- In-line error checking could not be done, due to the cycle overhead
- They decided to do Dual Modular Redundancy for both the Instruction and Fetch Units (I-Unit) and the Execution Units (E-Unit) Separately on chip.
  - They physically enlarged the size of the chip citing 6x CMOS transistor yield
- The register file is protected by ECC
G5 Checkpointing Unit (R-Unit)

- Keeps track of the state of the entire CPU
  - Checks both the I-Unit and E-Unit and its duplicates
  - Successful execution places new state in the update buffer
  - Then stores are placed in the store buffer and the update buffer contents are placed in the checkpoint array
  - Checkpoint array + store buffer = precise state

- On errors, instructions are retried
  - The CPU is reset (except for R-Unit state), store buffer contents are sent to the L2
  - The CPU state is then set to the last successful instruction completion
  - If the error is transient, execution continues otherwise the processor stops and a spare is used automatically
Memory Hierarchy Fault Tolerance

- Write-through L1, ECC protected L2 (shared by 6 processors) and store buffer
  - If a line has a permanent fault, it is deleted and restored w/ a spare line after a power-cycle

- Main Memory uses SEC-DED (single error correct, double error detect)
  - Background scrubbing active checks for errors and corrects them
  - Too many errors and the chip is marked as bad and the data migrated
I/O Fault Tolerance

- Redundant pathing
- First system to use fibre channel
  - Less overhead required
  - The I/O channel adapter and bridge hardware are combined into the Integrated Cluster Bus (ICB)
- Redundant power supplies and UPS systems integrated

Diagram:

- Hardware dynamic pathing
- No single point of failure
- In-line error checking
- Hierarchical recovery:
  1. Interface (1 operation)
  2. Channel (>1 operation)
  3. MBA level

Interfaces:
- S/390 parallel
- ESCON
- FICON
- ISCS
- Network:
  - FDDI
  - Ethernet
  - Token ring
  - ATM

Connections:
- LAN/WAN
Discussion Questions

Is there a more efficient way of detecting errors then DMR?

Why not use TMR and have voting instead of having a R-unit and doing rollback?

They mentioned the G3 and G4 had more robust ECC in their memory, why go to a less robust version in G5?

Overall MTTF is 45 years, isn’t this overkill considering the trends in computing power?