Daniel J. Sorin

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Durham, NC 27708

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Research Interests

Multiprocessor computer architectures, with an emphasis on memory system design

Fault tolerant computer architectures

Verification-aware microprocessor design

Architectures for emerging nanotechnologies

Evaluation of system performance and dependability

Education

University of Wisconsin—Madison, Madison, WI

Doctorate of Philosophy in Electrical and Computer Engineering, August 2002

Advisor: David A. Wood

University of Wisconsin—Madison, Madison, WI

Master of Science in Electrical and Computer Engineering, May 1998

Duke University, Durham, NC

Bachelor of Science in Electrical and Computer Engineering, May 1996

Honors and Awards

Paper chosen as one of IEEE Micro's Top Picks from Computer Architecture Conferences, 2007

NSF Faculty Early Career Award, 2005

Technology Research News' Top of 2004 list for research performed by nanocomputing research group

Warren Faculty Scholarship, Pratt School of Engineering, Duke University

Outstanding Graduate Research Award, University of Wisconsin Department of Computer Sciences

Intel Foundation Graduate Fellowship

Phi Beta Kappa, Tau Beta Pi, and Eta Kappa Nu academic honor societies

Experience

Associate Professor, Duke University, Department of Electrical and Computer Engineering and Department of Computer Science

July 2009-present

Assistant Professor, Duke University, Department of Electrical and Computer Engineering and Department of Computer Science

September 2002-June 2009

Research Assistant, University of Wisconsin—Madison, Computer Sciences Department

August 1996-August 2002

Teaching Assistant, University of Wisconsin—Madison, Dept. of Electrical and Computer Engr.

August 1996-May 1997

Books

1. Daniel J. Sorin. "Fault Tolerant Computer Architecture." *Synthesis Lectures on Computer Architecture*, Morgan & Claypool Publishers, 2009.

Journal Publications

1. Albert Meixner and Daniel J. Sorin. "Dynamic Verification of Memory Consistency in Cache-Coherent Multithreaded Computer Architectures." *IEEE Transactions on Dependable and Secure Computing (TDSC)*, volume 6, number 1, January-March 2009, pages 18-31.

2. Fred A. Bower, Daniel J. Sorin, and Landon P. Cox. "The Impact of Dynamically Heterogeneous Multicore Processors on Thread Scheduling." *IEEE Micro*, May/June 2008, pages 17-25.

3. Albert Meixner, Michael E. Bauer, and Daniel J. Sorin. "Argus: Low-Cost, Comprehensive Detection of Errors in Simple Cores." *IEEE Micro: Micro's Top Picks from Computer Architecture Conferences*, volume 28, number 1, January/February 2008, pages 52-59.

4. Fred A. Bower, Daniel J. Sorin, and Sule Ozev. "Online Diagnosis of Hard Faults in Microprocessors." *ACM Transactions on Architecture and Code Optimization (TACO)*, volume 4, number 2, June 2007, article 8.

5. Tong Li, Alvin R. Lebeck, and Daniel J. Sorin. "Spin Detection Hardware for Improved Management of Multithreaded Systems." *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, volume 17, number 6, June 2006, pages 508-521.

6. Jaidev P. Patwardhan, Chris Dwyer, Alvin R. Lebeck, and Daniel J. Sorin. "NANA: A Nano-Scale Active Network Architecture." *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, volume 2, number 1, January 2006, pages 1-30.

7. Fred A. Bower, Sule Ozev, and Daniel J. Sorin. "Autonomic Microprocessor Execution via Self-Repairing Arrays." *IEEE Transactions on Dependable and Secure Computing (TDSC)*, volume 2, number 4, October-December 2005, pages 297-310.

8. Chris Dwyer, Alvin R. Lebeck, and Daniel J. Sorin. "Self-Assembled Architecture and the Temporal Aspects of Computing." *IEEE Computer*, volume 38, number 1, January 2005, pages 56-64.

9. Chris Dwyer, Vijeta Johri, Jaidev P. Patwardhan, Alvin R. Lebeck, and Daniel J. Sorin. "Design Tools for Self-assembling Nanoscale Technology", *Institute of Physics Nanotechnology*, volume 15, number 9, September 2004, pages 1240-1245. (Paper chosen by *Technology Research News* as part of their Top of 2004 list)

10. Alaa R. Alameldeen, Milo M. K. Martin, Carl J. Mauer, Kevin E. Moore, Min Xu, Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Simulating a $2M Commercial Server on a $2K PC." *IEEE Computer*, volume 36, number 2, February 2003, pages 50-57.

11. Daniel J. Sorin, Jonathan L. Lemon, Derek L. Eager, and Mary K. Vernon. "Analytic Evaluation of Shared-Memory Architectures." *Transactions on Parallel and Distributed Systems (TPDS)*, volume 14, number 2, February 2003, pages 166-180.

12. Daniel J. Sorin, Manoj Plakal, Anne E. Condon, Mark D. Hill, Milo M. K. Martin, and David A. Wood. "Specifying and Verifying a Broadcast and a Multicast Snooping Cache Coherence Protocol." *Transactions on Parallel and Distributed Systems (TPDS)*, volume 13, number 6, June 2002, pages 556-578.

Refereed Conference Publications

1. Patrick J. Eibl, Daniel J. Sorin, and Andrew D. Cook. "Reduced Precision Checking for a Floating Point Adder." *24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, October 2009.

2. Meng Zhang, Anita Lungu, and Daniel J. Sorin. "Analyzing Formal Verification and Testing Efforts of Different Fault Tolerance Mechanisms." *24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, October 2009.

3. Anita Lungu, Pradip Bose, Alper Buyuktosunoglu and Daniel J. Sorin. "Dynamic Power Gating with Quality Guarantees." *International Symposium on Low Power Electronics and Design (ISLPED)*, August 2009.

4. Anita Lungu, Pradip Bose, Daniel Sorin, Steven German and Geert Janssen. "Multicore Power Management: Ensuring Robustness via Early-Stage Formal Verification." *Seventh ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, July 2009.

5. Bogdan F. Romanescu and Daniel J. Sorin. "Core Cannibalization Architecture: Improving Lifetime Chip Performance for Multicore Processors in the Presence of Hard Faults." *Seventeenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October 2008, pages 43-51.

6. Albert Meixner and Daniel J. Sorin. "Detouring: Translating Software to Circumvent Hard Faults in Simple Cores." *38th Annual International Conference on Dependable Systems and Networks (DSN)*, June 2008, pages 80-89.

7. Bogdan F. Romanescu, Michael E. Bauer, Daniel J. Sorin, and Sule Ozev. "Reducing the Impact of Intra-Core Process Variability with Criticality-Based Resource Allocation and Prefetching." *ACM International Conference on Computing Frontiers*, May 2008, pages 129-138.

8. Albert Meixner, Michael E. Bauer, and Daniel J. Sorin. "Argus: Low-Cost, Comprehensive Detection of Errors in Simple Cores." *40th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December, 2007, pages 210-222. [Selected by IEEE Micro as one of 10 "Top Picks" among all computer architecture conference publications in 2007]

9. Sule Ozev, Daniel J. Sorin, and Mahmut Yilmaz. "Low-Cost Run-time Diagnosis of Hard Delay Faults in the Functional Units of a Microprocessor." *IEEE International Conference on Computer Design (ICCD)*, October 2007, pages 317-324.

10. Mahmut Yilmaz, Albert Meixner, Sule Ozev, and Daniel J. Sorin. "Lazy Error Detection for Microprocessor Functional Units." *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, September 2007, pages 361-369.

11. Anita Lungu and Daniel J. Sorin. "Verification-Aware Microprocessor Design." *Sixteenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007, pages 83-93.

12. Albert Meixner and Daniel J. Sorin. "Error Detection Using Dynamic Dataflow Verification." *Sixteenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007, pages 104-115.

13. Bogdan F. Romanescu, Michael E. Bauer, Daniel J. Sorin, and Sule Ozev. "Reducing the Impact of Process Variability with Prefetching and Criticality-Based Resource Allocation." Poster and extended abstract in *Sixteenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007, page 424.

14. Albert Meixner and Daniel J. Sorin. "Unified Microprocessor Core Storage." *ACM Conference on Computing Frontiers*, May 2007, pages 23-34.

15. Albert Meixner and Daniel J. Sorin. "Error Detection via Online Checking of Cache Coherence with Token Coherence Signatures." *13th International Symposium on High Performance Computer Architecture (HPCA),* February, 2007, pages 145-156.

16. Mahmut Yilmaz, Derek R. Hower, Sule Ozev, and Daniel J. Sorin. "Self-Detecting and Self-Diagnosing 32-bit Microprocessor Multiplier." *International Test Conference (ITC)*, October 2006.

17. Nathan N. Sadler and Daniel J. Sorin. "Choosing an Error Protection Scheme for a Microprocessor's L1 Data Cache." *International Conference on Computer Design (ICCD)*, October 2006, pages 499-505.

18. Albert Meixner and Daniel J. Sorin. "Dynamic Verification of Memory Consistency in Cache-Coherent Multithreaded Computer Architectures." *International Conference on Dependable Systems and Networks (DSN)*, June 2006, pages 73-82.

19. Fred A. Bower, Derek R. Hower, Mahmut Yilmaz, Daniel J. Sorin, and Sule Ozev. "Applying Architectural Vulnerability Analysis to Hard Faults in the Microprocessor." Poster and 2-page paper at *ACM SIGMETRICS*, June 2006, pages 375-376.

20. Fred A. Bower, Daniel J. Sorin, and Sule Ozev. "A Mechanism for Online Diagnosis of Hard Faults in Microprocessors." *38th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, November 2005, pages 197-208.

21. Albert Meixner and Daniel J. Sorin. "Dynamic Verification of Sequential Consistency." *32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005, pages 482-493.

22. Tong Li, Carla S. Ellis, Alvin R. Lebeck, and Daniel J. Sorin. "Pulse: A Dynamic Deadlock Detection Mechanism Using Speculative Execution." *USENIX Annual Technical Conference*, April 2005, pages 31-44.

23. Jonathan R. Carter, Sule Ozev, and Daniel J. Sorin. "Circuit-Level Modeling for Concurrent Testing of Operational Defects due to Gate Oxide Breakdown." *Design, Automation, and Test in Europe (DATE)*, March 2005, pages 300-305.

24. Chris Dwyer, Moky Cheung, and Daniel J. Sorin. "Semi-empirical SPICE Models for Carbon Nanotube FET Logic." *Fourth IEEE Conference on Nanotechnology (IEEE-Nano)*, August 2004, pages 386-388.

25. Fred A. Bower, Paul G. Shealy, Sule Ozev, and Daniel J. Sorin. "Tolerating Hard Faults in Microprocessor Array Structures." *International Conference on Dependable Systems and Networks (DSN)*, June 2004, pages 51-60.

26. Jaidev P. Patwardhan, Chris Dwyer, Alvin R. Lebeck, and Daniel J. Sorin. "Circuit and System Architecture for DNA-Guided Self-Assembly of Nanoelectronics." Invited paper in *Foundations of Nanoscience: Self-Assembled Architectures and Devices (FNANO)*, April 2004, pages 344-358.

27. Daniel J. Sorin, Milo M. K. Martin, Mark D. Hill, and David A. Wood. "Using Speculation to Simplify Multiprocessor Design." *International Parallel and Distributed Processing Symposium (IPDPS)*, April 2004, pages 75-84.

28. Jaidev P. Patwardhan, Alvin R. Lebeck, and Daniel J. Sorin. "Communication Breakdown: Analyzing CPU Usage in Commercial Web Workloads." *International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March 2004, pages 12-19.

29. Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Dynamic Verification of End-to-End Multiprocessor Invariants." *International Conference on Dependable Systems and Networks (DSN-3)*, June 2003, pages 281-290.

30. Milo M. K. Martin, Pacia J. Harper, Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Using Destination-Set Prediction to Improve the Latency/Bandwidth Tradeoff in Shared Memory Multiprocessors." *30th Annual International Symposium on Computer Architecture (ISCA)*, June 2003, pages 206-217.

31. Tong Li, Alvin R. Lebeck, and Daniel J. Sorin. "Quantifying Instruction Criticality for Shared Memory Multiprocessors." *15th Symposium on Parallelism in Algorithms and Architectures (SPAA)*, June 2003, pages 128-137.

32. Daniel J. Sorin, Milo M. K. Martin, Mark D. Hill, and David A. Wood. "SafetyNet: Improving the Availability of Shared Memory Multiprocessors with Global Checkpoint/Recovery." *29th Annual International Symposium on Computer Architecture (ISCA)*, May 2002, pages 123-134.

33. Milo M. K. Martin, Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Bandwidth Adaptive Snooping." *8th International Symposium on High Performance Computer Architecture (HPCA)*, February 2002, pages 251-262.

34. Milo M. K. Martin, Daniel J. Sorin, Harold W. Cain, Mark D. Hill, and Mikko H. Lipasti. "Correctly Implementing Value Prediction in Microprocessors that Support Multithreading or Multiprocessing." *34th International Symposium on Microarchitecture (MICRO)*, December 2001, pages 328-337.

35. Milo M. K. Martin, Daniel J. Sorin, Anastassia Ailamaki, Alaa R. Alameldeen, Ross M. Dickson, Carl J. Mauer, Kevin E. Moore, Manoj Plakal, Mark D. Hill, and David A. Wood. "Timestamp Snooping: An Approach for Extending SMPs." *9th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, November 2000, pages 25-36.

36. Derek L. Eager, Daniel J. Sorin, and Mary K. Vernon. "AMVA Techniques for High Service Time Variability." *ACM SIGMETRICS*, June 2000, pages 217-228.

37. Mark D. Hill, Anne E. Condon, Manoj Plakal, and Daniel J. Sorin. "A System-Level Specification Framework for I/O Architectures." *11th Annual Symposium on Parallel Algorithms and Architectures (SPAA)*, June 1999, pages 138-147.

38. E. Ender Bilir, Ross M. Dickson, Ying Hu, Manoj Plakal, Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Multicast Snooping: A New Coherence Method Using a Multicast Address Network." *26th Annual International Symposium on Computer Architecture (ISCA)*, May 1999, pages 294-304.

39. Anne E. Condon, Mark D. Hill, Manoj Plakal, and Daniel J. Sorin. "Using Lamport Clocks to Reason About Relaxed Memory Models." *5th International Symposium on High Performance Computer Architecture (HPCA)*, January 1999, pages 270-278.

40. Daniel J. Sorin, Vijay S. Pai, Sarita V. Adve, Mary K. Vernon, and David A. Wood. "Analytic Evaluation of Shared-Memory Systems with ILP Processors." *25th Annual International Symposium on Computer Architecture (ISCA)*, June 1998, pages 380-391.

41. Manoj Plakal, Daniel J. Sorin, Anne E. Condon, and Mark D. Hill. "Lamport Clocks: Verifying a Directory Cache-Coherence Protocol." *10th Annual Symposium on Parallel Algorithms and Architectures (SPAA)*, June 1998, pages 67-76.

Refereed and Invited Workshop Publications

1. Anita Lungu, Pradip Bose, Daniel J. Sorin, Steven German, and Geert Janssen. “Multicore Power Management: Ensuring Robustness via Early-Stage Formal Verification.” *3rd Workshop on Dependable Architectures (WDA-3)*, November 2008.

2. Albert Meixner and Daniel J. Sorin. “IOTA: Detecting Erroneous I/O Behavior via I/O Transaction Auditing.” *First Workshop on Compiler and Architectural Techniques for Application Reliability and Security (CATARS)*, June 2008.

3. Daniel J. Sorin and Sule Ozev. “Fault Tolerant Microprocessors for Space Missions.” *NASA Science Technology Conference*, June 2007. (invited paper)

4. Bogdan F. Romanescu, Sule Ozev, and Daniel J. Sorin. “Quantifying the Impact of Process Variability on Microprocessor Behavior.” *2nd Workshop on Architectural Reliability (WAR)*, December 2006.

5. Albert Meixner and Daniel J. Sorin. “Comprehensive Detection of Hardware Errors in Commodity Multithreaded Architectures.” 2-page paper and poster in *Workshop on Edge Computing Using New Commodity Architectures (EDGE)*, May 2006.

6. Jaidev Patwardhan, Chris Dwyer, Alvin R. Lebeck, and Daniel J. Sorin. “Evaluating the Connectivity of Self-Assembled Networks of Nano-Scale Processing Elements.” *IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH’05)*, May 2005, pages 2.17-2.24.

7. Alaa R. Alameldeen, Pacia J. Harper, Milo M. K. Martin, Carl J. Mauer, Daniel J. Sorin, Min Xu, Mark D. Hill, and David A. Wood. "Evaluating Non-deterministic Multi-threaded Commercial Workloads." *Fifth Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW-02)*, February 2002, pages 30-38.

Book Contributions

1. Exercise Editor for: David A. Patterson and John L. Hennessy. *Computer Organization and Design: The Hardware/Software Interface*, 3rd edition. Morgan-Kaufmann Publishers, 2004.

Patents

1. United State Patent 6,883,070. “Bandwidth-Adaptive, Hybrid, Cache-Coherence Protocol.” Inventors: Milo M. K. Martin, Daniel J. Sorin, Mark D. Hill, and David A. Wood. April 19, 2005.

2. United States Patent 7,415,644. “Self-Repairing of Microprocessor Array Structures.” Inventors: Fred A. Bower, Sule Ozev, Paul G. Shealy, and Daniel J. Sorin. August 19, 2008.

Other Publications

1. Bogdan F. Romanescu, Michael E. Bauer, Sule Ozev, and Daniel J. Sorin. “VariaSim: Simulating Circuits and Systems in the Presence of Process Variability.” *Computer Architecture News (CAN)*, volume 35, number 5, December 2007, pages 45-48.

2. Milo M.K. Martin, Daniel J. Sorin, Bradford M. Beckmann, Michael R. Marty, Min Xu, Alaa R. Alameldeen, Kevin E. Moore, Mark D. Hill, and David A. Wood. “Multifacet’s General Execution-driven Multiprocessor Simulator (GEMS) Toolset.” *Computer Architecture News (CAN)*, volume 33, number 4, November 2005.

Software Distributions

1. Multifacet GEMS Simulation infrastructure. `http://www.cs.wisc.edu/gems/`

2. Pulse: dynamic deadlock detection. `http://www.ee.duke.edu/~sorin/tasmania/`

3. VariaSim statistical static timing analysis. `http://www.ee.duke.edu/variasim/`

Conference Talks

1. "Multicore Power Management: Ensuring Robustness via Early-Stage Formal Verification." *Seventh ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, Cambridge, Massachusetts, July 2009.

2. "Fault Tolerant Microprocessors for Space Missions." *NASA Science Technology Conference (NSTC-07)*, Adelphi, Maryland, June 2007.

3. "Choosing an Error Protection Scheme for a Microprocessor's L1 Data Cache." *International Conference on Computer Design (ICCD)*, San Jose, California, October 2006.

4. "Using Speculation to Simplify Multiprocessor Design." *International Parallel and Distributed Processing Symposium (IPDPS)*, Santa Fe, New Mexico, April 2004.

5. "Dynamic Verification of End-to-End Multiprocessor Invariants." *International Conference on Dependable Systems and Networks (DSN-3)*, San Francisco, California, June 2003.

6. "SafetyNet: Improving the Availability of Shared Memory Multiprocessors with Global Checkpoint/Recovery." *29th International Symposium on Computer Architecture (ISCA)*, Anchorage, Alaska, June 2002.

7. "Correctly Implementing Value Prediction in Microprocessors that Support Multithreading or Multiprocessing." *34th International Symposium on Microarchitecture (MICRO-34)*, Austin, Texas, December 2001.

8. "AMVA Techniques for High Service Time Variability." *ACM SIGMETRICS 2000*, Santa Clara, California, June 2000.

9. "A System-Level Specification Framework for I/O Architectures." *11th Annual Symposium on Parallel Algorithms and Architectures (SPAA)*, Saint-Malo, France, June 1999. (Also presented at the Wisconsin Architecture Affiliates Meeting, October 1999)

10. "Using Lamport Clocks to Reason About Relaxed Memory Models." *5th International Symposium on High Performance Computer Architecture (HPCA)*, Orlando, Florida, January 1999.

11. "Analytic Evaluation of Shared-Memory Systems with ILP Processors." *25th Annual International Symposium on Computer Architecture (ISCA)*, Barcelona, Spain, June 1998. (Also presented at the Wisconsin Architecture Affiliates Meeting, October 1998)

Invited Talks

"Detecting Faults and Hardware Bugs Using Dynamic Verification"

- Dagstuhl seminar on Fault Tolerant Distributed Algorithms for VLSI Chips (Dagstuhl, Germany), September 2008

"Post-Silicon Validation Using Dynamic Verification"

- GSRC Workshop on Post-Silicon Validation (Anaheim, CA), June 2008

"Low-cost, Comprehensive Error Detection for Commodity Processors"

- Stanford University (Palo Alto, CA), May 2008; University of California—Berkeley, May 2008; University of Illinois (Champaign-Urbana, IL), April 2008; University of Michigan (Ann Arbor, MI), April 2008

"Why Do We Still Have Bugs?" (panel discussion)

• IBM T.J. Watson Research Center (Yorktown Heights, NY), April 2008

"The Design of Dependable and Variability-Tolerant Multithreaded Architectures"

• IBM T.J. Watson Research Center (Yorktown Heights, NY), September 2006

"Comprehensive Detection of Errors in Multithreaded Architectures"

• Intel Corporation (Hudson, MA), April 2007; University of Texas at Austin, March 2007; Advanced Micro Devices (Austin, TX), March 2007; Carnegie Mellon University (Pittsburgh, PA), February 2007; University of Pennsylvania (Philadelphia, PA), June 2006

"Comprehensive Error Detection for Multithreaded Memory Systems"

• NC State University: Computer Engineering Seminar, November 2005

"Duke FaultFinder Project"

• IBM University Day (Research Triangle Park, NC), October 2005

"Sherlock: Dynamic Verification of Multithreaded Memory Systems"

• Intel Labs (Portland, OR), September 2003; University of British Columbia (Vancouver, Canada), June 2003

"SafetyNet: Improving the Availability and Designability of Shared Memory Multiprocessors"

• University of California—Berkeley, April 2002; University of California—San Diego, April 2002; Stanford University (Palo Alto, CA), March 2002; University of Pennsylvania (Philadelphia, PA), March 2002; North Carolina State University (Raleigh, NC), February 2002; Duke University (Durham, NC), February 2002; Case Western Reserve University (Cleveland, OH), February 2002; Northwestern University (Evanston, IL), February 2002

"SafetyNet: Improving the Availability of Shared Memory Multiprocessors with Global Checkpoint/Recovery"

• Intel Labs (Portland, OR), January 2002

Tutorials

"GEMS: Multifacet's Accurate and Flexible Full System Simulator", at the *32nd International Symposium on Computer Architecture (ISCA)*, June 2005. Organized by Mike Marty, Bradford Beckmann, Luke Yen, Alaa R. Alameldeen, Min Xu, Kevin E. Moore, Daniel J. Sorin, and Milo M.K. Martin

Teaching

ECE 152: Computer Architecture: Spring 2005, Spring 2008, Spring 2009

• major updating of course in Spring 2005

ECE 192: Undergraduate Research: Spring 2005, Spring 2007, Spring 2009

• Derek Hower (Spring 2005), Michael Bauer (Spring 2007), Zachary Drillings (Spring 2009), Alex Edelsburg (Spring 2009), Andrew First (Spring 2009)

ECE 193: Undergraduate Research: Fall 2004, Fall 2005, Fall 2007

• Benjamin Burnham (Fall 2004), Derek Hower (Fall 2005), Michael Bauer (Fall 2007)

ECE 194: Undergraduate Research: Spring 2006, Spring 2008

• Derek Hower (Spring 2006), Michael Bauer (Spring 2008)

ECE 198: Undergraduate Research: Spring 2009

• George Rossin (Spring 2009), Preeyanka Shah (Spring 2009)

ECE 252 / CPS 220: Advanced Computer Architecture I: Fall 2003, Fall 2005, Fall 2007, Fall 2009

- first cross-listed with Computer Science in Fall 2003

ECE 254 / CPS 225: Fault Tolerant and Testable Computing Systems: Fall 2004, Fall 2006, Fall 2008

- major updating of course in Fall 2004

ECE 259 / CPS 221: Advanced Computer Architecture II: Spring 2003, Spring 2004, Spring 2006

- developed and first offered in ECE in Spring 2003
- added to Digital Systems sequence in Spring 2006 (first class with undergraduates)

ECE 399: Independent Study: Spring 2009

- Patrick Eibl (Spring 2009)

Conference and Workshop Program Committee Service

International Symposium on Computer Architecture (ISCA): 2008, 2009

International Conference on Dependable Systems and Networks (DSN): 2008, 2009, 2010

International Symposium on Microarchitecture (MICRO): 2009

International Symposium on High-Performance Computer Architecture (HPCA): 2009, 2010

International Conference on Parallel Architectures and Compilation Techniques (PACT): 2009

ACM SIGMETRICS: 2005

International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS): 2010 (external review committee)

Symposium on Parallelism in Algorithms and Architectures (SPAA): 2004, 2007

International Conference on Computer Design (ICCD): 2006, 2007, 2008

IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS): 2007

ACM Computing Frontiers: 2008

International Conference on Parallel and Distributed Systems (ICPADS): 2004

International Conference on High Performance Computing (HiPC): 2007

IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH): 2007

Workshop on Compiler and Architectural Techniques for Application Reliability and Security (CATARS): 2009

Workshop on Quality-Aware Design (W-QUAD): 2008

IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH): 2005, 2006

Workshop on Introspective Architecture (WISA): 2006

Annual IEEE Workshop on Workload Characterization (WWC): 2003

Grant Proposal Panel Service

National Science Foundation—Computing Processes and Artifacts Program: 2 panels

National Science Foundation—Computer Systems Research Program: 2 panels

National Science Foundation—Expeditions in Computing

Service to Computer Architecture Community

Referee for the following journals: IEEE Transactions on Parallel and Distributed Systems (TPDS), IEEE Transactions on Dependable and Secure Computing (TDSC), IEEE Transactions on Computers (TC), IEEE Transactions on Circuits and Systems (TCAS), IEEE Micro, ACM Transactions on Architecture and Code Optimiziation (TACO), ACM Transactions on Computer Systems (TOCS), ACM Transactions on Emerging Technologies in Computing Systems (JETC), IEEE Transactions on Very Large Scale Integration Systems (TVLSI).

Referee for the following conferences: International Symposium on Computer Architecture (ISCA), International Symposium on Microarchitecture (MICRO), International Symposium on High-Performance Computer Architecture (HPCA), Symposium on Parallelism in Algorithms and Architectures (SPAA), ACM SIGMETRICS, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), Symposium on Operating Systems Principles (SOSP), International Parallel and Distributed Processing Symposium (IPDPS), International Conference on Supercomputing (ICS), International Symposium on Performance Analysis of Systems and Software (ISPASS), Usenix Annual Technical Conference, International Conference on Computer Design (ICCD), ACM MobiSys, International Conference on Parallel and Distributed Systems (ICPADS), Asia-Pacific Computer Systems Architecture Conference.

Referee for the following workshops: Workshop on Workload Characterization (WWC), IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH), Workshop on Introspective Architecture (WISA), Workshop on Hot Topics in Operating Systems (HotOS), North Atlantic Test Workshop (NATW).

Publications chair for: 2006 IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH '06)

Finance chair for: 2005 IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH '05)

Session chair for: 2004 Symposium on Parallelism in Algorithms and Architectures (SPAA), 2008 Workshop on Dependable and Secure Nanocomputing (WDSN), 2008 International Conference on Parallel Architectures and Compilation Techniques (PACT)

Service to Department and University

ECE task force on Educational Computing Infrastructure, 2004-5

Evaluator of Duke Fulbright Scholarship candidates, 2004

ECE faculty search committee 2003-4, 2005-6

Computer Engineering / Computer Science taskforce, 2003

ECE Computing Committee, 2002-2006, 2007-current (chair)

ECE Graduate Studies Committe, 2006-8

Pratt IT Advisory Committee (PITAC), 2007-current (chair August 2008-current)

Pratt IT Director Search Committee, 2008

Pratt liaison between faculty and IT, fall 2008 (during search for new Pratt IT Director)

CS faculty search committee 2008-9

PhD Graduates

1. Tong Li, Ph.D. 2005, "Self-Monitoring of Thread Interactions for Improved Resource Management in Multithreaded Systems" (co-advised with Alvin R. Lebeck, CS).

2. Albert Meixner, Ph.D. 2008, "Low-cost Methods for Error Detection in Multi-core Systems" (CS)

- Duke CS Department's Research Initiation Project award, 2005

3. Anita Lungu, Ph.D. 2009, "Verification-Aware Processor Design" (CS)
   - Duke CS Department's Outstanding Masters Thesis award, 2007

PhD Advisees

1. Fred A. Bower (began study in Fall 2003, CS)
2. Adam N. Jacobvitz (began study in Fall 2009)
3. Morakinyo K. Olugbade (began study in Fall 2009)
4. Bogdan F. Romanescu (began study in Fall 2005)
5. Meng Zhang (began study in Fall 2008)

Master's Graduates

1. Moky Cheung, M.S. 2004.

2. Jennifer S. Miller, M.S. 2005, "Analytical Evaluation of Performance Variability in Digital Circuits Due to Process Variability."
   - National Science Foundation Graduate Fellow

3. Nathan N. Sadler, M.S. 2006.

Postdoctoral Advisees

1. Chris Dwyer (first position: Assistant Professor, Department of ECE, Duke University)

Undergraduate Pratt Fellow Advisees

1. Michael Bauer, B.S.E. 2008
2. Derek Hower, B.S.E. 2006.
   - Won Duke ECE Department's Charles Seager Memorial Award for undergraduate research

PhD Committees

John Burchett (advisor Brady, PhD 2005), Xiaobo Fan (CS-advisor Lebeck, PhD 2004), Jangwoo Kim (Carnegie Mellon University, advisor Babak Falsafi, PhD 2008), Jaidev Patwardhan (CS-advisor Lebeck, PhD 2006), Constantin Pistol (CS-advisors Lebeck and Dwyer, PhD 2009), Heng Zeng (CS-advisors Lebeck and Ellis, PhD 2004), Ying Zhang (advisor Chakrabarty, PhD 2004)

Master's Committees

Jeannie Albrecht (CS-advisor Vahdat, MS 2003), Ferdinand Schober (CS-advisor Kedem, MS 2004), Sara Sprenkle (CS-advisor Chase, MS 2004), Mahmut Yilmaz (advisor Ozev, MS 2006)

Outreach Students Supervised

Celanese Bozeman, Shaw University, summer 2008

External Funding

1. Recipient of gift of $65,377 from Toyota InfoTechnology Center, March 2009.

1. Principal Investigator: "Correct and Scalable Address Translation for Multicore Processors." *Semiconductor Research Corporation (SRC), Contract 2009-HJ-1881*, $180,000. February 1, 2009 - March 31, 2012.

2. Principal Investigator: "CPA-CSA: Verification-Aware Microarchitecture." *National Science Foundation CCF-0811290*, $220,000. September 1, 2008 - August 31, 2011.

3. Recipient of gift of $90,803 from Toyota InfoTechnology Center, August 2008.

4. Doctoral advisor of IBM PhD Scholarship awardee Anita Lungu, $10,000, 2008-2009.

5. Recipient of gift of $87,573 from Toyota InfoTechnology Center, September 2007.

6. Principal Investigator: "CAREER: Improving Multiprocessor Availability with Dynamic Verification and Autonomic Execution." *National Science Foundation CCF-0444516*, $400,000. June 16, 2005 - May 31, 2010.

7. Principal Investigator with co-investigator Sule Ozev: "Autonomic Computing via Dynamic Self-Repair of Hardware Faults." *National Aeronautics and Space Administration (NASA) AISR program #NNG04GQ06G*, $394,198, January 1, 2005 - December 31, 2007.

8. Recipient of gift of 40 Intel computers from Intel Corporation (Portland, OR), November, 2004.

9. Co-investigator with large Duke-wide team: "Shared University Research (SUR)." *IBM*, $150,000, 2004.

10. Doctoral advisor of National Science Foundation Graduate Fellowship awardee Jennifer S. Miller. 2004-2007.

11. Co-investigator with PI Alvin R. Lebeck and co-PIs John H. Reif, Paul D. Franzon, and Thomas LaBean: "ITR: Nanoarchitecture: Balancing Regularity, Complexity, and Defect Tolerance using DNA for Nanoelectronic Integration." *National Science Foundation CCR-0326157*, $1,200,000, September 15, 2003 - September 14, 2006.

12. Co-investigator with PI Alvin R. Lebeck. "ITR: Architectural Support for Service Level Agreements." *National Science Foundation CCR-0312561*, $220,004, August 1, 2003 - July 31, 2006.

13. Principal Investigator. "FaultFinder: Improving the Availability of Multiprocessor Servers." *National Science Foundation CCR-0309164*, $114,422, July 15, 2003 - June 30, 2005.