Daniel J. Sorin

Professor of Electrical and Computer Engineering

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Research Interests

Multiprocessor computer architectures, with an emphasis on memory system design

Fault tolerant computer architectures

Verification-aware microprocessor design

Special-purpose computer architectures

Education

University of Wisconsin—Madison, Madison, WI

Doctorate of Philosophy in Electrical and Computer Engineering, August 2002

Advisor: David A. Wood

University of Wisconsin—Madison, Madison, WI

Master of Science in Electrical and Computer Engineering, May 1998

Duke University, Durham, NC

Bachelor of Science in Electrical and Computer Engineering, May 1996

Honors and Awards

Best Paper Nomination at 2019 International Conference on Dependable Systems and Networks

Honorable Mention by IEEE Micro's Top Picks from Computer Architecture Conferences, 2018

Distinguished Visiting Fellow of Royal Academy of Engineering (UK), 2017

Distinguished Visiting Fellow of Scottish Informatics & Computer Science Alliance (SICSA), 2017

Visiting Professorship awarded by Leverhulme Trust (UK), 2017-8

Co-chair of IEEE Micro's Top Picks from Computer Architecture Conferences in 2015

IEEE Micro's Top Picks from Computer Architecture Conferences, 2015

Best Paper Award at 2014 International Symposium on High-Performance Computer Architecture

Computing Community Consortium's Computing Research Highlight of the Week, February 11-18, 2011 [http://www.cra.org/ccc/rh-detouring.php]

2011 Lois and John L. Imhoff Distinguished Teaching Award

IEEE Micro's Top Picks from Computer Architecture Conferences, 2010

IEEE Micro's Top Picks from Computer Architecture Conferences, 2007

NSF Faculty Early Career Award, 2005

Technology Research News' Top of 2004 list for research performed by nanocomputing research group

Warren Faculty Scholarship, Pratt School of Engineering, Duke University

Outstanding Graduate Research Award, University of Wisconsin Department of Computer Sciences

Intel Foundation Graduate Fellowship

Phi Beta Kappa, Tau Beta Pi, and Eta Kappa Nu academic honor societies

Senior Member of the IEEE

Senior Member of the ACM

Work Experience

Professor, Duke University, Department of Electrical and Computer Engineering and Department of Computer Science

July 2015-present

Founder and Chief Architect, Realtime Robotics, Inc.

March 2016-present

Associate Professor, Duke University, Department of Electrical and Computer Engineering and Department of Computer Science

July 2009-June 2015

Assistant Professor, Duke University, Department of Electrical and Computer Engineering and Department of Computer Science

September 2002-June 2009

Research Assistant, University of Wisconsin—Madison, Computer Sciences Department

August 1996-August 2002

Teaching Assistant, University of Wisconsin—Madison, Dept. of Electrical and Computer Engr.

August 1996-May 1997

Books

1. Vijay Nagarajan, Daniel J. Sorin, Mark D. Hill, and David A. Wood. "A Primer on Memory Consistency and Cache Coherence, 2nd edition." *Synthesis Lectures on Computer Architecture*, Morgan & Claypool Publishers, 2020.

2. Daniel J. Sorin, Mark D. Hill, and David A. Wood. "A Primer on Memory Consistency and Cache Coherence." *Synthesis Lectures on Computer Architecture*, Morgan & Claypool Publishers, 2011.

3. Daniel J. Sorin. "Fault Tolerant Computer Architecture." *Synthesis Lectures on Computer Architecture*, Morgan & Claypool Publishers, 2009.

Journal Publications

1. Atefeh Mehrabi, Aninda Manocha, Benjamin C. Lee, and Daniel J. Sorin. "Bayesian Optimization for Efficient Accelerator Synthesis." *ACM Transactions on Architecture and Code Optimization (TACO)*, December 2020.
2. Georgios Mappouras, Alireza Vahid, Robert Calderbank, and Daniel J. Sorin. "Extending Flash Lifetime in Embedded Processors by Expanding Analog Choice." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, volume 37, number 11, November 2018.
3. Meng Zhang, Jesse D. Bingham, John Erickson, and Daniel J. Sorin. "PVCoherence: Designing Flat Coherence Protocols for Scalable Verification." *IEEE Micro: Micro's Top Picks from Computer Architecture Conferences*, May/June 2015.

4. Ralph Nathan and Daniel J. Sorin. "Argus-G: Comprehensive, Low-Cost Error Detection for GPGPU Cores." *Computer Architecture Letters,* January, 2014.
5. Milo M. K. Martin, Mark D. Hill, and Daniel J. Sorin. "Why On-Chip Cache Coherence Is Here to Stay." *Communications of the ACM*, volume 55, number 7, July 2012, pages 78-89.
6. Bogdan F. Romanescu, Alvin R. Lebeck, and Daniel J. Sorin. "Address Translation-Aware Memory Consistency." *IEEE Micro: Micro's Top Picks from Computer Architecture Conferences*, volume 31, number 1, January/February 2011, pages 109-118.
7. Meng Zhang, Alvin R. Lebeck, and Daniel J. Sorin. "Fractal Consistency: Architecting the Memory System to Facilitate Verification." *Computer Architecture Letters*, volume 9, number 2, July-December 2010, pages 61-64.
8. Albert Meixner and Daniel J. Sorin. "Dynamic Verification of Memory Consistency in Cache Coherent Multithreaded Computer Architectures." *IEEE Transactions on Dependable and Secure Computing (TDSC)*, volume 6, number 1, January-March 2009, pages 18-31.
9. Fred A. Bower, Daniel J. Sorin, and Landon P. Cox. "The Impact of Dynamically Heterogeneous Multicore Processors on Thread Scheduling." *IEEE Micro*, May/June 2008, pages 17-25.
10. Albert Meixner, Michael E. Bauer, and Daniel J. Sorin. "Argus: Low-Cost, Comprehensive Detection of Errors in Simple Cores." *IEEE Micro: Micro's Top Picks from Computer Architecture Conferences*, volume 28, number 1, January/February 2008, pages 52-59.
11. Fred A. Bower, Daniel J. Sorin, and Sule Ozev. "Online Diagnosis of Hard Faults in Microprocessors." *ACM Transactions on Architecture and Code Optimization (TACO)*, volume 4, number 2, June 2007, article 8.
12. Tong Li, Alvin R. Lebeck, and Daniel J. Sorin. "Spin Detection Hardware for Improved Management of Multithreaded Systems." *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, volume 17, number 6, June 2006, pages 508-521.
13. Jaidev P. Patwardhan, Chris Dwyer, Alvin R. Lebeck, and Daniel J. Sorin. "NANA: A Nano-Scale Active Network Architecture." *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, volume 2, number 1, January 2006, pages 1-30.
14. Fred A. Bower, Sule Ozev, and Daniel J. Sorin. "Autonomic Microprocessor Execution via Self Repairing Arrays." *IEEE Transactions on Dependable and Secure Computing (TDSC)*, volume 2, number 4, October-December 2005, pages 297-310.
15. Chris Dwyer, Alvin R. Lebeck, and Daniel J. Sorin. "Self-Assembled Architecture and the Temporal Aspects of Computing." *IEEE Computer*, volume 38, number 1, January 2005, pages 56-64.
16. Chris Dwyer, Vijeta Johri, Jaidev P. Patwardhan, Alvin R. Lebeck, and Daniel J. Sorin. "Design Tools for Self-assembling Nanoscale Technology", *Institute of Physics Nanotechnology*, volume 15, number 9, September 2004, pages 1240-1245. **[Paper chosen by *Technology Research News* as part of their Top of 2004 list]**
17. Alaa R. Alameldeen, Milo M. K. Martin, Carl J. Mauer, Kevin E. Moore, Min Xu, Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Simulating a $2M Commercial Server on a $2K PC." *IEEE Computer*, volume 36, number 2, February 2003, pages 50-57.
18. Daniel J. Sorin, Jonathan L. Lemon, Derek L. Eager, and Mary K. Vernon. "Analytic Evaluation of Shared-Memory Architectures." *Transactions on Parallel and Distributed Systems (TPDS)*, volume 14, number 2, February 2003, pages 166-180.

19. Daniel J. Sorin, Manoj Plakal, Anne E. Condon, Mark D. Hill, Milo M. K. Martin, and David A. Wood. "Specifying and Verifying a Broadcast and a Multicast Snooping Cache Coherence Protocol." *Transactions on Parallel and Distributed Systems (TPDS)*, volume 13, number 6, June 2002, pages 556-578.

Refereed Conference Publications

1. Atefeh Mehrabi, Donghyuk Lee, Niladrish Chatterjee, Daniel J. Sorin, Benjamin C. Lee, and Mike O'Connor. "Learning Sparse Matrix Row Permutations for Efficient SpMM on GPU Architectures." *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March 2021.

2. Sean Murray, George Konidaris, and Daniel J. Sorin. "Roadmap Subsampling for Changing Environments." *IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS)*, October 2020.

3. Nicolai Oswald, Vijay Nagarajan, and Daniel J. Sorin. "HieraGen: Automatically Generating Hierarchical Cache Coherence Protocols from Atomic Specifications." *47th International Symposium on Computer Architecture (ISCA)*, June 2020.

4. Samantha Archer, Georgios Mappouras, Daniel J. Sorin, and Robert Calderbank. "Foosball Coding: Correcting Shift Errors and Bit Flip Errors in 3D Racetrack Memory." *50th IEEE/IFIP International Conference on Dependable Systems and Networks (DSN 2020)*, June 2020.

5. Atefeh Mehrabi, Aninda Manocha, Benjamin C. Lee, and Daniel J. Sorin. "Prospector: Synthesizing Efficient Accelerators via Statistical Learning." *Design, Automation & Test in Europe (DATE)*, March 2020.

6. Sean Murray, Will Floyd-Jones, George Konidaris, and Daniel J. Sorin. "A Programmable Architecture for Robot Motion Planning Acceleration." *30th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2019)*, July 2019.

7. Georgios Mappouras, Alireza Vahid, Robert Calderbank, and Daniel J. Sorin. "GreenFlag: Protecting 3D-Racetrack Memory from Shift Errors." *49th IEEE/IFIP International Conference on Dependable Systems and Networks (DSN 2019)*, June 2019. **[Nominated for Best Paper Award]**

8. Nicolai Oswald, Vijay Nagarajan, and Daniel J. Sorin. "ProtoGen: Automatically Generating Directory Cache Coherence Protocols from Atomic Specifications." *45th International Symposium on Computer Architecture (ISCA)*, June 2018. **[Honorable Mention from *IEEE Micro's annual Top Picks in Computer Architecture*. There were 12 Top Picks and 11 Honorable Mentions.]**

9. Georgios Mappouras, Alireza Vahid, Robert Calderbank, Derek R. Hower, and Daniel J. Sorin. "Jenga: Efficient Fault Tolerance for Stacked DRAM." *35th IEEE International Conference on Computer Design (ICCD)*, November 2017.

10. Opeoluwa Matthews and Daniel J. Sorin. "Architecting Hierarchical Coherence Protocols for Push-Button Parametric Verification." *50th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, October 2017.

11. Sean Murray, Will Floyd-Jones, Ying Qi, Daniel Sorin, and George Konidaris. "The Microarchitecture of a Real-time Robot Motion Planning Accelerator." *49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, October 2016.

12. Sean Murray, Will Floyd-Jones, Ying Qi, Daniel Sorin, and George Konidaris. "Robot Motion Planning on a Chip." *Robotics: Science and Systems (RSS)*, June 2016.

13. Georgios Mappouras, Alireza Vahid, Robert Calderbank, and Daniel J. Sorin. "Methuselah Flash: Rewriting Codes for Extra-Long Storage Lifetime." *46th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN)*, June 2016.

14. Ali Eslami, Georgios Mappouras, Alireza Vahid, Alfredo Velasco, Robert Calderbank, and Daniel J. Sorin. "Writing without Disturb on Phase Change Memories by Integrating Coding and Layout Design." *The International Symposium on Memory Systems (MEMSYS)*, October 2015.

15. Adam N. Jacobvitz, Andrew D. Hilton, and Daniel J. Sorin. "Multi-Program Benchmark Definition." *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS),* March 2015.

16. Ralph Nathan, Bryan Anthonio, Shih-Lien Lu, Helia Naeimi, Daniel J. Sorin, and Xiaobai Sun. "Recycled Error Bits: Energy-Efficient Architectural Support for Floating Point Accuracy." *SC '14*, November 2014.

17. Ralph Nathan and Daniel J. Sorin. "Nostradamus: Low-Cost Hardware-Only Error Detection for Processor Cores." *Design, Automation & Test in Europe (DATE)*, March 2014.

18. Meng Zhang, Jesse D. Bingham, John Erickson, and Daniel J. Sorin. "PVCoherence: Designing Flat Coherence Protocols for Scalable Verification." *20th International Symposium on High Performance Computer Architecture (HPCA)*, February 2014. **[Best Paper Award] [Selected by IEEE Micro as one of 12 "Top Picks" among all computer architecture conference publications in 2014]**

19. Opeoluwa Matthews, Meng Zhang, and Daniel J. Sorin. "Scalably Verifiable Dynamic Power Management." *20th International Symposium on High Performance Computer Architecture (HPCA)*, February 2014.

20. Kushal Seetharam, Lance Co Ting Keh, Ralph Nathan, and Daniel J. Sorin. "Applying Reduced Precision Arithmetic to Detect Errors in Floating Point Multiplication." *19th IEEE Pacific Rim International Symposium on Dependable Computing (PRDC)*, December 2013.

21. Blake A. Hechtman and Daniel J. Sorin. "Exploring Memory Consistency for Massively-Threaded Throughput-Oriented Processors." *International Symposium on Computer Architecture (ISCA)*, June 2013, pages 201-212.

22. Blake A. Hechtman and Daniel J. Sorin. "Evaluating Cache Coherent Shared Virtual Memory for Heterogeneous Multicore Chips." Extended abstract and poster in the *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, April 2013, pages 118-119.

23. Adam N. Jacobvitz, A. Robert Calderbank, and Daniel J. Sorin. "Coset Coding to Improve the Lifetime of Memory." *International Symposium on High Performance Computer Architecture (HPCA)*, February, 2013, pages 222-233.

24. Adam N. Jacobvitz, A. Robert Calderbank, and Daniel J. Sorin. "Writing Cosets of a Convolutional Code to Increase the Lifetime of Flash Memory." Invited paper at the *50th Annual Allerton Conference on Communication, Control, and Computing*, October, 2012, pages 308-318.

25. Patrick J. Eibl, Albert Meixner, and Daniel J. Sorin. "An FPGA-Based Experimental Evaluation of Microprocessor Core Error Detection with Argus-2." Poster and 2-page paper at *ACM SIGMETRICS*, June 2011, pages 121-122.

26. Meng Zhang, Alvin R. Lebeck, and Daniel J. Sorin. "Fractal Coherence: Scalably Verifiable Cache Coherence." *43rd International Symposium on Microarchitecture (MICRO)*, December 2010, pages 471-482.

27. Bogdan F. Romanescu, Alvin R. Lebeck, Daniel J. Sorin. "Specifying and Dynamically Verifying Address Translation-Aware Memory Consistency." *15th International Conference on Architectural*

Support for Programming Languages and Operating Systems (ASPLOS), March 2010. **[Selected by IEEE Micro as one of 11 "Top Picks" among all computer architecture conference publications in 2010]**

28. Bogdan F. Romanescu, Alvin R. Lebeck, Daniel J. Sorin, and Anne Bracy. "UNified Instruction/Translation/Data (UNITD) Coherence: One Protocol to Rule Them All." *16th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, January 2010.

29. Patrick J. Eibl, Daniel J. Sorin, and Andrew D. Cook. "Reduced Precision Checking for a Floating Point Adder." *24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, October 2009, pages 145-152.

30. Meng Zhang, Anita Lungu, and Daniel J. Sorin. "Analyzing Formal Verification and Testing Efforts of Different Fault Tolerance Mechanisms." *24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, October 2009, pages 277-285.

31. Anita Lungu, Pradip Bose, Alper Buyuktosunoglu and Daniel J. Sorin. "Dynamic Power Gating with Quality Guarantees." *International Symposium on Low Power Electronics and Design (ISLPED)*, August 2009, pages 377-382.

32. Anita Lungu, Pradip Bose, Daniel Sorin, Steven German and Geert Janssen. "Multicore Power Management: Ensuring Robustness via Early-Stage Formal Verification." *Seventh ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, July 2009, pages 7887.

33. Bogdan F. Romanescu and Daniel J. Sorin. "Core Cannibalization Architecture: Improving Lifetime Chip Performance for Multicore Processors in the Presence of Hard Faults." *Seventeenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October 2008, pages 43-51.

34. Albert Meixner and Daniel J. Sorin. "Detouring: Translating Software to Circumvent Hard Faultsin Simple Cores." *38th Annual International Conference on Dependable Systems and Networks (DSN)*, June 2008, pages 80-89.

35. Bogdan F. Romanescu, Michael E. Bauer, Daniel J. Sorin, and Sule Ozev. "Reducing the Impact of Intra-Core Process Variability with Criticality-Based Resource Allocation and Prefetching." *ACM International Conference on Computing Frontiers*, May 2008, pages 129-138.

36. Albert Meixner, Michael E. Bauer, and Daniel J. Sorin. "Argus: Low-Cost, Comprehensive Detection of Errors in Simple Cores." *40th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December, 2007, pages 210-222. **[Selected by IEEE Micro as one of 10 "Top Picks" among all computer architecture conference publications in 2007]**

37. Sule Ozev, Daniel J. Sorin, and Mahmut Yilmaz. "Low-Cost Run-time Diagnosis of Hard Delay Faults in the Functional Units of a Microprocessor." *IEEE International Conference on Computer Design (ICCD)*, October 2007, pages 317-324.

38. Mahmut Yilmaz, Albert Meixner, Sule Ozev, and Daniel J. Sorin. "Lazy Error Detection for Microprocessor Functional Units." *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, September 2007, pages 361-369.

39. Anita Lungu and Daniel J. Sorin. "Verification-Aware Microprocessor Design." *Sixteenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007, pages 83-93.

40. Albert Meixner and Daniel J. Sorin. "Error Detection Using Dynamic Dataflow Verification." *Sixteenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007, pages 104-115.

41. Bogdan F. Romanescu, Michael E. Bauer, Daniel J. Sorin, and Sule Ozev. "Reducing the Impact of Process Variability with Prefetching and Criticality-Based Resource Allocation." Poster and extended abstract in *Sixteenth International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007, page 424.

42. Albert Meixner and Daniel J. Sorin. "Unified Microprocessor Core Storage." *ACM Conference on Computing Frontiers*, May 2007, pages 23-34.

43. Albert Meixner and Daniel J. Sorin. "Error Detection via Online Checking of Cache Coherencewith Token Coherence Signatures." *13th International Symposium on High Performance Computer Architecture (HPCA),* February, 2007, pages 145-156.

44. Mahmut Yilmaz, Derek R. Hower, Sule Ozev, and Daniel J. Sorin. "Self-Detecting and Self-Diagnosing 32-bit Microprocessor Multiplier." *International Test Conference (ITC)*, October 2006.

45. Nathan N. Sadler and Daniel J. Sorin. "Choosing an Error Protection Scheme for a Microprocessor's L1 Data Cache." *International Conference on Computer Design (ICCD)*, October 2006, pages 499-505.

46. Albert Meixner and Daniel J. Sorin. "Dynamic Verification of Memory Consistency in Cache Coherent Multithreaded Computer Architectures." *International Conference on Dependable Systems and Networks (DSN)*, June 2006, pages 73-82.

47. Fred A. Bower, Derek R. Hower, Mahmut Yilmaz, Daniel J. Sorin, and Sule Ozev. "Applying Architectural Vulnerability Analysis to Hard Faults in the Microprocessor." Poster and 2-page paper at *ACM SIGMETRICS*, June 2006, pages 375-376.

48. Fred A. Bower, Daniel J. Sorin, and Sule Ozev. "A Mechanism for Online Diagnosis of Hard Faultsin Microprocessors." *38th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, November 2005, pages 197-208.

49. Albert Meixner and Daniel J. Sorin. "Dynamic Verification of Sequential Consistency." *32nd Annual International Symposium on Computer Architecture (ISCA)*, June 2005, pages 482-493.

50. Tong Li, Carla S. Ellis, Alvin R. Lebeck, and Daniel J. Sorin. "Pulse: A Dynamic Deadlock Detection Mechanism Using Speculative Execution." *USENIX Annual Technical Conference*, April 2005, pages 31-44.

51. Jonathan R. Carter, Sule Ozev, and Daniel J. Sorin. "Circuit-Level Modeling for Concurrent Testing of Operational Defects due to Gate Oxide Breakdown." *Design, Automation, and Test in Europe (DATE)*, March 2005, pages 300-305.

52. Chris Dwyer, Moky Cheung, and Daniel J. Sorin. "Semi-empirical SPICE Models for Carbon Nanotube FET Logic." *Fourth IEEE Conference on Nanotechnology (IEEE-Nano)*, August 2004, pages 386-388.

53. Fred A. Bower, Paul G. Shealy, Sule Ozev, and Daniel J. Sorin. "Tolerating Hard Faults in Microprocessor Array Structures." *International Conference on Dependable Systems and Networks (DSN)*, June 2004, pages 51-60.

54. Jaidev P. Patwardhan, Chris Dwyer, Alvin R. Lebeck, and Daniel J. Sorin. "Circuit and SystemArchitecture for DNA-Guided Self-Assembly of Nanoelectronics." Invited paper in *Foundations of Nanoscience: Self-Assembled Architectures and Devices (FNANO)*, April 2004, pages 344-358.

55. Daniel J. Sorin, Milo M. K. Martin, Mark D. Hill, and David A. Wood. "Using Speculation to Simplify Multiprocessor Design." *International Parallel and Distributed Processing Symposium (IPDPS)*, April 2004, pages 75-84.

56. Jaidev P. Patwardhan, Alvin R. Lebeck, and Daniel J. Sorin. "Communication Breakdown: Analyzing CPU Usage in Commercial Web Workloads." *International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March 2004, pages 12-19.

57. Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Dynamic Verification of End-to-End Multiprocessor Invariants." *International Conference on Dependable Systems and Networks (DSN-3)*, June 2003, pages 281-290.

58. Milo M. K. Martin, Pacia J. Harper, Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Using Destination-Set Prediction to Improve the Latency/Bandwidth Tradeoff in Shared Memory Multiprocessors." *30th Annual International Symposium on Computer Architecture (ISCA)*, June 2003, pages 206-217.

59. Tong Li, Alvin R. Lebeck, and Daniel J. Sorin. "Quantifying Instruction Criticality for Shared Memory Multiprocessors." *15th Symposium on Parallelism in Algorithms and Architectures (SPAA)*, June 2003, pages 128-137.

60. Daniel J. Sorin, Milo M. K. Martin, Mark D. Hill, and David A. Wood. "SafetyNet: Improving the Availability of Shared Memory Multiprocessors with Global Checkpoint/Recovery." *29th Annual International Symposium on Computer Architecture (ISCA)*, May 2002, pages 123-134.

61. Milo M. K. Martin, Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Bandwidth Adaptive Snooping." *8th International Symposium on High Performance Computer Architecture (HPCA)*, February 2002, pages 251-262.

62. Milo M. K. Martin, Daniel J. Sorin, Harold W. Cain, Mark D. Hill, and Mikko H. Lipasti. "Correctly Implementing Value Prediction in Microprocessors that Support Multithreading or Multiprocessing." *34th International Symposium on Microarchitecture (MICRO)*, December 2001, pages 328-337.

63. Milo M. K. Martin, Daniel J. Sorin, Anastassia Ailamaki, Alaa R. Alameldeen, Ross M. Dickson,Carl J. Mauer, Kevin E. Moore, Manoj Plakal, Mark D. Hill, and David A. Wood. "Timestamp Snooping: An Approach for Extending SMPs." *9th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, November 2000, pages 25-36.

64. Derek L. Eager, Daniel J. Sorin, and Mary K. Vernon. "AMVA Techniques for High Service Time Variability." *ACM SIGMETRICS*, June 2000, pages 217-228.

65. Mark D. Hill, Anne E. Condon, Manoj Plakal, and Daniel J. Sorin. "A System-Level Specification Framework for I/O Architectures." *11th Annual Symposium on Parallel Algorithms and Architectures (SPAA)*, June 1999, pages 138-147.

66. E. Ender Bilir, Ross M. Dickson, Ying Hu, Manoj Plakal, Daniel J. Sorin, Mark D. Hill, and David A. Wood. "Multicast Snooping: A New Coherence Method Using a Multicast Address Network." *26th Annual International Symposium on Computer Architecture (ISCA)*, May 1999, pages 294-304.

67. Anne E. Condon, Mark D. Hill, Manoj Plakal, and Daniel J. Sorin. "Using Lamport Clocks to Reason About Relaxed Memory Models." *5th International Symposium on High Performance Computer Architecture (HPCA)*, January 1999, pages 270-278.

68. Daniel J. Sorin, Vijay S. Pai, Sarita V. Adve, Mary K. Vernon, and David A. Wood. "Analytic Evaluation of Shared-Memory Systems with ILP Processors." *25th Annual International Symposium on Computer Architecture (ISCA)*, June 1998, pages 380-391.

69. Manoj Plakal, Daniel J. Sorin, Anne E. Condon, and Mark D. Hill. “Lamport Clocks: Verifying a Directory Cache-Coherence Protocol.” *10th Annual Symposium on Parallel Algorithms and Architectures (SPAA)*, June 1998, pages 67-76.

Publications in Conference Special Sessions

1. Daniel J. Sorin, Opeoluwa Matthews, and Meng Zhang. "Architecting Dynamic Power Management to be Formally Verifiable." *Design Automation Conference (DAC)*, June 2014.

2. Dimitris Gizopoulos, Mihalis Psarakis, Sarita V. Adve, Pradeep Ramachandran, Siva Kumar Sastry Hari, Daniel Sorin, Albert Meixner, Arijit Biswas, and Xavier Vera. “Architectures for Online Error Detection and Recovery in Multicore Processors.” Paper presented as part of embedded tutorial in *Design, Automation & Test in Europe (DATE)*, March 2011.

Refereed and Invited Workshop Publications

1. Yaqi Zhang, Ralph Nathan, and Daniel J. Sorin. "Reduced Precision Checking to Detect Errors in Floating Point Arithmetic." *12th Workshop on Silicon Errors in Logic - System Effects (SELSE)*, March 2016.

2. John Ingalls, Adam Jacobvitz, Patrick Eibl, Michael Ansel and Daniel Sorin. “Experiences in Developing and Evaluating a Low-Cost Soft-Error-Tolerant Multicore Processor.” *10th Workshop on Silicon Errors in Logic - System Effects (SELSE)*, April 2014.

3. Adam N. Jacobvitz, Robert Calderbank, and Daniel J. Sorin. “Coset Coding to Extend the Lifetime of Non-Volatile Memory.” *Non-Volatile Memories Workshop (NVM-W)*, March 2014.

4. Blake A. Hechtman and Daniel J. Sorin. “The Limits of Concurrency in Cache Coherence.” *10th Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD)*, June 2012.

5. Ralph Nathan and Daniel J. Sorin. “Argus-G: A Low-Cost Error Detection Scheme for GPGPUs.” *Workshop on Resilient Architectures*, December 2010.

6. Anita Lungu, Pradip Bose, Daniel J. Sorin, Steven German, and Geert Janssen. “Multicore Power Management: Ensuring Robustness via Early-Stage Formal Verification.” *3rd Workshop on Dependable Architectures (WDA-3)*, November 2008.

7. Albert Meixner and Daniel J. Sorin. “IOTA: Detecting Erroneous I/O Behavior via I/O Transaction Auditing.” *First Workshop on Compiler and Architectural Techniques for Application Reliability and Security (CATARS)*, June 2008.

8. Daniel J. Sorin and Sule Ozev. “Fault Tolerant Microprocessors for Space Missions.” *NASA Science Technology Conference*, June 2007. (invited paper)

9. Bogdan F. Romanescu, Sule Ozev, and Daniel J. Sorin. “Quantifying the Impact of Process Variability on Microprocessor Behavior.” *2nd Workshop on Architectural Reliability (WAR)*, December 2006.

10. Albert Meixner and Daniel J. Sorin. “Comprehensive Detection of Hardware Errors in Commodity Multithreaded Architectures.” 2-page paper and poster in *Workshop on Edge Computing Using New Commodity Architectures (EDGE)*, May 2006.

11. Jaidev Patwardhan, Chris Dwyer, Alvin R. Lebeck, and Daniel J. Sorin. “Evaluating the Connectivity of Self-Assembled Networks of Nano-Scale Processing Elements.” *IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH’05)*, May 2005, pages 2.17-2.24.

12. Alaa R. Alameldeen, Pacia J. Harper, Milo M. K. Martin, Carl J. Mauer, Daniel J. Sorin, Min Xu, Mark D. Hill, and David A. Wood. "Evaluating Non-deterministic Multi-threaded Commercial

Workloads." *Fifth Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW02)*, February 2002, pages 30-38.

Book Contributions

Exercise Editor for: David A. Patterson and John L. Hennessy. *Computer Organization and Design: The Hardware/Software Interface*, 3rd edition. Morgan-Kaufmann Publishers, 2004.

Patents

1. United States Patent 6,883,070. "Bandwidth-Adaptive, Hybrid, Cache-Coherence Protocol." Inventors: Milo M. K. Martin, Daniel J. Sorin, Mark D. Hill, and David A. Wood. April 19, 2005.

2. United States Patent 7,415,644. "Self-Repairing of Microprocessor Array Structures." Inventors: Fred A. Bower, Sule Ozev, Paul G. Shealy, and Daniel J. Sorin. August 19, 2008.

3. United States Patent 9,335,996. "Recycling Error Bits in Floating-Point Units." Inventors: Helia Naeimi, Ralph Nathan, Daniel Sorin, and Shih-Lien Lu. May 10, 2016.

4. United States Patent 9,632,866. "Systems for and Methods of Extending Lifetime of Non-volatile Memory." Inventors: Robert Calderbank, Adam N. Jacobvitz, Daniel J. Sorin. April 25, 2017.

5. Japan Patent 2017-557268. "Specialized Robot Motion Planning Hardware and methods of making and using the same." Inventors: George D. Konidaris and Daniel J. Sorin.

Other Publications

1. Bogdan F. Romanescu, Michael E. Bauer, Sule Ozev, and Daniel J. Sorin. "VariaSim: Simulating Circuits and Systems in the Presence of Process Variability." *Computer Architecture News (CAN)*, volume 35, number 5, December 2007, pages 45-48.

2. Milo M.K. Martin, Daniel J. Sorin, Bradford M. Beckmann, Michael R. Marty, Min Xu, Alaa R. Alameldeen, Kevin E. Moore, Mark D. Hill, and David A. Wood. "Multifacet's General Execution-driven Multiprocessor Simulator (GEMS) Toolset." *Computer Architecture News (CAN)*, volume 33, number 4, November 2005.

Software Distributions

1. Multifacet GEMS Simulation infrastructure. `http://www.cs.wisc.edu/gems/`
2. Cynk runtime for CPU/GPU task-parallel programming: `https://bitbucket.org/blakehechtman/cynk/wiki/Home`
3. Pulse: dynamic deadlock detection. `http://www.ee.duke.edu/~sorin/tasmania/`
4. VariaSim statistical static timing analysis. `http://www.ee.duke.edu/variasim/`

Conference Talks

1. "PVCoherence: Designing Flat Coherence Protocols for Scalable Verification." *0th International Symposium on High Performance Computer Architecture (HPCA)*, Orlando, Florida, February 2014. **Best Paper Award**

2. "Architectures for Online Error Detection and Recovery in Multicore Processors." *Design, Automation & Test in Europe (DATE)*, Grenoble, France, March 2011.

3. "Multicore Power Management: Ensuring Robustness via Early-Stage Formal Verification." *Seventh ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, Cambridge, Massachusetts, July 2009.

4. "Fault Tolerant Microprocessors for Space Missions." *NASA Science Technology Conference (NSTC-07)*, Adelphi, Maryland, June 2007.
5. "Choosing an Error Protection Scheme for a Microprocessor's L1 Data Cache." *International Conference on Computer Design (ICCD)*, San Jose, California, October 2006.
6. "Using Speculation to Simplify Multiprocessor Design." *International Parallel and Distributed Processing Symposium (IPDPS)*, Santa Fe, New Mexico, April 2004.
7. "Dynamic Verification of End-to-End Multiprocessor Invariants." *International Conference on Dependable Systems and Networks (DSN-3)*, San Francisco, California, June 2003.
8. "SafetyNet: Improving the Availability of Shared Memory Multiprocessors with Global Checkpoint/Recovery." *29th International Symposium on Computer Architecture (ISCA)*, Anchorage, Alaska, June 2002.
9. "Correctly Implementing Value Prediction in Microprocessors that Support Multithreading or Multiprocessing." *34th International Symposium on Microarchitecture (MICRO-34)*, Austin, Texas, December 2001.
10. "AMVA Techniques for High Service Time Variability." *ACM SIGMETRICS 2000*, Santa Clara, California, June 2000.
11. "A System-Level Specification Framework for I/O Architectures." *11th Annual Symposium on Parallel Algorithms and Architectures (SPAA)*, Saint-Malo, France, June 1999. (Also presented at the Wisconsin Architecture Affiliates Meeting, October 1999)
12. "Using Lamport Clocks to Reason About Relaxed Memory Models." *5th International Symposium on High Performance Computer Architecture (HPCA)*, Orlando, Florida, January 1999.
13. "Analytic Evaluation of Shared-Memory Systems with ILP Processors." *25th Annual International Symposium on Computer Architecture (ISCA)*, Barcelona, Spain, June 1998. (Also presented at the Wisconsin Architecture Affiliates Meeting, October 1998)

Invited Talks

"Reliable Robotics in Academia and Industry"

- Plenary keynote talk at the 27th IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS) and 16th IEEE International Conference on Design & Technology of Integrated System in Nanoscale Era (DTIS), June 2021.

"Specialized Processors to Accelerate Robot Motion Planning"

- University of Rochester, November 2020

"Robot Motion Planning: From the Lab to the Factory Floor"

- Triangle Area Pratt Faculty-Alumni Event, November 2020

"Real-time Motion Planning for the Masses"

- Workshop on Accelerating AI for Embedded Autonomy @ ESWEEK 2020, September 2020

"Designing Processors to Accelerate Robot Motion Planning"

- University of Edinburgh (UK), October 2016
- University of Glasgow (UK), September 2017
- Ecole Polytechnique de Lausanne (Switzerland), October 2017

- Heriot-Watt University (UK), November 2017
- University of Ghent (Belgium), November 2017

"Designing Verifiable Coherence Protocols"

- IBM T.J. Watson Research Center (Yorktown Heights, NY), July 2016
- Cornell University, October 2015
- University of St Andrews (UK), September 2017
- Cambridge University (UK), November 2017

"Cache Coherence: Scalability, New Platforms, and Verification"

- Qualcomm (Raleigh, NC), May 2013

"Verification-Aware Architecture and Fractal Coherence"

- Keynote talk at 3rd HiPEAC Workshop on Design for Reliability (Heraklion, Greece), January 2011
- Washington University (St. Louis, MO), February 2011 "Verification-Aware Architecture"
- Workshop on Resilient Architectures (Atlanta, GA), December 2010

"UNified Instruction/Translation/Data (UNITD) Coherence: One Protocol to Rule Them All"

- AMD (Portland, OR), September 2010
- Intel Corporation (Hillsboro, OR), September 2010

"Detecting Faults and Hardware Bugs Using Dynamic Verification"

- Dagstuhl seminar on Fault Tolerant Distributed Algorithms for VLSI Chips (Dagstuhl, Germany), September 2008

"Post-Silicon Validation Using Dynamic Verification"

- GSRC Workshop on Post-Silicon Validation (Anaheim, CA), June 2008

"Low-cost, Comprehensive Error Detection for Commodity Processors"

- Stanford University (Palo Alto, CA), May 2008; University of California—Berkeley, May 2008; University of Illinois (Champaign-Urbana, IL), April 2008; University of Michigan (Ann Arbor, MI), April 2008

"Why Do We Still Have Bugs?" (panel discussion)

- IBM T.J. Watson Research Center (Yorktown Heights, NY), April 2008

"The Design of Dependable and Variability-Tolerant Multithreaded Architectures"

- IBM T.J. Watson Research Center (Yorktown Heights, NY), September 2006 "Comprehensive Detection of Errors in Multithreaded Architectures"
- Intel Corporation (Hudson, MA), April 2007; University of Texas at Austin, March 2007; Advanced Micro Devices (Austin, TX), March 2007; Carnegie Mellon University (Pittsburgh, PA), February 2007; University of Pennsylvania (Philadelphia, PA), June 2006

"Comprehensive Error Detection for Multithreaded Memory Systems"

- NC State University: Computer Engineering Seminar, November 2005

"Duke FaultFinder Project"

- IBM University Day (Research Triangle Park, NC), October 2005 "Sherlock: Dynamic Verification of Multithreaded Memory Systems"
- Intel Labs (Portland, OR), September 2003; University of British Columbia (Vancouver, Canada), June 2003

"SafetyNet: Improving the Availability and Designability of Shared Memory Multiprocessors"

- University of California—Berkeley, April 2002; University of California—San Diego, April 2002; Stanford University (Palo Alto, CA), March 2002; University of Pennsylvania (Philadelphia, PA), March 2002; North Carolina State University (Raleigh, NC), February 2002; Duke University (Durham, NC), February 2002; Case Western Reserve University (Cleveland, OH), February 2002; Northwestern University (Evanston, IL), February 2002

"SafetyNet: Improving the Availability of Shared Memory Multiprocessors with Global Checkpoint/Recovery"

- Intel Labs (Portland, OR), January 2002

Tutorials

"Verification-Aware Dynamic Power Management" as part of Tutorial on Energy-Secure System Architectures, at the *38th International Symposium on Computer Architecture (ISCA)*, June 2011. "Fault Tolerant Computer Architecture," at the *Sixth International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES)*. Week-long course sponsored by the European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC). Terrassa (Barcelona), Spain, July 2010.

"GEMS: Multifacet's Accurate and Flexible Full System Simulator", at the *32nd International Symposium on Computer Architecture (ISCA)*, June 2005. Organized by Mike Marty, Bradford Beckmann, Luke Yen, Alaa R. Alameldeen, Min Xu, Kevin E. Moore, Daniel J. Sorin, and Milo M.K. Martin

Teaching (Sp = Spring, Fa = Fall)

>> ECE 152: Introduction to Computer Architecture: Sp 2005, Sp 2008, Sp 2009, Sp 2011, Sp 2012

- major updating of course in Sp 2005

>> ECE/CS 250: Computer Architecture: Fa 2012, Sp 2013, Fa 2014, Sp 2016, Sp 2017, Sp 2019, Sp 2021

- developed and first offered in Fa 2012

>> ECE 552 / CPS 550 (was ECE 252 / CPS 220): Advanced Computer Architecture I: Fa 2003, Fa 2005, Fa 2007, Fa 2009, Fa 2013, Fa 2015, Fa 2018, Fa 2020

- first cross-listed with Computer Science in Fa 2003

>> ECE/CS 554 (was ECE 254 / CPS 225): Fault Tolerant and Testable Computing Systems: Fa 2004, Fa 2006, Fa 2008, Fa 2011, Sp 2015, Fa 2019

- major updating of course in Fa 2004

>> ECE 652 / CS 650 (was ECE 259 / CS 221): Advanced Computer Architecture II: Sp 2003, Sp 2004, Sp 2006, Sp 2010, Sp 2014, Sp 2020

- developed and first offered in ECE in Sp 2003
- added to Digital Systems sequence in Sp 2006 (first class with undergraduates)>> I have also taught dozens of independent study courses.

Journal Editor Service

Editor-in-Chief, *Computer Architecture Letters* (2017-present)

Associate Editor-in-Chief, *Computer Architecture Letters* (2015-present)

Associate Editor, *Computer Architecture Letters* (2012-2015)

Subject Area Editor, *Journal of Parallel and Distributed Computing* (2014-2015)

Program Committee Chairmanship

Co-chair (with Milo Martin) of Selection Committee for IEEE Micro's Top Picks in Computer Architecture, 2016

Program chair of HiPEAC 2017

Conference and Workshop Program Committee Service

International Symposium on Computer Architecture (ISCA): 2008, 2009, 2010, 2013, 2015, 2017, 2019, 2020, 2021

International Conference on Dependable Systems and Networks (DSN): 2008, 2009, 2010, 2012, 2013

International Symposium on Microarchitecture (MICRO): 2009, 2010, 2012, 2014, 2015, 2017, 2019, 2020, 2021

International Symposium on High-Performance Computer Architecture (HPCA): 2009, 2010, 2013, 2014, 2015, 2016, 2018, 2021, 2022

IEEE Micro's Top Picks in Computer Architecture: 2012, 2014, 2017

International Conference on Parallel Architectures and Compilation Techniques (PACT): 2009, 2014

ACM SIGMETRICS: 2005

International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS): 2010, 2011, 2012, 2018, 2021

Symposium on Parallelism in Algorithms and Architectures (SPAA): 2004, 2007

International Conference on Computer Design (ICCD): 2006, 2007, 2008

IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS): 2007, 2020, 2021

IEEE International Symposium on Workload Characterization (IISWC): 2011

ACM Computing Frontiers: 2008

International Conference on Parallel and Distributed Systems (ICPADS): 2004

International Conference on High Performance Computing (HiPC): 2007

IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH): 2007

Workshop on Compiler and Architectural Techniques for Application Reliability and Security (CATARS): 2009

Workshop on Quality-Aware Design (W-QUAD): 2008

IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH): 2005, 2006

Workshop on Introspective Architecture (WISA): 2006

Annual IEEE Workshop on Workload Characterization (WWC): 2003

Grant Proposal Panel Service

National Science Foundation—Computing Processes and Artifacts Program: 4 panels

National Science Foundation—Computer Systems Research Program: 2 panels National Science Foundation—Expeditions in Computing

Service to Computer Architecture Community

Referee for the following journals: IEEE Transactions on Parallel and Distributed Systems (TPDS), IEEE Transactions on Dependable and Secure Computing (TDSC), IEEE Transactions on Computers (TC), IEEE Transactions on Circuits and Systems (TCAS), IEEE Micro, ACM Transactions on Architecture and Code Optimization (TACO), ACM Transactions on Computer Systems (TOCS), ACM Transactions on Emerging Technologies in Computing Systems (JETC), IEEE Transactions on Very Large Scale Integration Systems (TVLSI), ACM Transactions on Embedded Computing Systems (TECS), IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.

Referee for the following conferences: International Symposium on Computer Architecture (ISCA), International Symposium on Microarchitecture (MICRO), International Symposium on High-Performance Computer Architecture (HPCA), International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Symposium on Parallelism in Algorithms and Architectures (SPAA), ACM SIGMETRICS, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), Symposium on Operating Systems Principles (SOSP), International Parallel and Distributed Processing Symposium (IPDPS), International Conference on Supercomputing (ICS), International Symposium on Performance Analysis of Systems and Software (ISPASS), Usenix Annual Technical Conference, International Conference on Computer Design (ICCD), ACM MobiSys, International Conference on Parallel and Distributed Systems (ICPADS), Asia-Pacific Computer Systems Architecture Conference, International Test Conference (ITC).

Referee for the following workshops: Workshop on Workload Characterization (WWC), IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH), Workshop on Introspective Architecture (WISA), Workshop on Hot Topics in Operating Systems (HotOS), North Atlantic Test Workshop (NATW).

Publications chair for: 2006 IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH '06)

Finance chair for: 2005 IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH '05)

Service to Department and University

Pratt Undergraduate Research Committee, 2018

Computer Engineering group leader 2012-7, 2018-current

ECE task force on Educational Computing Infrastructure, 2004-5

Evaluator of Duke Fulbright Scholarship candidates, 2004

ECE faculty search committee 2003-4, 2005-6, 2009-10 (chair), 2012 (chair)

Computer Engineering / Computer Science taskforce, 2003

ECE Computing Committee, 2002-2006, 2007-2010 (chair)

ECE Graduate Studies Committee, 2006-8, 2012-current

Pratt IT Advisory Committee (PITAC), 2007-2010 (chair August 2008-2010)

Pratt IT Director Search Committee, 2008

Pratt liaison between faculty and IT, fall 2008 (during search for new Pratt IT Director)

CS faculty search committee 2008-9

Review committee for Duke's CIO/VP of IT, 2012

PhD Graduates

1. Tong Li, Ph.D. 2005, "Self-Monitoring of Thread Interactions for Improved Resource Management in Multithreaded Systems" (co-advised with Alvin R. Lebeck, CS).
2. Albert Meixner, Ph.D. 2008, "Low-cost Methods for Error Detection in Multi-core Systems" (CS)
   • Duke CS Department's Research Initiation Project award, 2005
3. Anita Lungu, Ph.D. 2009, "Verification-Aware Processor Design" (CS)
   • Duke CS Department's Outstanding Masters Thesis award, 2007
4. Fred A. Bower, Ph.D. 2010, "Technology Impacts of CMOS Scaling on Microprocessor Core Design for Hard-Fault Tolerance in Single-Core Applications and Optimized Throughput in Throughput-Oriented Chip Multiprocessors" (CS)
5. Bogdan F. Romanescu, Ph.D. 2010, "Cost-effective Designs for Supporting Correct Execution and Scalable Performance in Many-core Processors"
6. Meng Zhang, Ph.D. 2013, "Scalably Verifiable Cache Coherence"
   • Duke ECE Department's Honorable Mention for Outstanding PhD Award
7. Blake A. Hechtman, Ph.D. 2014, "Exploiting Parallelism in Massively Threaded Throughput-Oriented Processors"
8. Adam N. Jacobvitz, Ph.D. 2014, "Coset Coding to Extend the Lifetime of Non-Volatile Memory"
9. Ralph Nathan, Ph.D. 2015, "Using Runtime Floating Point Accuracy Feedback to Make Automated Precision/Performance Tradeoffs"
10. Opeoluwa (Luwa) Matthews, Ph.D. 2017, "A Formal Framework for Designing Verifiable Systems Protocols"
11. Sean Murray, Ph.D. 2019, "Accelerated Motion Planning Through Hardware/Software Co-Design"
12. Georgios Mappouras, Ph.D. 2020, "Integrating Computer Architecture and Coding Theory to Advance Emerging Memory Technologies"

PhD Advisees

1. Atefeh Mehrabi

Master's Graduates

1. Moky Cheung, M.S. 2004
2. Jiayu (Tom) Gong, M.S. 2014
3. John S. Ingalls, M.S. 2012
4. Jennifer S. Miller, M.S. 2005, "Analytical Evaluation of Performance Variability in Digital Circuits Due to Process Variability."
   • National Science Foundation Graduate Fellow
5. Morakinyo K. Olugbade, M.S. 2011.
   • National Science Foundation Graduate Fellow

6. Nathan N. Sadler, M.S. 2006

7. Alfredo Velasco, M.S. 2016

Postdoctoral Advisees

1. Chris Dwyer

Undergraduate Pratt Fellow Advisees

1. Michael Bauer, B.S.E. 2008
2. William Floyd-Jones, B.S.E. 2017
3. Derek Hower, B.S.E. 2006
   • Won Duke ECE Department's Charles Seager Memorial Award for undergraduate research
4. John Ingalls, B.S.E. 2011
5. Martha Barker, B.S.E. 2015
6. Yaqi Zhang, B.S.E. 2015
   • Won Duke ECE Department's Charles Seager Memorial Award for undergraduate research

PhD Committees

Sandeep Agrawal (CS-advisor Lebeck), Ramin Bashizade (CS-advisor Lebeck, PhD 2020), Ioana Burcea (University of Toronto, advisor Andreas Moshovos, PhD 2012), John Burchett (advisor Brady, PhD 2005), Xiaobo Fan (CS-advisor Lebeck, PhD 2004), Daniel Gaultney (advisor Kim), Marisabel Guevara (CS-advisor Lee, PhD 2014), Tamara Lehman (advisors Lee and Hilton, PhD 2019), Jangwoo Kim (Carnegie Mellon University, advisor Babak Falsafi, PhD 2008), Yang Liu (CS-advisor Lebeck, PhD 2011), Mohammad Mottaghi (advisor Dwyer, PhD 2014), Jaidev Patwardhan (CS-advisor Lebeck, PhD 2006), Constantin Pistol (CS-advisors Lebeck and Dwyer, PhD 2009), Valentin Pistol (CS-advisors Lebeck and Cox), Hyojin Sung (University of Illinois, advisor Sarita Adve), Jun Yang (CS-advisor Lebeck, PhD 2013), Heng Zeng (CS-advisors Lebeck and Ellis, PhD 2004), Rui Zhang (UNC, advisor Cynthia Sturton, PhD 2020), Xiangyu Zhang (CS-advisor Lebeck, PhD 2020), Ying Zhang (advisor Chakrabarty, PhD 2004)

Master's Committees

Sandeep Agrawal (CS-advisor Lebeck), Jeannie Albrecht (CS-advisor Vahdat), Alex Dutu (CS-advisor Lebeck), Xinyi Hong (advisor Cummings), Gang Luo (CS-advisor Babu), Ferdinand Schober (CS-advisor Kedem), Sara Sprenkle (CSadvisor Chase), Jie Xiao (CS-advisor Lebeck), Mahmut Yilmaz (advisor Ozev)

Outreach Students Supervised

Bryan Anthonio, Cornell University, summer 2012; Celanese Bozeman, Shaw University, summer 2008; Vanessa Martinez, Arizona State University, summer 2014; Najae Prelow, Jackson State University, summer 2013; Abigail Schatzman, summer 2016

External Funding

1. Principal Investigator: "SHF:Small: Automatic Generation of Cache Coherent Memory Systems for Multicore Processors." *National Science Foundation CCF-200-2737*, $400,000, July 1, 2020 – June 30, 2023.

2. Co-PI with PI Robert Calderbank: "CIF:Small:High Performance Memories that Integrate Coding and Computer Architecture." *National Science Foundation CCF-1717602*, $470,000, September 1, 2017 – August 31, 2020.
3. Co-PI with PI George Konidaris: "Low-Power, Real-Time Motion Planning for Complex Robots." *Open Source Robotics Foundation*. $100,000, October 15, 2015 – April 15, 2016.
4. Principal Investigator with co-PI Robert Calderbank: "SHF:Small:Using Coding Theory to Optimize the Representation of Information in Computer Architecture." *National Science Foundation CCF-1421177,* $450,000, August 1, 2014 - July 31, 2017.
5. Principal Investigator: "SHF:Small:Designing Architectures to be Formally Verifiable." *National Science Foundation CCF-1421167,* $340,000*,* August 15, 2014 – July 31, 2017.
6. Principal Investigator: "SHF: EAGER: FIESTA: A Sound Multi-Program Workload Methodology." *National Science Foundation CCF-1259028*, $134,472, ended December 31, 2012. (This grant was initially at the University of Pennsylvania under PI Amir Roth and was transferred to PI Sorin at Duke. The initial grant amount was $188,528, some of which was spent before the grant was transferred.)
7. Principal Investigator: "SHF: Small: Shared Memory Architectures and Microarchitectures for Heterogeneous General-Purpose Chips." *National Science Foundation CCF-1216695,* $300,000, August 1, 2012 - July 31, 2015.
8. Recipient of gift of $50,000 from AMD, December 2011.
9. Principal Investigator: "SHF:Small:Commodity Processors with Mainframe Reliability." *National Science Foundation CCF-1115367*, $420,000, July 1, 2011 - June 30, 2014.
10. Recipient of gift of $65,377 from Toyota InfoTechnology Center, March 2009.
11. Principal Investigator: "Correct and Scalable Address Translation for Multicore Processors." *Semiconductor Research Corporation (SRC), Contract 2009-HJ-1881*, $180,000. February 1, 2009 - March 31, 2012.
12. Principal Investigator: "CPA-CSA: Verification-Aware Microarchitecture." *National Science Foundation CCF-0811290*, $220,000. September 1, 2008 - August 31, 2011.
13. Recipient of gift of $90,803 from Toyota InfoTechnology Center, August 2008.
14. Doctoral advisor of IBM PhD Scholarship awardee Anita Lungu, $10,000, 2008-2009.
15. Recipient of gift of $87,573 from Toyota InfoTechnology Center, September 2007.
16. Principal Investigator: "CAREER: Improving Multiprocessor Availability with Dynamic Verification and Autonomic Execution." *National Science Foundation CCF-0444516*, $400,000. June 16, 2005 - May 31, 2010.
17. Principal Investigator with co-investigator Sule Ozev: "Autonomic Computing via Dynamic Self Repair of Hardware Faults." *National Aeronautics and Space Administration (NASA) AISR program #NNG04GQ06G*, $394,198, January 1, 2005 - December 31, 2007.
18. Recipient of gift of 40 Intel computers from Intel Corporation (Hillsboro, OR), November, 2004.
19. Co-investigator with large Duke-wide team: "Shared University Research (SUR)." *IBM*, $150,000, 2004.
20. Doctoral advisor of National Science Foundation Graduate Fellowship awardees: Jennifer S.Miller, Morakinyo K. Olugbade.

21. Co-investigator with PI Alvin R. Lebeck and co-PIs John H. Reif, Paul D. Franzon, and Thomas LaBean: "ITR: Nanoarchitecture: Balancing Regularity, Complexity, and Defect Tolerance using DNA for Nanoelectronic Integration." *National Science Foundation CCR-0326157*, $1,200,000, September 15, 2003 - September 14, 2006.
22. Co-investigator with PI Alvin R. Lebeck. "ITR: Architectural Support for Service Level Agreements." *National Science Foundation CCR-0312561*, $220,004, August 1, 2003 - July 31, 2006.
23. Principal Investigator. "FaultFinder: Improving the Availability of Multiprocessor Servers." *National Science Foundation CCR-0309164*, $114,422, July 15, 2003 - June 30, 2005.