Alignment Tolerant InP/Si CMOS Hybrid Integrated Photoreceivers
Operating at 0.9 Gbps

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The implementation of low cost fiber optic links, including to the home and in-home fiber optic backbones, rely upon the cost reduction of optoelectronic interfaces. Alignment tolerant photoreceivers can reduce the packaging cost of optical links for low cost applications by easing packaging constraints. Previously reported optical alignment tolerance measurements have been reported for speeds up to 200 Mbps [1]. Hybrid integration of compound semiconductor photodetectors with Si CMOS receiver circuits enables independent optimization of both the optoelectronic devices and the circuitry for low cost fiber applications. Previous hybrid integrated receiver results reported to date include a Si CMOS receiver integrated with a thin film PIN GaAs photodiode [2]. The PIN had a 30 μm diameter, circular detecting area, and the integrated receiver operated at 800 Mbps. In another hybrid receiver implementation, GaAs multiple quantum well (MQW) modulator/detectors were bump bonded onto Si CMOS [3]. The integrated receiver demonstrated a data rate of 1 Gbps with device sizes on the order of 50 μm on a side [4]. Herein, we report on the hybrid integration of a thin film large area (250 x 250 μm²), low capacitance (0.43 pF), high responsivity (0.5 A/W, with no AR coating) InGaAs/InP® inverted metal-semiconductor-metal (I- MSM) photodetector onto a Si CMOS differential receiver circuit. In contrast to previously reported results, this hybrid optoelectronic integrated circuit (OEIC) utilized a large area photodetector designed for a high level of alignment tolerance and operation at wavelengths of 1.3-1.55 μm. The integrated receiver (shown in Figure 1) has a measured bit-error-rate (BER) of 10⁻⁵ at 0.9 Gbps and 10⁻¹ at 650 Mbps. The alignment tolerance of this receiver at 650 Mbps has been modeled and measured, and the theoretical results correspond well to experimental data.

The speed of a photodetector is limited by either the RC time constant of the device or the transit times of photogenerated carriers within the device. In general, detector capacitance increases as a function of increasing device area. For this reason, alignment tolerance is often sacrificed so that the input capacitance specifications of the receiver circuitry may be met. Conventional MSM (C-MSM) photodetectors, when compared to PIN photodiodes, have low capacitances per unit area, which enable larger detecting areas for a given input capacitance. However, the interdigitated electrode structure of an MSM shadows portions of the detector’s absorbing region, resulting in responsivities that are considerably lower than PIN photodiodes. By inverting an MSM – essentially flipping a conventional MSM upside down and removing the substrate – the low capacitance per unit area of the C-MSM is retained, and the responsivity of the device dramatically improves since the electrode shadowing loss is eliminated. I-MSMs have shown only slight degradations in transient response when compared to similar C-MSMs [5].

The I-MSM integrated onto the receiver shown in Figure 1 was fabricated from a wafer grown by molecular beam epitaxy (MBE) with the following nominally undoped layer structure: 400 Å InAlAs cap layer, 500 Å graded layer, 7400 Å InGaAs layer, 500 Å InAlAs layer, 2000 Å stop etch layer, and InP substrate. The I-MSM was fabricated and integrated using the process described in [1]. The fully differential Si CMOS receiver circuit was fabricated by National Semiconductor Corporation in the CMOS7 (0.35 μm) process. It consisted of a differential current mode input, current to voltage conversion, and voltage gain stages. The integrated circuit was wire bonded in chip on board format to a printed circuit board for testing.

The performance of the integrated receiver was tested using a DFB laser operating at 1.55 μm pigtailed to a single-mode optical
fiber. The single mode fiber was coupled via FC connectors to a Mach-Zehnder modulator, which was
driven with a pseudorandom pattern by a BER transmitter. The output of the modulator was FC-coupled to
a single-mode fiber patch cord that was cleaved on the opposite end. The cleaved end of the fiber was
positioned in a fiber chuck over the integrated receiver using an XYZ translation stage. A Keithley Source-
Measure Unit (SMU) biased the I-MSM. The integrated receiver demonstrated a BER of 10^{-11} at 650 Mbps
and 10^{-10} at 0.9 Gbps. Eye diagrams of the receiver output at 622 Mbps and 0.9 Gbps are shown in Figures
2 and 3, respectively.

The integrated receiver was modeled and tested for longitudinal alignment tolerance. Longitudinal alignment tolerance refers to receiver performance as a function of the separation between the
surface of the photodetector and that of the emitting source. The mode field diameter of this fiber was given
by the manufacturer as 9.3 μm. Photocurrent as a function of fiber to detector misalignment was measured
at 650 Mbps. The intensity distribution of the beam emitted from the fiber cleave was approximated to
first-order a circular Gaussian with a waist equal to the mode field radius of the optical fiber. The
intensity of the Gaussian beam was integrated over the area of the I-MSM to calculate the percentage of
power coupled from the fiber to the detector as a function of longitudinal separation. Both the theoretical
predictions and the experimental results showed a ~3 dB decrease in coupled power from the fiber to the
detector at a longitudinal separation of 2.9 mm.

Hybrid integration and alignment tolerant OE components are steps toward the realization of low
cost, pervasive OE implementation. In this paper, we report the integration of a thin film large area I-MSM
onto a differential Si CMOS receiver circuit. This integrated receiver demonstrated operation at 0.9 Gbps
and highly alignment tolerant operation at 650 Mbps. Measured alignment tolerance of the receiver
responded well to the performance predicted by theory.

References
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Figure 2 – Eye diagram of receiver output at 622 Mbps.

Figure 3 – Eye diagram of receiver output at 0.9 Gbps.