EPILAYER TRANSFER FOR INTEGRATION OF III-V PHOTODETECTORS
ONTO A SILICON PLATFORM USING Au-Sn AND Pd-Ge BONDING

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ABSTRACT

A novel process to bond InP-based, substrate-removed, vertical Schottky photodetectors to a commercially available silicon read-out integrated circuit is demonstrated as a new technique for optoelectronic hybridization. High-quality In(Ga)As epilayers were bonded to silicon substrates and patterned to form a 320 x 256 focal plane array to demonstrate this technique. The epilayers were joined to the silicon through a metal-metal bond of either Au-Sn or Ge-Pd. Scanning electron and optical microscopy revealed that the Au-Sn formed a eutectic (melting) bond, whereas the Ge-Pd formed a solid-state bond. Samples bonded with Ge-Pd exhibited superior performance and were easier to process than the Au-Sn samples. Using this bonding technique, samples with a dark current density of 595 pA/μm² at -5 V and a peak responsivity of 0.21 A/W over λ=0.8 to 1.5 μm were obtained. Bonded devices survived severe thermal cycling between 77K and 373K. The process described is uncomplicated and does not require any specialized equipment beyond that of a standard photolithography tool.

I. BACKGROUND

Integration of III-V compound semiconductor materials to silicon electronic circuitry combines the application-specific properties of the III-V material with the high-density electronics of silicon technology. Indium bump bonding is currently the standard method of hybrid integration of an array of III-V semiconductor photodetectors onto a silicon read-out integrated circuit (ROIC). Indium bump bonding has been employed to hybridize a variety of devices to silicon [1–4], including CdZnTe, GaAs, and other III-V compound semiconductors. By bonding an array of III-V detectors onto a silicon ROIC, one has the advantage of being able to optimize the detectors and the read-out electronics separately. In principle, any semiconductor device can be developed independently and bonded to a silicon platform in order to add a certain functionality that would not otherwise be available in a silicon-only system.

Although indium bump bonding has been used to bond detector arrays with a pitch as small as 11.5 μm [2], it requires a complicated procedure where the completed detector array must be aligned to the contact pads on the ROIC. This procedure requires a specialized indium bump alignment and bonding tool that is not commonly found in most cleanroom facilities. We propose a wafer-to-wafer soldering process where each bond member is coated with a metal and joined by the metal-metal interaction at an elevated temperature and pressure. The bonded metal layers serve as a single “compliant layer.” After bonding the III-V substrate is removed, and the remaining epitaxial film is patterned by standard photolithography techniques. Any two wafers can be joined in this manner, and epilayer transfer can be accomplished so long as its surrogate substrate can be chemically removed. This process allows fabrication of smaller area detectors with higher detector densities and improved alignment accuracy, limited by the resolution of the photolithography and patterning process. These factors are especially important for multi-spectral focal plane array (FPA) technologies that require a high density of bonded devices to produce a high-resolution image for each spectral band [5].

We have investigated the Au-Sn and Pd-Ge systems as bonding films to form the compliant layer at temperatures ~350°C. The temperature must be such that the excess heat will not affect device structures on either bond member. Figure 1 is a schematic diagram of the epitaxial layer transfer process. One metal is first patterned above each ROIC electrical contact to form a bonding pad. The epilayer film on the other bond member is uniformly coated with the other metal and is joined to the bonding pads. Individual devices are formed by removing the substrate and then patterning the remaining epilayer film. This process requires that (1) the chosen metals on both bond members withstand the HCl etch used in the InP substrate removal and (2) the metal film on the InGaAs side must be easily patterned by a dry or wet etch to define individual pixels. Gold-tin was investigated because the AuSn alloy is resistant to the HCl etch and Sn can be removed by a dilute HF/H2O2 solution. Palladium-germanium also withstands the HCl etch, and
FIG. 1: (a) Schematic diagram of how InP-based epilayers coated with Sn are bonded to Ti/Au bonding pads on a silicon wafer. After bonding, the InP substrate is removed, and material that is not located over the bonding pads is etched away. (b) The same as above, but with Pd-Ge.

Ge can be removed by a fluorine-based reactive ion etch (RIE) process or a $\text{H}_2\text{O}_2$ wet etch.

II. EXPERIMENTAL PROCEDURE

A silicon substrate and an In(Al)GaAs epilayer structure on InP were prepared by performing a dilute HF (1%) dip and coated with metal by electron beam evaporation. (The actual epilayers are listed in Table I.) In the case of the of the silicon bond member a photosist lift-off layer was first established before metal deposition to achieve an array of bonding pads (see Fig. 1). For Au-Sn, 500 Å of Ti followed by 3500 Å of Au was deposited onto the silicon. The deposition sequence for the epilayer side was 200 Å of Ti, 200 Å of TiN, 40 Å of Ti, and 2000 Å of Sn. The bond members were joined at the Au/Sn interface. For Pd-Ge, 500 Å of Ti followed by 600 Å of Pd was deposited onto the silicon. The deposition sequence for the epilayer side was 200 Å of Ti, 200 Å of TiN, 100 Å of Ti, and 1000 Å of Ge. The bond members were joined at the Pd/Ge interface.

Samples were pressed together under vacuum at a pressure of 14 psi and bonded at ~350°C for 30-40 minutes. After bonding, the InP substrate was removed with a combination of mechanical polishing and selective chemical etching (80% HCl); only the thin epilayer structure remained on top of the metal bonding layers. The epilayers were patterned into mesa's over the bonding pads with a 10:1:1 solution of $\text{H}_2\text{O}_2\cdot\text{H}_3\text{PO}_4\cdot\text{H}_2\text{O}$ [6]. The remaining material between the mesas was removed by a wet or dry etch. Cr/Au ohmic contacts were deposited to complete the device. The final structure is a mesa of epiayers bonded to a silicon substrate with electrical contact to the substrate made through the bonding layer.

For comparison, samples were also fabricated by epoxy bonding to a glass substrate (see Ref. 6 for fabrication details). The epilayers were coated with the entire sequence of films (Ti/TiN/Ti/Ge/Pd/Ti) used in the Pd-Ge bonding. Epoxy-bonded samples do not experience the elevated temperature and pressure that occurs during a Pd-Ge bonding process. These samples will serve as a reference for the Pd-Ge bonded samples that do experience an elevated temperature and pressure.

### Table I: Thickness and doping of epitaxial film sequence on InP that is transferred to the silicon substrate.

<table>
<thead>
<tr>
<th>Substr.</th>
<th>InP</th>
<th>n⁺</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>In₀.₈₅Ga₀.₁₅As</td>
<td>$n = 5 \times 10^{18}$</td>
</tr>
<tr>
<td>2</td>
<td>InP</td>
<td>$n = 1 \times 10^{19}$</td>
</tr>
<tr>
<td>3</td>
<td>InP</td>
<td>undoped</td>
</tr>
<tr>
<td>4</td>
<td>In₀.₈₅Ga₀.₁₅As</td>
<td>undoped</td>
</tr>
<tr>
<td>5</td>
<td>In₀.₈₅Al₀.₁₅As</td>
<td>undoped</td>
</tr>
</tbody>
</table>

III. RESULTS AND DISCUSSION

The bond members were joined at ~350°C through either Au/Sn-based eutectic soldering or Ge-Pd solid state bonding. In the case of Au/Sn-based eutectic soldering, a bond is formed when the Au and Sn metals on each bond member mix to form a eutectic ($T_e = 278°C$) [7]. A 320 x 256 array of InGaAs photodetectors with a 30-μm pixel pitch was fabricated using Au-Sn. The left-hand side of Fig. 2 shows the epilayer mesa's produced by Au-Sn bonding. Though each mesa is securely bonded to its metal post, the AuSn alloy was found to protrude from each of the bonding pads because the alloy became liquid at the bonding temperature. We could not achieve satisfactory bonding at lower temperature settings. The protrusion of alloy between the mesas prevents the electrical isolation of each device. The alloy could not be chemically removed because of the presence of Au.

An alternative is found in using a Pd-Ge interface to join the two bond members. Pd-Ge films have been studied as ohmic contacts to III-V compound semiconductors [8-10]. In fact, Pd is well-known to react with GaAs and Si to form intermediate phases at temperatures less than 200°C [11-14]. Unlike the Au-Sn process, the Ge-Pd reaction is a solid state bond. The driving force to form Pd-based compounds results in a metallurgical bond without the material softening or liquefying under the bonding conditions. The right-hand side of Fig. 2 shows how the
Pd-Ge bond process does not leave any residual material between the pixels. To the authors’ knowledge, this is the first time Pd and Ge have been used to join two separate bond members together. Although Pd and Ge are not usually considered “low temperature” materials, the high surface diffusivity of Pd and its ability to penetrate and react with native oxides of semiconductors at temperatures less than 200°C makes it a unique material for wafer bonding purposes [12].

The robustness of the Pd-Ge bond is manifested during InP substrate removal and other subsequent processing. Samples were subjected to considerable mechanical agitation while grinding and exposed to a concentrated (80%) HCl soak while etching off the InP substrate. However, the bonded epilayers remained attached and continuous across the sample area. Patterned mesas were additionally subjected to extreme thermal cycling between 77K and 373K. After eight cycles between the high and low temperature environments, 99% of the mesas were observed to remain intact and unaffected. After sixteen cycles, 90% of the mesas remained, attesting to the mechanical toughness of the Pd-Ge bond.

Current-voltage measurements on discrete devices revealed a rectifying behavior as expected from the InAlAs/Ti Schottky junction. Figure 3 shows the reverse I-V characteristics of a Pd-Ge bonded sample and an epoxy-bonded sample. Both samples exhibited similar leakage currents in the hundreds of nanoamps range. The epoxy-bonded sample manifested a leakage current density of 444 pA/µm², and the Pd-Ge sample showed a leakage of 595 pA/µm², both at -5 V. Because the epoxy-bonded sample was not subjected to heating and pressing, it was expected to have a lower leakage current than the Pd-Ge bonded sample. But because the leakage current from the two samples is about the same, the heating and pressing during Pd-Ge bonding must not significantly affect device performance. Thus, Pd-Ge bonding is an ideal process for metallurgically joining two bond members at low temperature and low pressure without negatively impacting any existing device structures or material quality.

Responsivity measurements were taken in the near infrared from 1000 nm to 1700 nm by using a 0.15-m monochrometer and lock-in amplifier. Light from the monochrometer was coupled into a fiber, whose output facet was positioned over the detector. Figure 4 shows the responsivity of a discrete InGaAs Schottky detector, which was Pd-Ge bonded to a silicon substrate. Interference effects due to the finite thickness of the epilayer are observed [15]. A peak responsivity of 0.21 A/W was measured at λ = 1220 nm. Responsivities could not be measured in epoxy-bonded samples because their leakage characteristics quickly degraded after applying a voltage. These samples are suspected to degrade because of Joule heating in the metallization and poor heat dissipation through the epoxy and glass substrate. Thicker metallization should alleviate this problem.

Though higher responsivities have been observed in previously fabricated devices [6], these preliminary devices show that the Pd-Ge bond yields a suitable mechan-
ical and electrical contact for III-V epilayers hybridized to silicon. A number of optimizations will be examined in further study, including lowering the bonding temperature and examining the effects of the bonding process on the InAlAs/Ti Schottky interface. Future devices for bonding to a ROIC will probably employ a p-n junction for better leakage current performance.

IV. CONCLUSIONS

An new epitaxial film transfer process has been demonstrated for III-V compound semiconductor hybridization to silicon. Epilayers grown on InP have been transferred to silicon substrates by Au-Sn and Pd-Ge bonding at temperatures ~350°C. Wafers bonded with Au and Sn could not be fabricated into FPAs because the resulting AuSn alloy could not be removed from between the individual pixels. To avoid the problems associated with the Au-Sn eutectic solder, Pd and Ge were used. The high reactivity of Pd to Ge fuses the two materials upon contact without forming a eutectic melt. Furthermore, the Ge is easily etched by RIE. Using Pd-Ge, InP-based epilayers were metallurgically bonded onto a silicon substrate and patterned into FPAs. Discrete devices were also fabricated to electrically and optically characterize the devices that underwent the Pd-Ge bonding process. Schottky barrier diodes with reverse leakage current densities of ~500 pA/µm² and peak responsivities of 0.21 A/W were measured. Pd-Ge bonding is an effective means to hybridize III-V epitaxial films onto silicon.

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REFERENCES