Passive Device Modeling Methodology Using Nonlinear Optimization

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Abstract
In this paper we describe a method of accurately modeling new passive devices by deembedding the many building blocks from which they are built from just a few test structures. We use a nonlinear optimizer to find the optimal models for the building blocks by fitting extensive high frequency measurements of the test structures behavior. Key results are: the number of test structures needed is much less than the number of parameters and building blocks to be extracted; the extracted models of the building blocks are very predictive of the behavior of new devices built from them; and this methodology is much faster than other finite element like methods.

1. Introduction
Accurate modeling of integrated passive components is becoming very important for the accurate design and fabrication of compact, high performance systems. In applications where resistors play an integral role, their behavior must be accurately modeled. For relatively low frequency systems, resistors can be approximated as ideal components with low error. However, for higher frequencies this assumption is no longer valid, since parasitic effects must be considered to obtain accurate models.[1]

This paper uses a modeling concept that predicts the behavior of passive structures that are comprised of several key geometrical building blocks. The building block equivalent circuits are derived from fabricated test structures and measurements using optimization and extraction routines. Passive RLC models for each embedded building block are extracted and take into account effects of process nonidealities and unknown material properties. The objective here is to predict the electrical behavior of arbitrary geometry passive devices in a standard circuit simulator, thus enabling a major increase in modeling speed over methods that do not utilize lumped elements.

To be a practical method it is necessary that the number of test structures needed to accurately model all of the building blocks required be as few as possible. We show in this paper that the number of test structures can be much fewer than the number of parameters and building blocks used. Specifically, we model four building blocks with 18 parameters from only two test structures. We show that the predictive capability of the resulting models for new devices fabricated from the building blocks is both accurate and very fast.

2. Design and Modeling Flowchart
The modeling methodology can be described in a flow diagram, as shown in Figure 1. The first step in the modeling process is to identify what devices to model in a process, and identify building blocks and design rules. The next step is to design and fabricate test structures to characterize. Next, the test structures are characterized for building block circuit extraction. The measured data is then used to set up optimizations and determine initial guesses to extract equivalent circuits of the test structures and building blocks. Once successful optimizations have been achieved, then the building blocks with associated models and design rules are combined in a library.

3. Detailed Resistor Modeling Procedure

3.1 Devices Modeled
Most resistors are designed in straight lines or serpentine structures; however, the layout of choice for high frequency applications is usually straight lines. It is attractive to explore serpentine resistors for high frequency applications for several reasons. First, serpentine resistors are more efficient in substrate area for the same resistance value, and, if modeled correctly, could have larger application in the high frequency arena. Secondly, the serpentine structure presents a difficult modeling problem due to higher levels of parasitics, such as coupling effects between the segments of the structure, potentially affecting the overall system response.[2]

3.2 Identify Building Blocks
Serpentine resistors fabricated with 25 μm linewidths and spacings were considered. The serpentine geometry dictated three fundamental building blocks that required characterization: 1.) a square building block with connections on opposite sides; 2.) a U-
shaped section connecting two parallel segments of the resistor together; and 3.) a coupled block segment to characterize line to line coupling behavior on a per square basis. Due to testing requirements, a probe pad was added as a fourth building block. Coupling was only considered with respect to nearest neighbors. The building block sizes could be determined by a current flow visualization tool.[3]

Current visualization software was used to predict current flow through a representative serpentine resistor, shown in Figure 2. The cutoff points for each of the primitives were at the areas where the current contours stopped changing rapidly, indicating constant current flow between the boundaries. Using this approach, the pad primitive was taken to be the large pad square plus one adjacent line square, the material square and coupled material square were taken as one unit of material square each, and the U shaped primitive was represented by 3 squares on each of the horizontal and vertical axes of the U shape.

![Figure 2: Current distribution plot of serpentine resistor structure.](image)

### 3.3 Equivalent Circuits

Each building block is modeled as a SPICE compatible RLC circuit. For simple uncoupled building blocks, such as a piece of straight line, simple RLC models based on the partial element equivalent circuit (PEEC) are used for equivalent circuits.[4] In the case of blocks where coupling is examined, e.g. coupled material squares (corresponding to coupled adjacent lines or interacting material squares), coupled PEEC models joined by coupling capacitances and mutual inductances are used, as shown in Figure 3.

![Figure 3: Uncoupled and coupled PEEC circuits with associated building blocks.](image)

### 3.4 Test Structures

Once the building blocks have been defined, the next step is to characterize and develop models. This is achieved through the use of carefully designed test structures. The test structure set is designed to include all of the predefined building blocks. The equivalent circuit of the test structure is made up of the equivalent circuits of each of building block. Once designed and fabricated in the process of interest, high frequency measurements are taken and used to characterize each of the building blocks.[5]

By virtue of device measurements, no assumptions are made regarding material properties, layered dielectrics, or imperfect substrates, because all of these effects are represented in the measured data. This makes the modeling procedure entirely process independent.

To model the four stated building blocks, two test structures were fabricated, as shown in Figure 4. The first test structure is simply a line with probe pads on the two ends. It is used to characterize basic uncoupled material parameters, including self resistance, inductance, and capacitance.

The second test structure is a 3-segment meander resistor. This structure allows passive characterization of the U-shaped corner segments as well as line to line mutual inductance and coupling capacitance.

![Figure 4: Test structures and primitives for meander resistor modeling.](image)

It is interesting to note that a structure with first order coupling is actually a 4-port structure, whereas the test structures are only 2-port devices. Thus only standard, repeatable 2-port measurements are necessary. A 4-port device is much more difficult to measure in practice than a 2-port, since many different excitation and loading iterations are required. The method of simply measuring two port structures and extracting all required multipport information is a significant advantage over attempting to measure coupling between physically disconnected devices.

### 3.5 Processing and Measurement

The test structure design was fabricated by depositing gold on a 96 % alumina substrate, which had a surface roughness of approximately +/- 1.5 μm. A photomicrograph of the fabricated test structures is shown in Figure 5.

The test structures were measured using network analysis techniques, a DC curve tracer, and a high precision multimeter. For the high frequency measurements, a HP 8510C network analyzer was used with a Cascade Microtech probe station and ground-reference-ground configuration probes. Calibration was accomplished using a calibration substrate and utilization of the line-reflect-match (LRM) calibration method. Data was gathered for each of the test structures at over 200 frequency points between 500MHz and
20\text{GHz}, and were stored with the aid of computer data acquisition software and equipment. DC I-V measurements of the test structures were also made in order to ascertain component resistances. At DC, parasitic capacitance and inductance have no effect on the response and the measured resistance value, and, once properly apportioned, can be used directly in the models of the building blocks.

Figure 5: Photograph of fabricated structures for meander resistor modeling.

3.6 Modeling and Parameter Extraction

Circuit models must be generated for each of the defined building blocks. The circuit topologies and parameters for the uncoupled and coupled building blocks are shown in Figure 6. These circuits represent models for the building blocks only; the test structures and resistor circuits are comprised of many building block circuits connected in accordance with the structure geometry.

Figure 6: Building blocks, equivalent circuits and parameter values for serpentine resistor modeling.

The extraction of the circuit model parameters was achieved in several steps. Due to the highly nonlinear nature of the generated system equations with respect to circuit parameter values, a procedure of hierarchical optimization with respect to measured S-parameter and DC resistance data was chosen.[6] All optimizations and simulations were done using the Hspice circuit simulator on Sun Sparcstation 20 series workstations.

The starting point or initial guess of the circuit parameters was crucial for correct optimization results. Therefore, an initial optimization was done assuming that each test structure was comprised of one building block utilized repetitively across the length of the structure on a per square basis. This method was very effective for obtaining a good starting point for the optimization of the test structure circuits. Optimizations were performed for frequencies up to 10 GHz, and results for the meander resistor test structure (shown in the bottom of Figure 4) are shown in Figure 7.

Figure 7: Measured vs. modeled results for the meander resistor test structure: (a) \( S_{21} \) real and imaginary response; (b) \( S_{11} \) real and imaginary response.

3.7 9 Segment Meander Resistor

The computed fundamental building block models were used to predict the behavior of a 9 segment meander resistor. An equivalent circuit of the resistor was constructed by replacing each building block in the structure with its equivalent extracted circuit, as shown in Figure 8. Since only first level coupling was taken into account, each material square in each segment of the resistor was coupled to its nearest neighbor by a pair of mutual inductances and a coupling capacitance. As inferred from the circuit description, the resulting circuit using 25\text{um} linewidths and 300\text{um} line lengths per segment 9 segment resistor was a complex, highly interconnected system, consisting of approximately 700 nodes. The longest path length of the resistor was approximately 0.35 wavelengths long at 10GHz.

Figure 8: Serpentine resistor and associated building blocks.

3.8 Results

In spite of the large circuit size, the AC small signal circuit simulation was completed in less than 2 minutes. The predicted S-parameters, shown in Figure 9, were compared to measured values for the same structure. Both real and imaginary parts of \( S_{11} \) and \( S_{21} \) were accurately predicted up to 5GHz. In comparison, the same structure was designed and simulated in a method of moments solver with a 3GHz meshing frequency. The structure required 72 minutes to complete, while consuming approximately 50MB of system memory while utilizing 2 processors.
in a multiprocessing Sun workstation. Thus, for this example, a speedup factor of approximately 35 was demonstrated.

Figure 9: Measured vs. predicted results for 9 segment resistor: (a) S_{11} real and imaginary response. (b) S_{11} real and imaginary response.

3.9 Voltage Divider

In addition to confirming an S-parameter match between predicted and measured values, two of these resistors connected in a voltage divider configuration was also considered. A divider structure was not fabricated therefore, the target response was generated by modeling the S-parameters of the structure using our technique, and comparing these predicted results to an equivalent circuit modeled using a RF simulator (Hewlett Packard MDS). The divider circuit, shown in Figure 10, was created using standard SPICE netlist techniques.

Figure 10: Resistor divider circuit.

3.10 Results

The predicted resistor model circuit response, shown in Figure 11, models the divider behavior extremely well, matching the results generated by MDS up to approximately 10 GHz. In addition, the unusual voltage divider peaking behavior of the MDS response beyond 10 GHz was mimicked by our circuit, with the voltage peak frequency predicted slightly earlier in this case.

Figure 11: MDS generated vs. predicted results for voltage divider circuit: (a) Voltage magnitude response. (b) Voltage phase response.

4. Summary

This paper shows with enough frequency points and sufficient sensitivity, accurate equivalent circuit extraction of individual building blocks from multi building block test structures is possible. The fact that we can formulate a non-singular system of equations for a linear network, with each equation generated by a different frequency point, leads to the idea that simply by sampling the system over frequency, we can obtain all the information necessary to de-embed the various circuit parameters which comprise that system.\[1\] So, many more than one unknown sets of equivalent circuit parameters can be de-embedded from the measurements of one test structure.

5. References


