Capstone Design - Gigabit Ethernet
Midterm Report

Group 7

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1 – Abstract

The field of modern communications has an ever increasing need for improved means of data transfer, with emphasis on high speed and high quality technologies. The goal of this project is to design, implement and test a Gigabit Ethernet optoelectronic link that will work at a frequency of 1.25 GHz, and perform well under attenuation. The project deals with the design of a transceiver board which transmits data at a Gbps (gigabits per second) rate. The essence of the design is to calculate the transmitting laser’s bias currents, and implement filtering circuits to avoid electronic noise on the component. Once the design is complete, it will be fabricated and soldered on a PCB board, and then tested for performance and accuracy. Conclusions will be drawn as to the significance of the results and the importance of the design project. It is also intended to eventually discuss the role of the technology in the real world and try and generalize it into the big picture, and draw conclusions beyond the scope that is presented.


2 – Introduction

2.1 – General Background

Gigabit Ethernet is the latest in a series of networks based upon Ethernet, and is simply the most successful LAN networking technology available. Ethernet began as a 3 Mb/s network that operated over a coaxial cable. It was then standardized by the IEEE in 1982 as a predominantly 10 Mb/s network, and later evolved to support thin coaxial cable, fiber optic cable, and unshielded twisted-pair. The standardization of Ethernet over ordinary unshielded twisted-pair cable led to a growth in Ethernet that few people at the time imagined. Millions upon millions of Ethernet adapters, repeaters, and other networking equipment required to connect Ethernets together were sold. But this wasn’t enough. The rapid increase in computing power, computing resources, and the need to interconnect these computing environments led to a demand for faster networks. These requirements, along with general improvements in technology, silicon processes, and the resulting ability to cost-effectively transmit and receive data over ordinary telephone cable at 100 Mb/s led to the development and standardization of a 100 Mb/s version of Ethernet, Fast Ethernet. These networks ran the Ethernet protocol, only ten times faster. Therefore, Fast Ethernet provided a simple method to migrate overloaded 10 Mb/s networks. It too was, (and still is) hugely successful [15].

Gigabit Ethernet was the natural evolution after the development and widespread deployment of networking equipment based on Fast Ethernet (100BASE-T) technology. During the development of 100BASE-T, many claims were made by industry analysts, observers, and vendors as to how quickly this new technology would be adopted, and whether it was needed or just perceived to be needed. However once 100BASE-T standard was completed, vendors immediately introduced a torrent of products based on it. Costs associated with deploying 100BASE-T quickly fell, and the installed base of latent 100BASE-T devices leaped.

Gigabit Ethernet provides the data rate increase required to take the technology into a new high-speed era. Gigabit Ethernet is founded on key principles of 10Base-T, fast and switched Ethernet, and the Ethernet frame format over either shared or switched media in a network using standardized structured cabling. The Gigabit development team took the physical layer originally developed for the Fiber Channel Standard, improved it,
and incorporated into the physical layer of Gigabit Ethernet. The result is another tenfold increase in Ethernet rate, at a lower cost, and in less time than would have been required to develop a new technology. Gigabit Ethernet was approved as a standard in 1998. The primary longer-distance Gigabit Ethernet link media is single-mode optical fiber (SMF) with 10μm core diameter or multimode optical fiber (MMF) with either a 50μm core diameter or 62.5μm core diameter. Two transmission wavelengths, 850 nm (SX-short wavelength) and 1300 nm (LX-long wavelength) are supported.

To allow for the speed increase from 100 Mbps Fast Ethernet up to 1 Gbps, changes needed to be made to the Gigabit Ethernet architecture. The Gigabit Ethernet architecture essentially looks identical to that of Ethernet from the data link layer upwards, but the changes reflect inclusions from the ANSI X3T11 FiberChannel technology. The IEEE 802.3Z standard architecture for the Gigabit Ethernet is summarized in Figure 2.1.1 below.

![Figure 2.1.1 - IEEE 802.3Z standard architecture](image)

### 2.2 Optical Elements

This paper will focus on building part of the Physical Media Dependent (PMD) Layer of the Gigabit Ethernet architecture. For this project, a transmitter and receiver will have to be designed and built for a 1.25 Gbps Optoelectronic link.
The Group optoelectronic link will have two active components. They are a Vertical Cavity Surface Emitting Laser (VCSEL) on the transmitter side and a Photodiode (PD) on the receiver side.

Vertical Cavity Surface Emitting Laser (VCSEL) is a key component in the TX design. The differential input coming into an integrated circuit and coming out as a current drives the VCSEL to produce a laser. This laser enters an optic fiber leading up to the photodetector on the RX side. VCSELs are composed of several layers of mirrors that are produced by semi-conductors with varying compositions. These mirrors reflect a narrow range of wavelengths back into the cavity that in return causes the light emission of just one wavelength. Figures 2.2.1-2 demonstrates this description. VCSELs are used because they give high performance and are cost effective. They also tend to have other advantages including low threshold currents, low temperature sensitivity, high transmission speed with low power consumption, and easy alignment and production packaging due to a geometry which is similar to the photo detectors.

VCSELs could be purchased “connectorized” or “unconnectorized.” Connectorized components are pre-aligned and factory-tested to ensure minimal insertion-loss. The outside connectorized end will generally have a protective shroud that prevents damage to the connectors during installation. For this project VCSELs will be assessed by divergence angle, threshold current, and slope efficiency. Beam divergence angle is defined as the light intensity full width at the $\frac{1}{e^2}$ intensity level. Threshold
current is the minimum current that turns the VCSEL on. Slope efficiency is the ratio of the output power (micro watts) to input current (mA).

Photodiodes are used to detect the incoming light signal from the transmitter. Photodiodes are usually of the P-I-N form where a p-type and n-type semiconductor has an intrinsic region in between. Photodiodes have three characteristics that are critical in optoelectronic data links. These are the photodiode responsivity, capacitance and receiver area. Maximizing the receiver area allows more coupling between the fiber optic line and the photodiode. Responsivity is a term used to describe the sensitivity of the photo detector, which is given in Amps of current per Watt detected (A/W). Smaller capacitance values decrease the response time for the photo detector, which is critically important for the high speed that data is being transmitted.

2.3 – Design Project Description

The purpose of this project is to design and implement an optical transceiver that complies with the Optical Gigabit Ethernet standard IEEE 802.3z. During the course of the project, the group members will follow a self-assigned task and time management plan. The design must be carried out on a $350 budget allowance provided by the Georgia Tech ECE department. A system level design topology is provided by the instructors and recommended as guidance for the system design. As an initial step, a receiver board is provided without optical photo detector circuitry. After the electrical-only receiver board is assembled and tested, the group must design photo detector circuitry to integrate with the provided receiver design. Finally, the group will design an optical transceiver circuit, which interfaces and combines the transmitter with the optical receiver on the same board. Parts provided include the Maxim 3266 trans-impedance amplifier (TIA), Maxim 3264 limiting amplifier, and the Maxim 3287 laser driver. The MAX3287 in essence converts the input electrical signal into current which feeds the VCSEL and generates the output laser. The MAX3266 converts the current from the photo-detector into a differential voltage, and the MAX3264 “digitizes” this signal by trimming it into high and low signals (zeros and ones) [3,4,5]. The signal source used as a pattern generator for testing is the Tektronix GTS1250 GBIC test system. The oscilloscope used for measurements is the Tektronix TDS7154 Digital phosphor oscilloscope.
2.4 - Time Management

To accomplish the goals of this project, a Gantt chart was created as a timeline of how the work should be divided up and completed. It follows from the chart, shown in Figure 2.4.1, that research and gathering information is to continue till the end of the first run and beginning of the second run. Chronologically dividing the tasks gives the group an idea of when to complete the task and what to start on next if the task is to be completed early. It also gives them ample time to plan their time and schedules in a systematic manner. The ordering of parts and layout can be spaced such that the testing can be scheduled. A weekly update of the Gantt chart is done and Figure 2.4.1 is the updated Gantt chart until the first week of March.

![Figure 2.4.1 - Gantt Chart](image)

2.5 - Division of Labor

To maximize the efficiency of the group a delegation of tasks to individuals according to their specialties was essential. The project was divided into six main tasks and a minimum of two people was assigned to each of the tasks. These people would be primarily responsible for the tasks and through group meetings each person would present their findings and give recommendations. This sharing of knowledge amongst the individuals in the group would enable any group member to temporarily assume another member’s role if that person was not able to complete a task because of other obligations. The specific areas assigned can be seen in Table 2.5.1 and are described in detail below.
### Table 2.5.1 - Division of Labor

<table>
<thead>
<tr>
<th>Tasks</th>
<th>Members Responsible</th>
</tr>
</thead>
<tbody>
<tr>
<td>Website Management</td>
<td>Shilo</td>
</tr>
<tr>
<td>Writing &amp; Editing</td>
<td>Shilo, Dhairya (Editing)</td>
</tr>
<tr>
<td></td>
<td>All (writing)</td>
</tr>
<tr>
<td>Purchasing / Ordering</td>
<td>Dhairya, Jed</td>
</tr>
<tr>
<td>Soldering</td>
<td>Courtenay, Jed</td>
</tr>
<tr>
<td>Test &amp; Measurements</td>
<td>Courtenay, Pranjal</td>
</tr>
<tr>
<td>Layout &amp; Design</td>
<td>Courtenay, Shilo</td>
</tr>
<tr>
<td>Coordination / Budget</td>
<td>Dhairya, Shilo</td>
</tr>
</tbody>
</table>

The writing and editing of papers and presentations were held an important task and Pranjal and Shilo were responsible for it, though each member of the group writes some of the report’s section which closely relates to his work. Purchasing of active and passive components and ordering the board once the layout was completed was to be done mainly by Dhairya and Jed. The Soldering of parts was to be done by Jed and Courtenay. The test and measurements after the soldering was to be done by Courtney and Pranjal. Layout and Design was mainly carried out by Courtenay. Shilo aided in layout reviews. The overall coordination and financial budgeting were to be done by Dhairya and Shilo. It was generally conceded ahead in the early stages of the project that time management and group efficiency were of high priority. Group communication was handled mostly through email, and group meetings were held twice (if not more) each week, usually on Monday and Wednesday afternoon. The group also created a project website [13], in which all relevant information could be found, including an online calendar, presentations, data sheets and more.

### 3 - Optical Link Budget

#### 3.1 – General Idea

The optical link budget is meant to estimate the ranges of bias and modulation currents to the MAX3287 laser driver. The driver will then supply the chosen VCSEL with a total amount of current (I_{tot}) which will meet the threshold demand of the laser diode and cause it to lase constant optical power output (P_{out/max} or for simplicity P_{out}) that
meets the Eye Safe criteria [eye safe]. This power will then propagate through the optical fiber while suffering losses of -7.5 dB (approximately 82.2% power loss). When the signal reaches the photo-detector, the diode outputs a current \( I_{\text{TIA(in)}} \) which is then the input to the MAX3266 TIA. The transimpedance amplifier converts the current into a differential output voltage \( V_{\text{LA(in)}} \), and the MAX3264 limiting amplifier ‘translates’ this voltage into a digital signal [3]. Figure 3.1.1 demonstrates the idea using a block diagram.

![Figure 3.1.1 – Block Diagram of the Optical Link Budget](image)

### 3.2 – VCSEL and Optical Fiber Calculations

We began with the known Eye Safe power limit, which was estimated at 1 mw. Since specific values concerning this value do not appear in the IEEE 802.3z or the Eye Safe specs, we picked this number based on others’ past experiences [14]. Knowing this output power to the VCSEL as well as the ranges of threshold currents \( I_{\text{th}} \) and slope efficiency \( \eta \) found in the data sheets [6,7], we used equation 3.2.1 to find the total current into the laser.

\[
I_{\text{tot}} = \frac{P_{\text{out}}}{\eta} + I_{\text{th}} \quad \text{(Eq. 3.2.1)}
\]

Since the design of the transmitter deals with worst possible scenarios, we calculated the total current for 4 combinations of slope efficiency and threshold current based on the
minimum and maximum values in the data sheets:

\[ \{ \eta_{\text{min}} / I_{\text{th}(\text{min})}, \eta_{\text{max}} / I_{\text{th}(\text{max})}, \eta_{\text{min}} / I_{\text{th}(\text{max})}, \eta_{\text{max}} / I_{\text{th}(\text{min})} \} \]

The latter two being the worst possible combination of these variables. We then continued by calculating the output power at the end of the optical fiber, which is equal to the power input to the photo-detector \((P_{\text{in(PD)}})\). Using the value of -7.5 dB for attenuation in the fiber, we used equation 3.2.2 to find \(P_{\text{in(PD)}}\):

\[
P_{\text{in(PD)}} = P_{\text{out}} \cdot 10^{-\alpha/10} \approx P_{\text{out}} \cdot 10^{-0.75} = 0.1778 \cdot P_{\text{out}} \quad \text{(Eq. 3.2.2)}
\]

Where \(\alpha\) is the attenuation in the fiber and \(P_{\text{out}}\) is the Eye Safe laser output power (taken as 1 mw). The above equation demonstrates that the fiber attenuates about 82\% of the input power, and the power into the photo-detector evaluates to \(P_{\text{in(PD)}} = 0.1778\) mw. The range of \(I_{\text{tot}}\) varies according to the biasing of the VCSEL about the active region. This is shown in Figure 3.2.1.

![Figure 3.2.1 – VCSEL output power vs. input current curve.](image)

It can be seen that the total current is ranged between a maximum and minimum values, which then correspond to max, and min values for the VCSEL output power. Since the maximum output power \((P_{\text{out(max)}})\) was determined to be 1mw, we had to define the minimum output power. This was done using the “extinction ratio” (denoted ‘ER’) given...
in the IEEE 802.3z, and its value is about 9.5 dB (different values, from 9 to 10 dB are used to be on the safe side). This ratio relates the minimum and maximum output powers from the VCSEL [15]. Using equation 3.2.3 we found the value of $P_{\text{out/min}} = 0.1122 \text{ mw}$. 

$$P_{\text{out/min}} = P_{\text{out/max}} \cdot 10^{-(ER/10)} \quad \text{(Eq. 3.2.3)}$$

These values of output power were then used to perform a 4-corner calculation for $I_{\text{tot}}$, and are shown in tables 3.2.1 and 3.2.2 (bold lines mark the parts that will be used).

<table>
<thead>
<tr>
<th>VCSEL Part #</th>
<th>Total Current into VCSEL ($I_{\text{TOT(max)}}$) - [A]</th>
<th>Min $I_{\text{th}}$, Min $\eta$</th>
<th>Min $I_{\text{th}}$, Max $\eta$</th>
<th>Max $I_{\text{th}}$, Min $\eta$</th>
<th>Max $I_{\text{th}}$, Max $\eta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>HFE4391-521</td>
<td>3.671E-02, 8.143E-03, 4.071E-02, 1.214E-02</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HFE4391-541</td>
<td>2.600E-02, 7.250E-03, 3.000E-02, 1.250E-02</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HFE4384-522</td>
<td>1.817E-02, 4.833E-03, 2.267E-02, 9.333E-03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HFE4191-521</td>
<td>3.671E-02, 8.143E-03, 4.071E-02, 1.214E-02</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3.2.1 – VCSEL 4-corner Analysis for $I_{\text{tot}}$ with $P_{\text{out/max}} = 1\text{ mw}$.

<table>
<thead>
<tr>
<th>VCSEL Part #</th>
<th>Total Current into VCSEL ($I_{\text{TOT(min)}}$) - [A]</th>
<th>Min $I_{\text{th}}$, Min $\eta$</th>
<th>Min $I_{\text{th}}$, Max $\eta$</th>
<th>Max $I_{\text{th}}$, Min $\eta$</th>
<th>Max $I_{\text{th}}$, Max $\eta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>HFE4391-521</td>
<td>5.0072E-03, 1.8014E-03, 9.0072E-03, 5.8014E-03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HFE4391-541</td>
<td>3.8050E-03, 1.7013E-03, 7.8050E-03, 5.7013E-03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HFE4384-522</td>
<td>3.3700E-03, 1.8740E-03, 7.8700E-03, 6.3740E-03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HFE4191-521</td>
<td>5.0072E-03, 1.8014E-03, 9.0072E-03, 5.8014E-03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3.2.2 – VCSEL 4-corner Analysis for $I_{\text{tot}}$ with $P_{\text{out/min}} = 0.112\text{ mw}$.

Next we used equation 3.2.4 to find the modulation current for the VCSEL. We used combinations of values for the threshold and total currents of the VCSEL to evaluate the minimum and maximum modulation current.

$$I_{\text{mod}} = \frac{2}{3} (I_{\text{tot}} - I_{\text{th}}) \quad \text{(Eq. 3.2.4)}$$
This analysis was also done for the range of output power and the results are shown in tables 3.2.3 and 3.2.4.

<table>
<thead>
<tr>
<th>VCSEL Part #</th>
<th>Modulation Current - $I_{MOD}$ - [A] : $I_{MOD} = (2/3)*(I_{TOT}-I_{TH})$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$\text{Min } I_{TH}$, $\text{Min } \eta$</td>
</tr>
<tr>
<td>HFE4391-521</td>
<td>2.381E-02</td>
</tr>
<tr>
<td>HFE4391-541</td>
<td>1.667E-02</td>
</tr>
<tr>
<td>HFE4384-522</td>
<td>1.111E-02</td>
</tr>
<tr>
<td>HFE4191-521</td>
<td>2.381E-02</td>
</tr>
</tbody>
</table>

Table 3.2.3 – VCSEL 4-corner Analysis for $I_{mod}$ with $P_{out/max} = 1\text{mw}$.

<table>
<thead>
<tr>
<th>VCSEL Part #</th>
<th>Bias Current - $I_{BIAS}$ - [A] : $I_{BIAS} = I_{TOT}-I_{MOD}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$\text{Min } I_{TH}$, $\text{Min } \eta$</td>
</tr>
<tr>
<td>HFE4391-521</td>
<td>1.290E-02</td>
</tr>
<tr>
<td>HFE4391-541</td>
<td>9.333E-03</td>
</tr>
<tr>
<td>HFE4384-522</td>
<td>7.056E-03</td>
</tr>
<tr>
<td>HFE4191-521</td>
<td>1.290E-02</td>
</tr>
</tbody>
</table>

Table 3.2.4 – VCSEL 4-corner Analysis for $I_{mod}$ with $P_{out/min} = 0.112\text{mw}$.

The next step was to find the bias current, and this was done by relating $I_{tot}$ and $I_{mod}$, where $I_{bias}$ is their difference.

$$I_{bias} = I_{tot} - I_{mod} \quad \text{(Eq. 3.2.5)}$$

The values for the bias currents are shown in tables 3.2.5 and 3.2.6.
Table 3.2.6 – VCSEL 4-corner Analysis for $I_{\text{bias}}$ with $P_{\text{out/min}} = 0.112\text{mw}$. 

### VCSEL Part #

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Bias Current - $I_{\text{BIAS}}$ - [A]</th>
<th>$I_{\text{BIAS}}$ = $I_{\text{TOT}}-I_{\text{MOD}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min $I_{\text{TH}}$, Min $\eta$</td>
<td>Max $I_{\text{TH}}$, Min $\eta$, Max $I_{\text{TH}}$, Max $\eta$</td>
</tr>
<tr>
<td>HFE4391-521</td>
<td>2.336E-03</td>
<td>6.336E-03, 5.267E-03</td>
</tr>
<tr>
<td>HFE4391-541</td>
<td>1.935E-03</td>
<td>5.935E-03, 5.234E-03</td>
</tr>
<tr>
<td>HFE4384-522</td>
<td>2.123E-03</td>
<td>6.623E-03, 6.125E-03</td>
</tr>
<tr>
<td>HFE4191-521</td>
<td>2.336E-03</td>
<td>6.336E-03, 5.267E-03</td>
</tr>
</tbody>
</table>

3.3 – Photo-Detector Calculations

Our calculations for the PD began with estimating the current output from the diode into the transimpedance amplifier. Using the Responsivity parameter $\mathcal{R}$ (measured in A/w) specified in the Osifibercom and Hamamatsu data sheet [6,7], we found two values for the output current.

$$I_{\text{TIA}(\text{in})} = \mathcal{R} \cdot P_{\text{in(PD)}}$$  \hspace{1cm} (Eq. 3.3.1)

The PD data sheet also includes parameters such as the dark current of the diode and its capacitance. The dark current is the current generated by the diode when no light source is present. This current is normally measured in pA, and could therefore by neglected in the calculations, since the actual output current is in the $\mu$A range – several orders of magnitude larger. More important when choosing a PD was its capacitance. Since the MAXIM TIA data sheet specifies performance for a PD with capacitance 0.85 pF, such capacitance (or smaller) should be looked for in the PD to be used on the receiver [3,6,7].

3.4 – POT Calculations

3.4.1 – Calculating $R_{\text{bias}}$

To calculate the potentiometer values, it was necessary to first define the range of currents that flow through the VCSEL – the modulation current ($I_{\text{mod}}$) and the bias current ($I_{\text{bias}}$), and then calculate the range of resistances for each ($R_{\text{mod}}$ and $R_{\text{bias}}$). These values were shown in tables 3.2.3 through 3.2.6. To relate these currents to the desired resistances, the following circuit was used for calculations using Ohm’s law.

$^{1}$ It should be noted that when $I_{\text{mod}}$ is referred to during calculations, we are referring to the amplitude of that signal, as opposed to the peak-to-peak value, which would then be $I_{\text{mod-pp}} = 2 \cdot I_{\text{mod}}$. 

---

1. It should be noted that when $I_{\text{mod}}$ is referred to during calculations, we are referring to the amplitude of that signal, as opposed to the peak-to-peak value, which would then be $I_{\text{mod-pp}} = 2 \cdot I_{\text{mod}}$. 

14
Where $V_F$ is the forward bias of the photo-diode and is taken to be 2.2v for the PDs used. With the values of voltages and currents known, $R_{bias}$ could be calculated using equation 3.4.1.1.

$$R_{bias} = \frac{V_{CC} - V_F}{I_{bias}} \quad (Eq. \ 3.4.1.1)$$

Using the range of values found for $I_{bias}$ (shown in tables 3.2.5 and 3.2.6), the following values of $R_{bias}$ were calculated.

<table>
<thead>
<tr>
<th>VCSEL Part #</th>
<th>$R_{BIAS}$ : $R_{BIAS} = (V_{CC} - V_F)/I_{BIAS}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min $I_{th}$, Min $\eta$</td>
</tr>
<tr>
<td>HFE4391-521</td>
<td>216.97</td>
</tr>
<tr>
<td>HFE4391-541</td>
<td>300.00</td>
</tr>
<tr>
<td>HFE4384-522</td>
<td>396.85</td>
</tr>
<tr>
<td>HFE4191-521</td>
<td>216.97</td>
</tr>
</tbody>
</table>

Table 3.4.1.1 – $R_{bias}$ estimation using the previously calculated $I_{bias}$. 

Where the minimum and maximum values of the potentiometer $R_{\text{bias}}$ are 210 Ω and 1072.34 Ω. To accommodate these values, the range for $R_{\text{bias}}$ was chosen to be: $100 \, \Omega < R_{\text{bias}} < 1 \, k\Omega$.

3.4.2 – Calculating $R_{\text{mod}}$

To find $R_{\text{mod}}$ we performed an interpolation of the data given in the MAX3287 data sheet [5]. In the data sheet there is a table of values for $R_{\text{mod}}$ with a given $I_{\text{mod}}$. This table is shown below.

<table>
<thead>
<tr>
<th>TEMPCO (ppm/°C)</th>
<th>$I_{\text{MOD}} = 30$mA</th>
<th>$I_{\text{MOD}} = 15$mA</th>
<th>$I_{\text{MOD}} = 5$mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{MOD}}$ (kΩ)</td>
<td>$R_{\text{TC}}$ (kΩ)</td>
<td>$R_{\text{MOD}}$ (kΩ)</td>
<td>$R_{\text{TC}}$ (kΩ)</td>
</tr>
<tr>
<td>3500</td>
<td>26.7</td>
<td>1.69</td>
<td>53.6</td>
</tr>
<tr>
<td>3000</td>
<td>9.53</td>
<td>2.0</td>
<td>18.7</td>
</tr>
<tr>
<td>2500</td>
<td>5.76</td>
<td>2.49</td>
<td>11.3</td>
</tr>
<tr>
<td>2000</td>
<td>4.12</td>
<td>3.16</td>
<td>8.06</td>
</tr>
<tr>
<td>1500</td>
<td>3.24</td>
<td>4.32</td>
<td>6.19</td>
</tr>
<tr>
<td>1000</td>
<td>2.67</td>
<td>6.49</td>
<td>5.11</td>
</tr>
<tr>
<td>500</td>
<td>2.26</td>
<td>13.3</td>
<td>4.22</td>
</tr>
</tbody>
</table>

Table 3.4.2.1 – $R_{\text{mod}}$ values for different $I_{\text{mod}}$ values, taken from MAX3287 Data Sheet [MAX3287]

Using the above table, an interpolation graph was made in Microsoft Excel and an estimate formula to evaluate $R_{\text{mod}}$ was conceived. The Graph is shown in figure 3.4.2.1.
The relation between $R_{mod}$ and $I_{mod}$ is given in equation 3.4.2.1.

$$R_{mod} = 44.856 \cdot (I_{mod})^{-1.0712}$$  \hspace{1cm} (Eq. 3.4.2.1)

Using this relation and the values found for $I_{mod}$ (shown in tables 3.2.3 and 3.2.4), the range for $R_{mod}$ is tabulated in table 3.4.2.2.

<table>
<thead>
<tr>
<th>VCSEL Part #</th>
<th>$R_{mod}$ calculated using Linear Interpolation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min $I_{th}$, Min $\eta$</td>
</tr>
<tr>
<td>HFE4391-521</td>
<td>2458.36</td>
</tr>
<tr>
<td>HFE4391-541</td>
<td>3602.27</td>
</tr>
<tr>
<td>HFE4384-522</td>
<td>5561.67</td>
</tr>
<tr>
<td>HFE4191-521</td>
<td>2458.36</td>
</tr>
</tbody>
</table>

Table 3.4.2.2 – Interpolation for the values of $R_{mod}$.

The extreme values of $R_{mod}$ are 31184.72 $\Omega$ and 3602.27 $\Omega$. Therefore, the range for $R_{mod}$ was chosen to be $2 \, k\Omega < R_{mod} < 30 \, k\Omega$.

### 4 - Selection of Parts

Upon successful completion of the optical link budget, a final selection of parts and a tentative budget were made. The final selection was based on the four corner analysis done in the optical link budget which took care of the best and worse case scenarios. After careful inspection of the optical link budget two VCSEL’s (HFE4391-541 and HFE4384-522) manufactured by Honeywell International Inc [1,2]. Two photodiodes (FCI-125G-006HR-SC and S7912) manufactured by Osifibercom and Hamatsu were chosen [5,6].

The next step in selection of parts was to order the passive components. Three 1/8W resistors of 100$\Omega$, 115$\Omega$, 24.9$\Omega$ were selected. Two of these resistors were chosen because they were to be placed in series with the potentiometers such that the minimum resistance can be maintained. 0.01$\mu$F capacitors were also chosen for the various filter circuitries on the board. The above chosen resistors and capacitors were 0805 package [8]. 10nH ferrite beads available from Mouser electronics which would act as inductors were chosen as well [9]. The SMA and power connectors were a given project...
specification and hence no selection was necessary, only ordering. They were 145373 from Jameco Electronics and CP-002AHPJ-ND available at Digi-Key Electronics [11,8]. 2KΩ and 50KΩ ceramic single turn potentiometers were chosen, also available at Digi-Key [8].

Finally, the board layout was complete, and was to be ordered from Express PCB [12]. The layout was designed in such a way so that two designs were incorporated on one board so that two forms of designs were attempted - an aggressive layout on one side and a more conservative on the other.

5 - Financial Budget

After the final selection of parts a financial budget was made in order to ensure enough funds were available for a second run. A total of three hundred and fifty dollars were allotted to the group to successfully test and build a prototype of the transceiver board. Cost is as always a big issue in implementing any design and the case was the same here. Measures were taken to verify there was enough money at the end so that a final run was feasible in case the first design fails. In the initial ordering phase enough components were ordered such that both designs on the PCB board could be tested. Hamamatsu was kind enough to provide a free sample of their photo diode [6]. Honeywell also waived all shipping charges and hence these small savings could prove beneficial in saving money for the second run.

A complete and detailed look at the financial budget can be seen in Figure 5.1.

<table>
<thead>
<tr>
<th>Part#</th>
<th>Part Description</th>
<th>Vendor</th>
<th>Cost/piece</th>
<th>Quantity</th>
<th>Total Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>FCI-125G006RB-SC</td>
<td>Photo Diode</td>
<td>Coiltronics</td>
<td>$18.00</td>
<td>1</td>
<td>$18.00</td>
</tr>
<tr>
<td>57912</td>
<td>Photo Diode</td>
<td>Hamamatsu</td>
<td>$21.31</td>
<td>1</td>
<td>FREE</td>
</tr>
<tr>
<td>HFE409L-541</td>
<td>VCSEL</td>
<td>Honeywell</td>
<td>$10.50</td>
<td>1</td>
<td>$10.50</td>
</tr>
<tr>
<td>HFE4084-522</td>
<td>VCSEL</td>
<td>Honeywell</td>
<td>$17.75</td>
<td>1</td>
<td>$17.75</td>
</tr>
<tr>
<td>PCB Board</td>
<td>PCB Board</td>
<td>Express PCB</td>
<td>$62.00</td>
<td>1</td>
<td>$62.00</td>
</tr>
<tr>
<td>145373</td>
<td>SMA Connectors</td>
<td>Jameco</td>
<td>$6.96</td>
<td>4</td>
<td>$27.84</td>
</tr>
<tr>
<td>CP-002AHPJ-ND</td>
<td>Power Connectors</td>
<td>Digi-Ker</td>
<td>$0.61</td>
<td>2</td>
<td>$1.22</td>
</tr>
<tr>
<td>311-1000CT-ND</td>
<td>RES 100 OHM 1/4W 1% C0805 SMD</td>
<td>Digi-Ker</td>
<td>$0.10</td>
<td>5</td>
<td>$0.51</td>
</tr>
<tr>
<td>311-115CT-ND</td>
<td>RES 1/5 OHM 1/4W 1% C0805 SMD</td>
<td>Digi-Ker</td>
<td>$0.10</td>
<td>5</td>
<td>$0.51</td>
</tr>
<tr>
<td>311-24 90CT-ND</td>
<td>RES 2x 9 OHM 1/6W 1% C0805 SMD</td>
<td>Digi-Ker</td>
<td>$0.10</td>
<td>5</td>
<td>$0.51</td>
</tr>
<tr>
<td>399-115E 1 ND</td>
<td>CAP 10UF 60V CERAMIC XFR 305</td>
<td>Digi-Ker</td>
<td>$0.05</td>
<td>50</td>
<td>$2.50</td>
</tr>
<tr>
<td>CRPR505-MD</td>
<td>POT 50K 6MM CERN SC ST TOP</td>
<td>Digi-Ker</td>
<td>$0.64</td>
<td>5</td>
<td>$4.20</td>
</tr>
<tr>
<td>CT08002-MD</td>
<td>POT 2K6MM CERM SQ ST TOP</td>
<td>Digi-Ker</td>
<td>$0.99</td>
<td>5</td>
<td>$4.95</td>
</tr>
<tr>
<td>81-BLM1LH1025G</td>
<td>100H Ferrite Beads</td>
<td>Mouser Electronics</td>
<td>$0.36</td>
<td>20</td>
<td>$7.20</td>
</tr>
</tbody>
</table>

A complete and detailed look at the Financial Budget can be seen in Figure 5.1.
The financial budget gives a detailed look at the part numbers, vendors, part description, cost per piece and the quantities to be ordered. After reviewing the financial budget, the group decided $183.47 was enough for a second run if necessary and hence the parts were ordered from their respective vendors.

6. -Board Layout and Design

6.1 – Design Tools

The software package that was used to capture the schematic design for both the receiver and transceiver is ExpressSCH version 3.2.0. This software package is proprietary to the ExpressPCB Company and can be downloaded from the company’s website [12]. Though the use of ExpressSCH was not a required step in ordering boards from ExpressPCB, we decided it worthwhile to use this tool. By linking the schematic diagram with ExpressPCB’s layout software, one could highlight all pins on each net while routing the board. This feature was invaluable during the error checking phase of the design review. The following discussion of the schematic design is best partitioned into receiver and transmitter sections.

6.2 – Transceiver Schematic

6.2.1 – Receiver Schematic

The design for the receiver is shown below in Figure 6.2.1.1.

![Figure 6.2.1.1. Receiver Schematic](image)
The design for the receiver is composed primarily of the Hamamatsu S7912 photodiode, the MAXIM3266 transimpedance amplifier, and the MAXIM3264 limiting amplifier which are labeled in Figure 6.2.1.1. The idea for the schematic’s structure was derived from the application notes included in the data sheets for the Maxim IC’s which are provided in [3,4,5]. This same design without the photodiode was used on the test board discussed in Appendix A. Because the test board worked successfully, the only real variable of concern was the physical placement of the photodiode with respect to the transimpedance amplifier. This placement will be discussed in the following Layout section. In the two boxes are low-pass power supply filters designed to eliminate AC ripples on the supply lines [10]. Though the VCC symbol only refers to one physical power supply on the PCB board, a separate filter was dedicated to each IC. The values for the lumped elements in the filter were calculated based upon a cut-off frequency of 3 MHz, well below the gigahertz frequency of the signal lines. The design for the second order filter was based upon information contained within a Maxim application sheet regarding power supply filters which can be found in [10].

6.2.2 – Transmitter Schematic

The design for the transmitter schematic is provided below in Figure 6.2.2.1.

![Figure 6.3.1. Receiver Schematic](image)
The transmitter design is composed primarily of a MAXIM3287 laser driver chip and a Honeywell HFE4391-541 VCSEL [5]. The design for this circuit was obtained from the schematic diagram accompanying the MAXIM3287 evaluation board which is provided in [5]. Though the basic shape of this schematic was provided by Maxim, the resistor values of R1 and R4 had to be calculated based upon the performance specifications of the VCSEL used in the design. Because the proper functionality of the transmitter design relies heavily on these resistor values, they were implemented with potentiometers so that fine adjustments to the resistances can easily be made after the PCB is assembled. A detailed explanation of the calculations used to determine the values of R1 and R4 is provided in Section 3.4. As in the receiver schematic, the power supply filter is contained within the box. The VCC symbols in both the transmitter and receiver schematic refer to the same power supply. Furthermore, as will be apparent when the layout is discussed, both circuits share a common ground.

6.3 - Board Layout
6.3.1 – Design Tools

The software package that was used to layout the above schematic designs onto a PCB board was ExpressPCB version 3.2.0 [12]. This software was developed by Express PCB and can be obtained from the company’s website. Certainly, far superior layout software packages are available today. However, ExpressPCB was the vendor that offered to manufacture the fewest boards at the lowest price. The boards did lack a silkscreen and a solder mask. These features make assembling the board significantly easier but are, nonetheless, not imperative. Furthermore, the simplicity of the design did not warrant fancy routing software. The cost of the board is provided in Section 5.

The complete layout for one transceiver circuit is provided below in Figure 6.3.1.1.
When placing components and routing signals for this design, the three main design rules were followed.

1) All signal lengths were kept as short as possible to avoid transmission line effects. Specifically, if a signal trace is less than a tenth of a wavelength long, that trace should not behave as a transmission line. To be safe, this board was designed for the fifth harmonic, which is 2.5 GHz. Thus, every effort was made to keep traces under 4mm in length.

2) All differential pair signal were routed with equal trace lengths and in close proximity of one another. These precautions help to ensure that noise is common to both traces of the pair so that it can be better rejected.

3) All bends in the signal lines where made 45 degrees or less to prevent voltage reflections. All bends in power supply lines were made to be 90 degrees to block any AC ripple.

As with the schematic discussion, both the receiver and transmitter layout will be discussed separately.
6.3.2 – *Receiver Layout*

The receiver portion of the layout is marked with a dashed box in the top half of Figure 6.3.1.1. This layout is almost identical to the one used on the receiver test board discussed in Appendix A. A significant difference, however, is the photo diode, reference designator U5. The photo diode was purposely put to the side of the transimpedance amplifier in order to place it in close proximity to the VCSEL of the transmitter, reference designator U2. As a required specification for the transceiver design, the VCSEL and photo diode had to be no further apart than the Asante duplex module. The design in Figure 6.3.1.1 meets this specification.

One also notices that the receiver layout has been modified for use with a single power supply. Each Maxim chip is given one line from the power supply. Additionally, each power supply line has its own low-pass filter as indicated in Figure 6.3.1.1. The routing scheme for the power supply lines was somewhat of an educated attempt to satisfy the design specification of using only one single 5V power supply. No real precedence from previous semesters’ work existed for powering a receiver and transmitter with one supply.

In an attempt to satisfy design rule 1 mentioned above, the length of the design from connector to photo diode was shortened. Despite this effort, some traces did remain over 4mm in length. An example is the differential pair running from the SMA connectors J3 and J4 to the limiting amplifier, U4. In this particular situation, the length of these lines ran too long because of the bulky geometry of the SMA connectors. Similarly, the necessary placement of the photo diode caused the traces leading to its cathode and anode to run over the desired length. The 4mm length design goal was extremely conservative. Thus, traces that slightly miss this mark are still expected to work.

6.3.3 – *Transmitter Layout*

The receiver portion of the layout is marked with a dashed box in the bottom half of Figure 6.3.1.1. No part of the transmitter layout was borrowed from the previous work of others. The components were placed with the intent that the layout would fit easily when placed in parallel to the receiver design. Similar to the receiver power routing scheme, only one power line, equipped with a low-pass filter, was routed to the single
Maxim laser driver chip, reference designator U1. The transmitter design shared a common problem with its sensitive signals as did the receiver design. The differential pair routed from its SMA connectors to the laser driver chip, U2, are a bit longer than 4mm. Baring these traces, however, all other signal traces were within the proper length.

The most important network concerning the proper functionality of the transmitter board is the loop from the ground of resistor, R5, to the ground of the VCSEL, U2. It was crucial that both halves of the loop, from the ground of R5 to the laser driver chip and from the ground of the VCSEL to the laser driver chip, where both symmetrical and short in length to prevent unwanted feedback on the signal lines. From Figure 6.3.1.1, one can see that a strong effort was made to accomplish these goals.

6.4 – Design Overview

One can see from Figure 6.3.1.1 that the ground planes between the transmitter and receiver are split. In between these planes are two sets of an inductor, a 20 mil trace, and a 50 mil trace. The inductor is intended to act as an RF choke that would block any RF noise that might transverse the two planes [10]. However, it is not known whether or not the inductor is necessary or if the traces, which are cheaper to manufacture, will be sufficient. Thus, during the first assembly of the board the inductor will be placed. If the design works, the inductor will be removed and the board will be retested. Finally, the complete transmitter design in Figure 6.3.1.1 only takes up half of the PCB. A less aggressive design was placed on the other half of the board. This provides an alternative if the first design fails to work.

7 – Intermediate Conclusion & Future Plans (Dhairya)

The next step in the project is to solder the transceiver board early next week and perform several tests to ensure the reliability of the design. All of the VCSEL’s and Photodiodes have arrived, as well as the printed circuit board from ExpressPCB. The design’s passives have been shipped and are expected in the next couple of days. Once the passive components have arrived, the board will be soldered and ready for the testing phase.

In the upcoming weeks the task plan is divided into four major parts. First, the board must be put together. Second, an initial round of tests on the board will be
conducted. Thirdly, design improvisations will be made for the second run and the final testing phase.

Once the board is complete, a first attempt at testing the board will be conducted. In the groups’ opinion this is one of the most important tasks ahead and hence we should be accomplished comprehensively. There could be possibly two major outcomes at the end of the first testing phase - either the board will work and provide reasonable results or it will fail to meet the expectations, and further improvements are to be made.

Assuming the board does work, several tests will be performed on it to check its reliability. First, a basic loop-back test will be performed. This will ensure the basic functionality of the design. Second, baseline tests on the receiver and transmitter will be performed individually with the former being first. And last, sensitivity tests will be performed on the design as well. All these tests are necessary to find out how the design fairs with the given criteria, and how it performs compared to expectations. Once these tests are successfully carried out, another design review will be held. This time the aim of the review will be to optimize the design with emphasis on cost reduction, more aggressive layout such that design takes minimum area, more reliability, and better performance with attenuation. The cost of this design can be further reduced by using cheaper components such as unconnectorized photodiodes and cheaper VCSEL. The design layout has some room for improvement as well.

If the other possible outcome occurs, meaning that the design fails to meet our expectations, several debugging techniques will be utilized. These could include an attempt to trace the signal at each component. Other techniques will be used to try to detect the fault in the design, and may lead to “board surgery.” The optical link budget will also be reviewed again for the accuracy of the calculations and possibly a different selection of components will be made. In either scenario one more testing phase will be performed to improve out design.

In conclusion, it is the universal opinion of the group that the first run will turn out as successful. The plan is to complete the second round of testing (a 2nd run) within next three weeks and start working towards the final paper.

Since Gbps Ethernet has aspects in most areas of modern communication, understanding its concept and application to real world situations is crucial in an attempt to design it. Even though very few designs are flawless in reality, it is expected that this
particular project will be successful in its first run since it is based on past experience of others. If problems do arise, perhaps the most could be made from this project by facing the big picture of actual design and real life situations. These could later be learned from and conclusions could be drawn, not only for this field of electrical engineering, but to the engineering profession as a whole.
8 - References

VCSELs


MAXIM ICs Data Sheets


Photo Diodes


Passives

Ferrite Beads


Power Supply Filters


SMA Connectors

http://www.jameco.com/cgi-bin/ncommerce3/ExecMacro/Jameco/searchResult.d2w/report?sort=BKW&search=145373&Go.x=26&Go.y=10

PCB Board

http://www.expresspcb.com/

Course related Websites

http://www.ece.gatech.edu/academic/courses/ece4006/spring2003/G7/

http://www.ece.gatech.edu/academic/courses/ece4006/spring2003/

Miscellaneous

http://standards.ieee.org/
Appendix A – Soldering, Receiver Board and Attenuation Testing (Jed)

The appendix overviews the procedures taken to test the practice receiver board, and the attenuation testing that were performed on it later on.

As a first actual lab assignment, the group was to solder and test a practice board in order to familiarize with the lab equipment and PCB soldering. The unsoldered practice board and the soldered one are shown in Figures A.1 and A.2.

Figure A.1 – Unsoldered practice board.

Figure A.2 – Soldered practice board
Once the board was assembled, it was connected to the Tektronix GTS1250 GBIC Test System, which functions as the transmitting signal of choice. The board was also connected to the Tektronix TDS3054 Four Channel Color Digital Phosphor Oscilloscope, which gathers the data and presents the Eye waveforms. Figure A.3 shows 4 waveforms for different input signals.

![Figure A.3 – Waveforms appearing on the oscilloscope.](image)

Later on, using the TDS3054 oscilloscope, the data streams were tested once again on the test board using an attenuator. The attenuation tests were to reveal characteristics and limits of the circuit when accounting for line loss. Each data stream was tested over a wide range of dB loss.

The test setup was exactly as it was for initial board testing except with an added attenuator in series with the input data stream to the test board. Each signal was tested at dB losses ranging from 0 to 60 dB loss. Most signals responded well until the loss reached about 50 dB of attenuation. Once the loss was greater than this the signals became almost indiscernible. In order to produce good signal graphs the persistence of the oscilloscope was set to 10 micro-seconds verify.
The particular signal of interest was the PRBS7 (Pseudo Random Bit Stream). This signal actually improved when given a small amount of attenuation. This phenomenon shows that the circuit is overdriven with no attenuation, thus improves once attenuation is added. Figure A.4 shows the response to a PRBS7 setup at 40 dB as well as 50 dB.

![Figure A.4 – The PRBS7 Eye image for 40 dB and 50 dB.](image)

Clearly, the line loss is too great for the circuit to produce accurate results for any values around 50 dB and above. Data for attenuation above 50 dB was not taken because no signal pattern could be seen on the oscilloscope.

In conclusion of practice and attenuation tests, it was determined that the maximum workable circuit loss was between 40 and 50 dB. Any loss that is greater than this would not produce accurate test results. This information was taken into consideration while and designing the transceiver board.