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1 – Abstract

The field of modern communications has an ever increasing need for improved means of data transfer, with emphasis on high speed and high quality technologies. The goal of this project is to design, implement and test a Gigabit Ethernet optoelectronic link that will work at a frequency of 1.25 GHz, and perform well under attenuation. The project deals with the design of a transceiver board which transmits data at a Gbps (gigabits per second) rate. The essence of the design is to calculate the transmitting laser’s bias currents, and implement filtering circuits to avoid electronic noise on the component. Upon completion of the design, it is fabricated and soldered on a PCB board, and then tested for performance and accuracy, with and without attenuation. The Photo-Detector’s alignment tolerance is also estimated via measurements. Conclusions are drawn as to the significance of the results and the importance of the design project. The role of the technology in the real world and the implications of the design are also discussed, in an attempt to generalize the topic into a bigger picture, and draw conclusions beyond the scope that is presented.
Introduction

2.1 – General Background

Modern organizations depend upon their local-area networks (LANs) to provide connectivity for a growing number of complex, mission-critical desktop computing applications. As the volume of network traffic increases, however, the bandwidth offered by a typical 10 Mbps Ethernet LAN quickly becomes inadequate to maintain acceptable performance for a growing number of desktop/server computing environments. These traffic jams are fueling the need for higher-speed networks. The most appropriate solution is Gigabit Ethernet. Gigabit Ethernet provides 1 Gbps bandwidth for campus networks with the simplicity of Ethernet at lower cost than other technologies of comparable speed. It offers a natural upgrade path for current Ethernet installations, leveraging existing end stations, management tools and training. The simple migration and support offered by Ethernet, combined with the scalability and flexibility to handle new applications and data types, makes Gigabit Ethernet the strategic choice for high-speed, high-bandwidth networking. Gigabit Ethernet is an extension to the highly successful 10 Mbps and 100 Mbps IEEE 802.3 Ethernet standards. Offering a raw data bandwidth of 1000 Mbps, Gigabit Ethernet maintains full compatibility with the huge installed base of Ethernet nodes.

2.2 - The Gigabit Ethernet Standard – IEEE 802.3z

The key objectives of the 802.3z Gigabit Ethernet task force were to develop a Gigabit Ethernet standard that does the following:

- Allows half- and full-duplex operation at speeds of 1000 Mbps
- Uses the 802.3 Ethernet frame format
- Addresses backward compatibility with 10BASE-T and 100BASE-T technologies

There were three objectives for link distances: a multimode fiber-optic link with a maximum length of 500 meters; a single-mode fiber-optic link with a maximum length of 5 kilometers; and a copper based length of 25 meters.

The challenges associated with using lasers on multimode fiber have become more apparent as the operating speed has increased. In addition, the IEEE 802.3z task force was particularly attentive to the characteristics of the installed base of networking cabling, be it copper or fiber optic cabling. It was discovered that a jitter component caused by a phenomenon known as differential mode delay (DMD). With 1000BASE-LX transceivers over multimode fiber, external patch cords are used to mitigate DMD.
The initial applications for Gigabit Ethernet are for campuses or buildings requiring greater bandwidth between routers, switches, hubs, repeaters and servers. Examples include switch-to-router, switch-to-switch, switch-to-server and switch-to-switch connections.

2.3 – Design Project Overview

The primary goal of our group is to design and implement a functional Gigabit Ethernet and Eye Safety compliant optoelectronic transceiver. Once a working link has been built, the secondary goal is to optimize the link for error-free data transfer using the most affordable design. During the course of the project, the group members will follow a self-assigned task and time management plan. The design must be carried out on a $350 budget allowance provided by the Georgia Tech ECE department. A system level design topology is provided by the instructors and recommended as guidance for the system design. As an initial step, a receiver board is provided without optical photo detector circuitry. After the electrical-only receiver board is assembled and tested, the group must design photo detector circuitry to integrate with the provided receiver design. Finally, the group will design an optical transceiver circuit, which interfaces and combines the transmitter with the optical receiver on the same board.

Vertical-Cavity-Surface-Emitting Laser diodes (VCSELs) are an integral part of this project and feature in the Tx design. They are a relatively new class of semiconductor lasers that emit light perpendicularly from the wafer and are composed of layers of partially reflective mirrors which confine the light. For this project VCSELs will be assessed by divergence angle, threshold current, and slope efficiency. Photo detectors (PDs) form the beginning of the Rx module. They capture and convert the optical signal into an electrical one, maintaining the data present in the original stream. High responsivity, low capacitance and bigger receiver area are the critical characteristics required in a photodiode for a good optoelectronic link. The optical fibers used are multi-mode types, functioning at the 850 nm wavelength. As their name implies, multi-mode fibers propagate in more than one mode, the number of which depends on the core size and the numerical aperture (NA) of the fiber. The higher the previously mentioned parameters are, the easier it is to launch the light into the fiber, resulting in a reduced need for core-to-core alignment. The core size for the project fibers is 62.5 µm.
2.4 – Group Management

Group 7 consists of five individuals with varying strengths in optoelectronics and analog electronics. Listed below are the group members and their respective assignments in the design process.

<table>
<thead>
<tr>
<th>Tasks</th>
<th>Members Responsible</th>
</tr>
</thead>
<tbody>
<tr>
<td>Website Management</td>
<td>Shilo</td>
</tr>
<tr>
<td>Writing &amp; Editing</td>
<td>Shilo, Dhairya (Editing)</td>
</tr>
<tr>
<td></td>
<td>All (writing)</td>
</tr>
<tr>
<td>Purchasing / Ordering</td>
<td>Dhairya, Jed</td>
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<td>Soldering</td>
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<tr>
<td>Test &amp; Measurements</td>
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<td>Layout &amp; Design</td>
<td>Courtenay, Shilo</td>
</tr>
<tr>
<td>Coordination / Budget</td>
<td>Dhairya, Shilo</td>
</tr>
</tbody>
</table>

Table 2.1 - Division of Labor

In order to facilitate collaboration, a supporting website was created where all important data, files, links, presentations and papers are available [13]. Group meetings were held at least twice each week and strong group chemistry was present during the project. Progress was monitored constantly using a Gantt chart (Figure A20 in the appendix), and group leaders were assigned to keep track of tasks and assignments.

3 - Board Layout and Design

3.1 – Design Tools

The software package that was used to capture the schematic design for both the receiver and transceiver is ExpressSCH version 3.2.0. This software package is proprietary to the ExpressPCB company and can be downloaded from the company’s website [12]. Though the use of ExpressSCH was not a required step in ordering boards from ExpressPCB, it was found to be a worthwhile tool. By linking the schematic diagram with ExpressPCB’s layout software, one could highlight all pins on each net while routing the board. This feature was invaluable during the error-checking phase of the design review. The following discussion of the schematic design will be partitioned into receiver and transmitter sections.
3.2 – Transceiver Schematic

3.2.1 – Receiver Schematic

The design for the receiver is shown below in Figure 3.2.1.1.

![Receiver Schematic Diagram](image)

Figure 3.2.1.1 - Receiver Schematic

The design for the receiver is composed primarily of the Hamamatsu S7912 photodiode, the MAXIM3266 transimpedance amplifier, and the MAXIM3264 limiting amplifier, which are labeled in Figure 3.2.1.1. The idea for the schematic’s structure was obtained from the application notes included in the data sheets for the Maxim IC’s. These data sheets are provided in [3,4,5]. This same design without the photodiode was used on the test board shown in Appendix B. Because the test board worked successfully, the only real variable of concern was the physical placement of the photodiode with respect to the transimpedance amplifier. This placement will be discussed in the following Layout section. In the two boxes are low-pass power supply filters designed to eliminate AC ripples on the supply lines [10]. Though the VCC symbol only refers to one physical power supply on the PCB board, a separate filter was dedicated to each IC. The values for the lumped elements in the filter were calculated based upon a cut-off frequency of 3 MHz, well below the gigahertz frequency of the signal lines. The design for the second order filter was based upon information contained within a Maxim application sheet regarding power supply filters, which can be found in [10].
3.2.2 – Transmitter Schematic

The design for the transmitter schematic is provided below in Figure 3.2.2.1.

![Transmitter Schematic](image)

Figure 3.2.2.1. - Transmitter Schematic

The transmitter design is composed primarily of a MAXIM3287 laser driver chip and a Honeywell HFE4391-541 VCSEL [5]. The design for this circuit was obtained from the schematic diagram accompanying the MAXIM3287 evaluation board, which is provided in [5]. Though the basic shape of this schematic was provided by Maxim, the resistor values of R1 and R4 had to be calculated based upon the performance specifications of the VCSEL used in the design. Because the proper functionality of the transmitter design relies heavily on these resistor values, they were implemented with potentiometers so that fine adjustments to the resistances can easily be made after the PCB is assembled. A detailed explanation of the calculations used to determine the values of R1 and R4 is provided in Appendix A. As in the receiver schematic, the power supply filter is contained within the box. The VCC symbols in both the transmitter and receiver schematic refer to the same power supply. Furthermore, as will be apparent when the layout is discussed, both circuits share a common ground.

3.3 - Board Layout

3.3.1 – Design Tools

The software package that was used to layout the above schematic designs onto a PCB board was ExpressPCB version 3.2.0 [12]. This software was developed by Express PCB and can be obtained from the company’s website¹. Certainly, far superior layout software packages are available today. However, ExpressPCB was the vendor that offered to manufacture the fewest boards at the lowest price. The boards did lack a
silkscreen and a solder mask. These features make assembling the board significantly easier but are, nonetheless, not imperative. Furthermore, the simplicity of the design did not warrant fancy routing software. The cost of the board is provided in Section 7.

The complete layout for one transceiver circuit is provided below in Figure 3.3.1.1.

When placing components and routing signals for this design, these three main design rules were followed.

1) All signal lengths were kept as short as possible to avoid transmission line effects. Specifically, if a signal trace is less than a tenth of a wavelength long, that trace should not behave as a transmission line. To be safe, this board was designed for the fifth harmonic, which is 2.5 GHz. Thus, every effort was made to keep traces under 4mm in length.

2) All differential pair signal were routed with equal trace lengths and in close proximity of one another. These precautions help to ensure that noise is common to both traces of the pair so that it can be better rejected.

3) All bends in the signal lines where made 45 degrees or less to prevent voltage reflections. All bends in power supply lines were made to be 90 degrees to block any AC ripple.

As with the schematic discussion, both the receiver and transmitter layout will be discussed separately.
3.3.2 – Receiver Layout

The receiver portion of the layout is marked with a dashed box in the top half of Figure 3.3.1.1. This layout is almost identical to the one used on the receiver test board discussed in Appendix A. A significant difference, however, is the photo diode, reference designator U5. The photo diode was purposely put to the side of the transimpedance amplifier in order to place it in close proximity to the VCSEL of the transmitter, reference designator U2. As a required specification for the transceiver design, the VCSEL and photo diode had to be no further apart than the Asante duplex module. The design in Figure 3.3.1.1 meets this specification.

One also notices that the receiver layout has been modified for use with a single power supply. Each Maxim chip is given one line from the power supply. Additionally, each power supply line has its own low-pass filter as indicated in Figure 3.3.1.1. The routing scheme for the power supply lines was somewhat of an educated attempt to satisfy the design specification of using only one single 5V power supply. No real precedence from previous semesters’ work existed for powering a receiver and transmitter with one supply.

In an attempt to satisfy design rule 1 mentioned above, the length of the design from connector to photo diode was shortened. Despite this effort, some traces did remain over 4mm in length. An example is the differential pair running from the SMA connectors J3 and J4 to the limiting amplifier, U4. In this particular situation, the length of these lines ran too long because of the bulky geometry of the SMA connectors. Similarly, the necessary placement of the photo diode caused the traces leading to its cathode and anode to run over the desired length. The 4mm length design goal was extremely conservative. Thus, traces that slightly miss this mark are still expected to work.

3.3.3 – Transmitter Layout

The receiver portion of the layout is marked with a dashed box in the bottom half of Figure 3.3.1.1. No part of the transmitter layout was borrowed from the previous work of others. The components were placed with the intent that the layout would fit easily when placed in parallel to the receiver design. Similar to the receiver power routing scheme, only one power line, equipped with a low-pass filter, was routed to the single Maxim laser driver chip, reference designator U1. The transmitter design shared the same problem with its sensitive signals as did the receiver design. The differential pair
routed from its SMA connectors to the laser driver chip, U2, are a bit longer than 4mm. Baring these traces, however, all other signal traces were within the proper length.

The most important network concerning the proper functionality of the transmitter board is the loop from the ground of resistor, R5, to the ground of the VCSEL, U2. It was crucial that both halves of the loop, from the ground of R5 to the laser driver chip and from the ground of the VCSEL to the laser driver chip, where symmetrical and short in length to prevent unwanted feedback on the signal lines. From Figure 3.3.1.1, one can see that a strong effort was made to accomplish this goal.

3.4 – Design Overview

One can see from Figure 3.3.1.1 that the ground planes between the transmitter and receiver are split. In between these planes are two sets of an inductor, a 20 mil trace, and a 50 mil trace. The inductor is intended to act as an RF choke that would block any RF noise that might transverse the two planes [10]. However, it is not known whether or not the inductor is necessary or if the traces, which are cheaper to manufacture, will be sufficient. Thus, during the first assembly of the board the inductor will be placed. If the design works, the inductor will be removed and the board will be retested. Finally, the complete transmitter design in Figure 3.3.1.1 only takes up half of the PCB. A less aggressive design was placed on the other half of the board. This provides an alternative if the first design fails to work.

3.5 - Second Layout and Design

Upon initially testing the first PCB fabrication and assembly, it was found that both the schematic and board layout contained errors that prevented the transmitter from working correctly. Fortunately, these errors could be fixed by soldering external jumpers to the PCB. A detailed picture of the PCB with jumpers is provided in section 4. The eyes obtained from the testing of the mended PCB board, which are provided in Section 5, were very respectable, but were not perfect. Furthermore, the design failed to yield eyes at 10dB and 15dB of attenuation for some signals. The purpose of fabricating a second run was, therefore, twofold: 1) To fix the design such that the board did not require external jumpers; 2) To improve the layout such that signal integrity was increased; 3) To add to the layout for the purpose of increasing sensitivity.

3.5.1 - Fixing Board Errors

The first error discovered on the first board layout, Figure 3.3.1.1, was the presences of capacitor C3 between pin 2 of the MAXIM3287 laser driver chip and ground. Though this capacitor appears in MAXIM’s data sheets, last semester’s groups
discovered that the laser driver simply would not work with this capacitor present. The second board error found was a missing power supply hookup on pin 11 of the MAXIM3287 laser driver. This error was simply the result of a design oversight. The problem was easily fixed by adding both a trace from pin 11 to VCC and a bypass capacitor to accompany this trace. The second run PCB containing these corrections is shown below in Figure 3.5.5.1.

One can see that the capacitor C3 off pin 2 of the laser driver, U1, is no longer present. Instead, the capacitor was moved to the power supply trace to act as a bypass capacitor for the new power supply line to pin 11. There was some initial concern among the group that the power supply pin on the input side of the transmitter, pin2, and the power supply pins on the output side of the transmitter, pins 11 and 14, should not be connected to the VCC line in such close proximity as it is common practice to route input and output power lines separately. This routing scheme, however, didn’t pose any noticeable problems. These layout changes resulted in the successful operation of the transceiver.

3.5.2 - Improving Signal Integrity and Sensitivity

The most apparent addition to the Run 1 layout in Run 2 is the presence of a large ground plane on the component side of the PCB, which appears as large red patches in Figure 3.5.5.1. In placing this ground plain, a conscious effort was made to leave a 1mm gap between the plain and any trace on the PCB. Furthermore, in order to effectively
connect the new component side ground plain with the solder side ground plan, vias where dropped on the plain with spacing of at least 4mm. Historically, undesirable electromagnetic phenomena can occur when equally spaced arrays of the same component are placed on a PCB board. Thus, an attempt was made to drop the vias in a completely random fashion.

The intent of this ground plane was to help sink any electric field that might be radiating from traces and interfering with the signal paths. The group hoped that this effect might help clean up the appearance of the eyes obtained during testing. In addition, it was thought that cleaner signals might lead to better sensitivity results. However, when this board was tested, approximately the same results as those for Run 1 were obtained. These results were not too shocking since no group member had a firm scientific understanding of the electromagnetism present on the PCB board. The ground plane strategy was somewhat blindly attempted just because it appears on many of Maxim’s evaluation boards. Select test results and a picture of the fully populated Run 2 PCB board are provided in the appendix.

4 – Testing

4.1 – First Round

The preliminary round of testing involved baseline test for both the receiver and transmitter. This was done using the GDS as the signal generator feeding signals into the receiver or transmitter. The receiver or transmitter was then connected directly to the oscilloscope. Shown below in figure 4.1 is the baseline test setup for the receiver portion of the board.

![Figure 4.1 - Receiver Test Setup](image)
4.1.1 – Receiver/Transmitter Results

The receiver produced relatively good results with elements of jitter. Shown below in figure 4.1.1.1 are some of the pictures of the baseline receiver (Rx) testing. All of the baseline testing pictures can be found in the appendix. The jitter was attributed to weak signal strength from the GDS coupled with a cheap photo diode having low responsivity. The signal clarity also improved when pressure was put on the fiber coming out of the GDS indicating a weak connection. The transmitter failed to produce any satisfactory results in the first round of testing.

![Image](image1.png)

Figure 4.1.1.1 - Receiver Results with (a) K28.7 (b) PRBS7

4.1.2 – Troubleshooting

This resulted in debugging of the board by probing several traces to check power, ground and signal. After careful debugging, two primary errors were found. These were an unwanted capacitor connected to pin2 of the maxim laser driver and a floating Vcc pin on the same chip. The capacitor was shorted and a jumper was soldered to connect the floating pin to Vcc. A picture of the board after surgery can be seen in Figure 4.1.2.1.

![Image](image2.png)

Figure 4.1.2.1 - Board after surgery.

Also while probing and debugging a ferrite bead was burnt and hence had to be replaced. Now, the board was ready for a second round of testing. After the board surgery, the
transmitter began working and produced some results. Some of these results can be seen in Figure 4.1.2.2.

![Figure 4.1.2.2 - Initial Transmitter Results with (a) K28.7 (b) PRBS7](image)

After having a working receiver and transmitter design, loop-back test were performed and some results were obtained as seen in Figure 4.1.2.3.

![Figure 4.1.2.3 - Intial Loopback TxB Rx Results with (a)K28.7 (b) PRBS7](image)

When attenuation was added to the fiber, all tests failed. All initial result can be found in the appendix.

### 4.2 – Second Round

After the initial round of testing, the results were analyzed. Indifferent behavior was noticed in the K28.7 signal for the transmitter, and the PRBS signal was exhibiting noise for both Tx and RxTx tests. The possible problems could have been due to cross talk and laser not emitting enough power.

Aluminum foil as well as an old PCB were used to detect interference as well as cross talk. Since the foil and PCB had no effect on the signal, no crosstalk was suspected. The next step was to perform laser power analysis. The analysis of the laser
power was done by using a pre-calibrated photo diode. The equations and setup shown below in figure 4.2.1 were used to determine the output power of the laser. The $P_1$ measurement corresponds to the weak signal output in the Tx results. The $P_2$ calculation corresponds to the much improved clean signal shown in the Tx baseline results.

![Figure 4.2.1 – VCSEL Power Measurement](image)

$$P_{IN} = \frac{V_{MEASURED}}{320.5}$$  \hspace{1cm} (Eq. 4.2.1)

$$P_1 = \frac{8mV}{320.5} \approx 25\mu W$$  \hspace{1cm} (Eq. 4.2.2)

$$P_2 = \frac{289mV}{320.5} \approx 0.903mW$$  \hspace{1cm} (Eq. 4.2.3)

After tuning $R_{bias}$ and increasing the power to as shown above to 0.903mW, much better results were achieved. The improved results of transmitter can be seen in Figure 4.2.2.

![Figure 4.2.2 - Improved Transmitter Results with (a) K28.7 (b) PRBS7](image)

Loop-back tests were performed again and significant improvements in the waveforms were seen. Some of the eyes can be seen in the figure below.

![Figure 4.2.3 - Improved Loopback TxRx Results with (a) K28.7 (b) PRBS7](image)
4.3 – Attenuation Testing

After successfully performing the baseline and loop-back tests and achieving satisfactory results, attenuation testing was performed.

4.3.1 – Rx Attenuation

With a lot of jiggling of the fibers, the receiver finally produced satisfactory results with 5dB attenuation. These can be seen in Figure 4.3.1.1.

![Figure 4.3.1.1](image1)

Figure 4.3.1.1 - Rx Results with 5dB attenuation with (a) K28.7 (b) PRBS7

4.3.2 – Tx Attenuation

After having increased the power, the transmitter produced very good eyes with 5dB and 10dB attenuation. 15dB attenuation resulted in no satisfactory waveforms. These results can be seen in Figures 4.3.2.1 – 4.3.2.2.

![Figure 4.3.2.1](image2)

Figure 4.3.2.1 - Tx Results with attenuation with (a) K28.7 - 5dB (b)

![Figure 4.3.2.2](image3)

Figure 4.3.2.2 - Tx Results with attenuation with (a) K28.7 - 10dB (b) PRBS7 – 10dB.
4.3.3 – Loop-back Attenuation

Attenuation tests in the loop-back configuration were also attempted. Good eyes were obtained at 5dB attenuation. As the attenuation was increased, the eye deteriorated and clean waveforms were obtained only for selected signals. These results can be seen in Figure 4.3.3.1 – 4.3.3.3.

![Figure 4.3.3.1 – Loop-back Attenuation Results (a) K28.7 – 5dB (b) PRBS7 – 5dB](image1)

![Figure 4.3.3.2 – Loop-back Attenuation Results (b) D21.5 – 10dB (a) K28.7 – 10dB](image2)

![Figure 4.3.3.3 – Loop-back Attenuation Results (a) D21.5 – 15dB (b) K28.7 – 15dB](image3)
5 - Alignment Tolerance

After having completed baseline and loopback tests with the connectorized photo diode, the next step was to solder the unconnectorized photo diode and test for its alignment tolerance. The chosen unconnectorized photo diode was Hamamatsu’s S7912 [6]. After soldering the unconnectorized photo diode on the board, simple baseline test were performed to check if it was working. Successful eyes were obtained for all the signals and can be seen in Figures 5.1 – 5.2.

![Figure 5.1 - Eye results obtained with unconnectorized photo diode (a) D21.5 (b) K28.5](image1)

![Figure 5.2 - Eye results obtained with unconnectorized photo diode (a) K28.7 (b) PRBS7](image2)

After having achieved clear eyes for all signals, alignment tolerance testing was done to estimate the photo diode’s sensitivity and find out the actual aperture size. This was done by using a set of three vernier calipers in the x,y, and z direction. A setup of the alignment tolerance can be seen in Figure 5.3.
Before attempting the alignment tolerance testing, an initial reference point was found. This was a point where the best eye was achieved. This point was also the starting z axis point where the fiber was as close to the photo diode as possible. After having done that the fiber was kept at a constant value of y and z and moved to both extremes in the x-direction to find the extreme points in the x-axis scale. Similarly, points for the y-axis were also found. This gave a rough idea as to the shape of the aperture, and as expected from theory it was somewhat circular. Four other points on the outskirts of the circumference in all the four quadrants were taken to give the aperture shape more definition. The fiber was moved in the z direction away from the photo diode to see up to what point an acceptable eye was achieved. It was found that with the fiber at a distance of 123µm above the photo diode, an acceptable eye was still visible and beyond that no eye was seen. Another set of points on the circumference of the aperture were taken with the fiber set to 61.5µm above the photo diode, halfway between the extreme points in the z-direction. These coordinates were recorded as seen in Figure 5.4.

After recording the data, a 3D model of the aperture area and sensitivity was made using AutoCAD. These can be seen in Figure 5.5. As expected, the diameter of the aperture decreased as the fiber was moved upwards in the z-direction. This is because the
signal got weaker as the fiber moved way from the photo diode. This can be clearly seen from the 3-D models as they exhibit a conical reduction in sensitivity with the tip of the cone being only one point where eye was seen. The diameter of the base was largest as the fiber was closest to the photo diode. This was found to be 47µm compared to 100µm given in the data sheet [6].

![Figure 5.5 - 3D Models representing the aperture size and sensitivity of photo diode](image)

The 3D model also shows that the shape of the base is not completely circular, it is more of an ellipse and also there is a slight bulge at one corner. These discrepancies are due to the fiber being at a slight angle with the photo diode. The deviation in the diameter of the aperture size is also because it is very hard to obtain direct alignment with the aperture based on human vision.

6 - Financial Budget and BOM

6.1 – The Financial Budget

After the final selection of parts a financial budget was made in order to ensure keep a detailed track of all the expenses so that all the purchases were made within the budget. A total of three hundred and fifty dollars were allotted to the group to successfully test and build a prototype of the transceiver board. Cost is as always a big issue in implementing any design and the case was the same here. Right from the start measures were taken to verify there was enough money at the end so that a final run was feasible in case the first design fails. In the initial ordering phase enough components were ordered such that both designs on the PCB board could be tested. Hamamatsu was kind enough to provide a free sample of their photo diode [6]. Honeywell also waived all shipping charges and hence these small savings could prove beneficial in saving money for the second run. As it turned out the first design worked very well but to improve
results further a second run was done. This led to some changes to the financial budget as some more parts were purchased.

A complete and detailed look at the financial budget can be seen in Figure 6.1.

![Financial Budget Table](image)

**6.2 - Bill of Materials**

This transceiver board was a prototype of something that could possibly be manufactured commercially in bulk and therefore, it is important to realize how much each board would cost if it was manufactured in bulk. After contacting all the vendors of all the parts bulk prices were found and tabulated as bill of materials, $69.80, can seen in Figure 6.2.

![Bill Of Materials Table](image)
7 - Conclusions

Gigabit Ethernet and related technologies have had an extremely important impact on communications in the past decade. It is almost impossible to imagine society without the contributions made by advances such as this one or similar to it. Covering a scope that ranges from web surfing by the common user and up to state of the art communications in the military, this technology is found throughout. The goal of this project was to design, implement and test a Gigabit Ethernet optoelectronic link. As was previously shown, these three goals were successfully met.

The project began with the design of an optoelectronic link, consisting of a transmitter and a receiver sides. Each of these was tested successfully as a stand alone using an outside source which functioned as a complementary Tx/Rx, and later the entire circuit was analyzed in the loopback or transceiver mode, in which the transmitter was feeding the receiver. After the board was constructed, several design flaws were discovered and corrected. Some board surgery was necessary, but eventually the circuit worked as intended, if not better. Successful loopback and receiver/transmitter tests were performed, in attenuated and un-attenuated modes. Loopback attenuation analysis yielded excellent results for 5 dB on all 4 signals, good results for 10 dB on 2 of the signals and somewhat fair at 15 dB on the same two. The transmitter testing also produced excellent results for 5 dB and 10 dB attenuation and the receiver produced good eyes for 5 dB. The good results obtained could be attributed to the successful implementation of the design. The optical link budget specified an eye-safe VCSEL power output of 1 mW [14], and indeed the laser diode’s output power was measured to be about 0.9 mW. This explains why the transmitter testing went very well. However, since the connectorized PD used had somewhat of a low responsivity ($\mathcal{R}=0.36$ A/W) [7], the results obtained in the Rx tests did not yield too good of a sensitivity, and the eye was lost for attenuation larger than 5 dB. It is worth mentioning that when the connectorized PD was replaced with the un-connectorized one ($\mathcal{R}=0.47$ A/W) [6], a better looking eye could be seen on the scope. The loopback tests were also successful since the relatively good power output of the VCSEL compensated for the PD’s low responsivity, and produced good eye diagrams, as was shown in section 4.3.

In addition to the attenuation tests, the alignment tolerance of the un-connectorized PD was measured in section 5. This was done to observe how the PD fairs as the distance between it and the optical fiber is varied, or put in different alignment
compared to its higher responsivity region. It was observed that the waveform on the scope was steadily decreasing as a function of the distance of the fiber from the PD – as expected. Also, the PD’s tolerance appeared as a conic shape in the 3D space.

In contrary to competing designs, this board did not exhibit cross-talk effects, in which parallel lines induce phantom signals on the actual receiving unit. After discussion, it was speculated that this advantage was due to the specific board layout, in which the PD is aligned sideways with the TIA. It is also possible that this noise reduction is the effect of the excellent power supply filters, which contained a parallel combination of 10µF and 0.1µF capacitors, and therefore exhibit outstanding low-pass characteristics. These led to the design of the 2\textsuperscript{nd} board.

In the second layout, the board surgeries done in run 1 were replaced by ‘concrete’ links on the fabricated board. The layout was in a sense identical to run 1, with the only difference being the inclusion of a ground plain on the surface of the board. This was done in an attempt to reduce EM interferences and noise. As shown previously, the second run was not as successful as the first. Possible causes could be the added ground plain, the lack of ‘surgery wires’ which may have helped in reducing EMI by acting as inductors, or the weariness of the VCSEL and PD which were soldered and re-soldered over and again in an attempt to stick to the same working parts in both boards.

Overall, this project was labeled as very successful by all members of the design group. Excellent signals were obtained from the board – even under heavy attenuation (up to 10 and some 15 dB). No cross-talk was seen in the resulting waveforms. Since other competing designs did not exhibit similar properties, and most of the other groups experienced heavy cross-talk and unsuccessful attenuation results a week before the due date, it was deemed that this specific design was fortunate enough to meet all the design criteria set forth in the beginning of the term. Furthermore, the cost of the unit turned out to be relatively low, and the budget was handled very well such that there was more than enough money left after the first run. Even though the 1\textsuperscript{st} run was very successful and provided all the results necessary for successful conclusion of the project, it was decided by the group to proceed with the layout and fabrication of the 2\textsuperscript{nd} run, which was then tested and unfortunately proved less glorious than its predecessor.

The importance of this project is quite significant. Even though this actual design will probably never win any awards or even go to production, it served as an excellent learning tool to those senior students who are about to face engineering outside the classroom – ever so known as “The REAL WORLD.” The structure of the course was
designed to simulate actual working environment, in which there are design requirements, due dates, progress reports and several groups who are developing the same product in parallel, each striving to produce the best results. More than teaching about Gbps design, this course helped in sampling the actual engineering practice and profession. It was agreed by the group members that since not many undergraduate classes offer the opportunity to experience real world scenarios, the senior design project should be considered as an excellent opportunity rather than another class in which the overall goal was to just ‘make the grade.’ This was extremely present in the excellent group dynamics and chemistry, and to an outsider who might have attended a group meeting it would have been obvious that the group members were present because they wanted to be there and make the most of this project.

In conclusion, this project served as a learning tool more than everything else that was accomplished through it. And indeed a lot was accomplished. It is a common feeling among the members of Group 7 that we now have had a small taste of actual engineering, and so going out to the job market might not be too much of a shock. Gigabit Ethernet also served as a window to analog and high frequency practice. The scope of this course and the design project related to it goes beyond the conventional undergraduate classes by bringing the real world into the classroom. It taught how to design, implement, follow a project schedule and deal with problems in the form of errors and debugging, how to manage a budget - and manage it well. It taught responsibility, discipline and above all – how to work and function well within a group. Even though this class does not teach a lot of material and theory, it is still regarded as one of the most valuable and important classes the school of ECE has to offer. It is fairly obvious to see why.
8 - References

VCSELs


MAXIM ICs Data Sheets


Photo Diodes


Passives


Ferrite Beads


Power Supply Filters

SMA Connectors


PCB Board


Course related Websites


Miscellaneous

Appendix A - Optical Link Budget

A.1 – General Idea

The optical link budget is meant to estimate the ranges of bias and modulation currents to the MAX3287 laser driver. The driver will then supply the chosen VCSEL with a total amount of current ($I_{\text{tot}}$) which will meet the threshold demand of the laser diode and cause it to lase constant optical power output ($P_{\text{out max}}$ or for simplicity $P_{\text{out}}$) that meets the Eye Safe criteria [eye safe]. This power will then propagate through the optical fiber while suffering losses of -7.5 dB. When the signal reaches the photo-detector, the diode outputs a current ($I_{\text{TIA (in)}}$) which is then the input to the MAX3266 TIA. The transimpedance amplifier converts the current into a differential output voltage ($V_{\text{LA (in)}}$), and the MAX3264 limiting amplifier ‘translates’ this voltage into a digital signal [3]. Figure A.1.1 demonstrates the idea using a block diagram.

$$I_{\text{tot}} = \frac{P_{\text{out}}}{\eta} + I_{\text{th}} \quad \text{(Eq. A.2.1)}$$

Since the design of the transmitter deals with worst possible scenarios, the total current for 4 combinations of slope efficiency and threshold current was calculated based on the
minimum and maximum values in the data sheets:
\[
\left\{ \frac{\eta_{\text{min}}}{I_{\text{th}(\text{min})}}, \frac{\eta_{\text{max}}}{I_{\text{th}(\text{max})}}, \frac{\eta_{\text{min}}}{I_{\text{th}(\text{max})}}, \frac{\eta_{\text{max}}}{I_{\text{th}(\text{min})}} \right\}
\]

The latter two being the worst possible combination of these variables. Then, the output power at the end of the optical fiber was found, which is equal to the power input to the photo-detector (\(P_{\text{in}}(\text{PD})\)). Using the value of -7.5 dB for attenuation in the fiber, we used equation 3.2.2 to find \(P_{\text{in}}(\text{PD})\):

\[
P_{\text{in}}(\text{PD}) = P_{\text{out}} \cdot 10^{-\alpha/10} = P_{\text{out}} \cdot 10^{-0.75} = 0.1778 \cdot P_{\text{out}} \quad \text{(Eq. A.2.2)}
\]

Where \(\alpha\) is the attenuation in the fiber and \(P_{\text{out}}\) is the Eye Safe laser output power (taken as 1 mw). The above equation demonstrates that the fiber attenuates about 82% of the input power, and the power into the photo-detector evaluates to \(P_{\text{in}}(\text{PD}) = 0.1778\) mw. The range of \(I_{\text{tot}}\) varies according to the biasing of the VCSEL about the active region. This is shown in Figure A.2.1.

![Figure A.2.1 – VCSEL output power vs. input current curve](image)

It can be seen that the total current is ranged between a maximum and minimum values, which then correspond to max, and min values for the VCSEL output power. Since the maximum output power (\(P_{\text{out}}/\text{max}\)) was determined to be 1mw, we had to define the minimum output power. This was done using the “extinction ratio” (denoted ‘ER’) given in the IEEE 802.3z, and its value is about 9.5 dB (different values, from 9 to 10 dB are used to be on the safe side). This ratio relates the minimum and maximum output powers from the VCSEL [15]. Using equation A.2.3 we found the value of \(P_{\text{out}}/\text{min} = 0.1122\) mw.
These values of output power were then used to perform a 4-corner calculation for $I_{tot}$, and are shown in tables A.2.1 and A.2.2 (bold lines mark the parts that will be used).

Next we used equation A.2.4 to find the modulation current for the VCSEL. We used combinations of values for the threshold and total currents of the VCSEL to evaluate the minimum and maximum modulation currents, using the power outputs obtained through the extinction ration of equation A.2.3.

$$I_{mod} = \frac{2}{3}(I_{tot} - I_{th}) \quad \text{(Eq. A.2.4)}$$

This analysis was also done for the range of output power and the results are shown in tables A.2.3 and A.2.4.
The next step was to find the bias current, and this was done by relating $I_{\text{tot}}$ and $I_{\text{mod}}$,
where $I_{\text{bias}}$ is their difference.

$$I_{\text{bias}} = I_{\text{tot}} - I_{\text{mod}} \quad \text{(Eq. A.2.5)}$$

The values for the bias currents are shown in tables A.2.5 and A.2.6.
A.3 – Photo-Detector Calculations

Our calculations for the PD began with estimating the current output from the diode into the transimpedance amplifier. Using the Responsivity parameter $\mathcal{R}$ (measured in A/w) specified in the Osifibercom and Hamamatsu data sheet [6,7], we found two values for the output current.

$$I_{\text{TIA(in)}} = \mathcal{R} \cdot P_{\text{in(PD)}}$$  \hspace{1cm} (Eq. A.3.1)

The PD data sheet also includes parameters such as the dark current of the diode and its capacitance. The dark current is the current generated by the diode when no light source is present. This current is normally measured in pA, and could therefore by neglected in the calculations, since the actual output current is in the μA range – several orders of magnitude larger. More important when choosing a PD was its capacitance. Since the MAXIM TIA data sheet specifies performance for a PD with capacitance 0.85 pF, such capacitance (or smaller) should be looked for in the PD to be used on the receiver [3,6,7].

A.4 – POT Calculations

A.4.1 – Calculating $R_{\text{bias}}$

To calculate the potentiometer values, it was necessary to first define the range of currents that flow through the VCSEL – the modulation current ($I_{\text{mod}}$) and the bias current ($I_{\text{bias}}$), and then calculate the range of resistances for each ($R_{\text{mod}}$ and $R_{\text{bias}}$). These values were shown in tables A.2.3 through A.2.6. To relate these currents to the desired resistances, the following circuit was used for calculations using Ohm’s law.

---

$^1$ It should be noted that when $I_{\text{mod}}$ is referred to during calculations, we are referring to the amplitude of that signal, as opposed to the peak-to-peak value, which would then be $I_{\text{mod-pp}} = 2 \cdot I_{\text{mod}}$. 

---

Table A.2.6 – VCSEL 4-corner Analysis for $I_{\text{bias}}$ with $P_{\text{out(max)}} = 0.112\text{mw}$.
Where $V_F$ is the forward bias of the photo-diode and is taken to be 2.2v for the PDs used. With the values of voltages and currents known, $R_{bias}$ could be calculated using equation A.4.1.1.

$$R_{bias} = \frac{V_{CC} - V_F}{I_{bias}}$$

(Eq. A.4.1.1)

Using the range of values found for $I_{bias}$ (shown in tables A.2.5 and A.2.6), the following values of $R_{bias}$ were calculated.

<table>
<thead>
<tr>
<th>VCSEL Part #</th>
<th>$R_{bias}$ : $R_{bias} = (V_{CC} - V_F)/I_{bias}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min $I_{TH}$, Min $\eta$</td>
</tr>
<tr>
<td>HFE4391-521</td>
<td>216.97</td>
</tr>
<tr>
<td>HFE4391-541</td>
<td>380.00</td>
</tr>
<tr>
<td>HFE4304-522</td>
<td>386.85</td>
</tr>
<tr>
<td>HFE4191-521</td>
<td>216.97</td>
</tr>
</tbody>
</table>

Table A.4.1.1 – $R_{bias}$ estimation using the previously calculated $I_{bias}$.
Where the minimum and maximum values of the potentiometer \( R_{\text{bias}} \) are 210 \( \Omega \) and 1072.34 \( \Omega \). To accommodate these values, the range for \( R_{\text{bias}} \) was chosen to be:
\[
100 \Omega < R_{\text{bias}} < 1 \text{k}\Omega.
\]

**A.4.2 – Calculating \( R_{\text{mod}} \)**

To find \( R_{\text{mod}} \) we performed an interpolation of the data given in the MAX3287 data sheet [5]. In the data sheet there is a table of values for \( R_{\text{mod}} \) with a given \( I_{\text{mod}} \). This table is shown below.

<table>
<thead>
<tr>
<th>TEMPCO (ppm/°C)</th>
<th>( I_{\text{MOD}} = 30\text{mA} )</th>
<th>( I_{\text{MOD}} = 15\text{mA} )</th>
<th>( I_{\text{MOD}} = 5\text{mA} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( R_{\text{MOD}} ) (k( \Omega ))</td>
<td>( R_{\text{TC}} ) (k( \Omega ))</td>
<td>( R_{\text{MOD}} ) (k( \Omega ))</td>
</tr>
<tr>
<td>3500</td>
<td>26.7</td>
<td>1.69</td>
<td>53.6</td>
</tr>
<tr>
<td>3000</td>
<td>9.53</td>
<td>2.0</td>
<td>18.7</td>
</tr>
<tr>
<td>2500</td>
<td>5.76</td>
<td>2.49</td>
<td>11.3</td>
</tr>
<tr>
<td>2000</td>
<td>4.12</td>
<td>3.16</td>
<td>8.06</td>
</tr>
<tr>
<td>1500</td>
<td>3.24</td>
<td>4.32</td>
<td>6.19</td>
</tr>
<tr>
<td>1000</td>
<td>2.67</td>
<td>6.49</td>
<td>5.11</td>
</tr>
<tr>
<td>500</td>
<td>2.26</td>
<td>13.3</td>
<td>4.22</td>
</tr>
</tbody>
</table>

*Table A.4.2.1 – \( R_{\text{mod}} \) values for different \( I_{\text{mod}} \) values, taken from MAX3287 Data Sheet [MAX3287]*

Using the above table, an interpolation graph was made in Microsoft Excel and an estimate formula to evaluate \( R_{\text{mod}} \) was conceived. The Graph is shown in figure A.4.2.1.

The relation between \( R_{\text{mod}} \) and \( I_{\text{mod}} \) is given in equation A.4.2.1.
\[ R_{\text{mod}} = 44.856 \cdot (I_{\text{mod}})^{-1.0712} \]  
(Eq. A.4.2.1)

Using this relation and the values found for \( I_{\text{mod}} \) (shown in tables A.2.3 and A.2.4), the range for \( R_{\text{mod}} \) is tabulated in table A.4.2.2.

<table>
<thead>
<tr>
<th>VCSEL Part #</th>
<th>( R_{\text{MOD calculated using Linear Interpolation}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min ( I_{\text{TR}} ), Min ( \eta )</td>
</tr>
<tr>
<td>HFE4391-421</td>
<td>2458.36</td>
</tr>
<tr>
<td>HFE4391-441</td>
<td>3602.27</td>
</tr>
<tr>
<td>HFE4384-427</td>
<td>5661.87</td>
</tr>
<tr>
<td>HFE4191-424</td>
<td>2458.36</td>
</tr>
</tbody>
</table>

Table A.4.2.2 – Interpolation for the values of \( R_{\text{mod}} \).

The extreme values of \( R_{\text{mod}} \) are 31184.72 \( \Omega \) and 3602.27 \( \Omega \). Therefore, the range for \( R_{\text{mod}} \) was chosen to be \( 2 \, k\Omega < R_{\text{mod}} < 30 \, k\Omega \).
Appendix B – Figures and Waveforms

Figure B1 - Test data of Tx before VCSEL power increase.

Figure B2 - Loopback test data before VCSEL power increase.
Figure B3 - Test data of loop back before VCSEL power increase (continued).

Figure B4 - Tx test data after VCSEL power increase.
Figure B5 - Test data of Tx before with 5dB attenuation.

Figure B6 - Test data of Tx with 10dB attenuation.
Figure B7 - Test data of Tx before 10dB attenuation (continued).

Figure B8 - Unconnectorized photo diode Rx data
Figure B9 - Test data of loop back with 0 dB attenuation.

Figure B10 - Test data of loop back with 5 dB attenuation.
Figure B11 - Test data of loop back with 5 dB attenuation (continued).

Figure B12 - Test data of loop back with 10 dB attenuation.

Figure B13 - Test data of loop back with 15 dB attenuation.
Figure B14 - Rx Baseline test results (GDSIII source, connectorized PD).

Figure B15 - Run 2 Rx baseline testing.
Figure B16 - Run 2 Rx baseline testing (continued).

Figure B17 - Run 2 Tx baseline testing data
Figure B18 - Run 2 loop back data test results.

Figure B19 - The 2nd Run Board
Figure B20 – Group 7 Gantt chart