Oscillation Control in CMOS Phase-Locked Loops

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Oscillation Control in CMOS Phase-Locked Loops

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This dissertation is dedicated to

the Samurai Professor

John Uyemura

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SUMMARY

Recent advances in voltage-controlled oscillator (VCO) design and the trend of CMOS processing indicate that the oscillator control is quickly becoming one of the forefront problems in high-frequency and low-phase-noise phase-locked loop (PLL) design. This control centric study explores the limitations and challenges in high-performance analog charge-pump PLLs when they are extended to multiple gigahertz applications.

Several problems with performance enhancement and precise oscillator control using analog circuits in low-voltage submicron CMOS processes, coupled with the fact that analog (or semi-digital) oscillators having various advantages over their digitally controlled counterparts, prompted the proposal of the digitally-controlled phase-locked loop. This research, then, investigates a class of otherwise analog PLLs that use a digital control path for driving a current-controlled oscillator. For this purpose, a novel method for control digitization is described where trains of pulses code the phase/frequency comparison information rather than the duration of the pulses: Pulse-Stream Coded Phase-Locked Loop (psc-PLL).

This work addresses issues significant to the design of future PLLs through a comparative study of the proposed digital control path topology and improved cutting-edge charge-pump PLLs.

CHAPTER I

INTRODUCTION

1.1 Motivation

Recent advances in applications of radio-frequency (RF) data communication, the rapid increase in microprocessor operating frequencies, and the possibility of high-frequency data storage have led to an exponential expansion of data traffic volume. This exponential growth has raised the demand for and the expectations of even higher data rates.

All modern communication systems (datacom, wireless, telecom) require a stable periodic signal to provide a timing basis for synchronizing, aligning the sampling clock, suppressing the clock skew, or synthesizing frequencies. Phase locking, studied for more than half a century, is the principal technique to provide timing solutions. An incomplete list of responsibilities realized by phase-locked loops (PLL) includes carrier recovery, clock recovery, phase modulation, phase/frequency demodulation, clock synchronization, frequency synthesis, duty cycle correction, and jitter reduction.

A PLL is a circuit that synchronizes an oscillator's output signal with a reference or input signal in both frequency and phase. The most fundamental block diagram of a PLL is shown in Figure 1 [1]. A PLL differs from other feedback systems as it operates on phase deviations rather than signal amplitudes. As the variable of interest changes dimension throughout the loop, the PLL's correct operation depends on the presence of

two nonlinear devices, namely the phase detector and the voltage-controlled oscillator (VCO). While the basic PLL nearly remained the same since its invention in 1930s, monolithically integrating PLLs has become an active area of research in recent years [2].

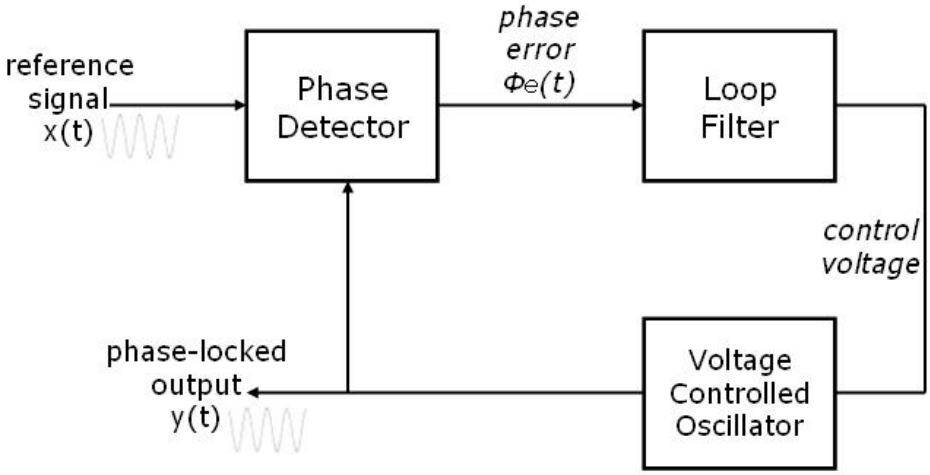


Figure 1: A general PLL block diagram

Today, a great concern for the integration of high-frequency systems are the problems associated with the synchronization difficulties. The implementation limitations on a fully integrated, low power, and high performance PLL significantly affect the overall system performance.

Although gigahertz (GHz) data rate integrated circuits have conventionally been implemented in gallium arsenide (GaAs) metal-semiconductor-field-effect-transistor (MESFET), silicon (Si) bipolar processes, or silicon germanium bipolar complementary metal-oxide semiconductor (BiCMOS); the submicron CMOS technology is an attractive option for meeting the demands of a growing market due to its large scale of integration and lower cost production [3]. As CMOS transistors scale down in size, their performance has improved significantly. Consequently, initial efforts on the

development of CMOS circuits at the multi-GHz frequency range have shown very promising results [4]. As integration scale improves, faster and smaller CMOS transistors can be packed into smaller die areas. The steady decrease in the gate length used to achieve gigahertz operating-frequencies has reduced the power supply voltage dramatically for reliable operation as shown in Table 1 [5].

Table 1: Technology development

YEAR	**1995**	**2001**	**2004**	**2007**	**2010**	**2013**	**2016**
Technology node (μm)	0.35	0.13	0.09	0.065	0.045	0.032	0.022
Power supply voltage (V)	3.3	1.1	0.9	0.8	0.7	0.6	0.5
Operating frequency (GHz)	0.3	1.684	4.171	9.289	15.079	22.480	39.683
Number of transistors (millions)	5	193	553	1106	2212	4424	8848

A major challenge in PLL design is to meet the demands of a new technology trend, which requires higher data rates while imposing new constraints on the PLL parameters. Analog circuit design is more complex in a submicron process, especially for circuits that require low input power. In addition to this, the allowable absolute timing uncertainty (clock jitter) for a given clock-skew tolerance decreases with increasing clock frequencies. Furthermore, a higher degree of integration results in substantial digital-switching noise that can be coupled through the power supply network and the substrate into noise-sensitive analog circuits. It is therefore clear that a poorly performing PLL can be system bottleneck in the current and coming communication/synchronous computation systems, given that a PLL is traditionally comprised of mostly analog blocks.

The challenges in PLL implementation are determined by technology trends and the application (operating frequency, tuning range, maximum allowable jitter, etc.). For monolithic implementations, the VCO has been the primary source of timing jitter when compared to the other loop components [6-9]. Besides, recent advances in VCO design and the trend of the CMOS processing indicate that the oscillator control is quickly becoming one of the forefront problems in digital system design [10, 11]. PLLs, in this work, are analyzed at this level of abstraction. However, the interested reader can also find more about the state of the art oscillator design within this work.

The challenges found in the design and implementation of high-frequency low-noise CMOS phase-locked loops are the primary motivation of this research.

1.2 Thesis Organization

In this work, the problem of precise oscillation control in CMOS phase-locked loops is addressed. In Chapter II, the basics of PLL operation is presented in a unique control centric flow; the existing PLL types are classified in this framework. The PLL subblocks are analyzed next. The comparative study of various architectures leads to the detailed analysis of the high-performance charge-pump PLLs (CPPLL). Chapter III demonstrates the CMOS implementation of the oscillation control blocks in CPPLLs. The next chapter, Chapter IV, introduces the design and test of two phase-locked loops with a single-ended control line; one of the loops is designed for maximum frequency. Chapter V describes the design of a low-jitter differential CPPLL in a standard submicron CMOS process. An LC oscillator is successfully utilized in the differential design, while the two single-ended PLLs utilize ring oscillators. Chapter VI is a comparative study of the

designs within this research and recent significant publications, discussing the major PLL design considerations.

In the past decade, there has been extensive research emphasis on analog charge-pump PLLs (CPPLL) and all digital PLLs (ADPLL) to achieve high performance. So far, only limited attention has been paid to hybrid systems that utilize advantages of digital circuits in the analog feedback loop. In this context, a class of otherwise analog PLLs that use a digital control path is analyzed for driving a current-controlled oscillator (CCO) in Chapter VII. Fundamentally, this chapter focuses on producing a control signal (a digital word in this case) that is less sensitive to variations in a submicron process. Particular emphasis is on merging the advantages of digital circuits with those of analog circuits for a more stable control voltage/current generation to achieve higher precision in oscillation control. A novel method for digitization is developed where trains of pulses code the phase/frequency comparison information rather than the duration of the pulses. Finally, in Chapter VIII, a brief summary of the research is presented with suggestions on future work. The conclusion also includes the discussions on the major contributions and a series of guidelines for the design of low-jitter PLLs.

CHAPTER II

PHASE-LOCKED LOOPS

This chapter focuses on the basics of phase-locked loops. A brief evaluation of different PLL types in a unique way is followed by the literature review of implementation and application issues of PLLs.

2.1 Phase-Locked Loop Basics

A PLL is a circuit that synchronizes an oscillator's output signal with a reference or input signal in both frequency and phase. The phase error between the oscillator's output signal and the reference signal is constant (not necessarily zero) when the PLL is locked (reference input and oscillator output are synchronized). If a phase error builds up, the feedback control mechanism acts on the oscillator to reduce the phase error to a minimum. The PLL differs from other feedback systems in that it operates on phase deviations rather than signal amplitudes and the variable of interest changes dimension through the loop, shown in Figure 2 (the reference and oscillator signals are used interchangeably with input *x(t)* and output *y(t)*, respectively). The input signal (ref: reference) is usually a phase-modulated periodic signal, for example,

$$x(t) = A\cos[\omega_{in}t + \Phi_n(t)] \quad \textbf{(1)}$$

where ω_{in} is the input angular frequency, A is the input signal magnitude, $\Phi_n(t)$ is the excess phase. The total phase of this signal is defined as $\Phi_{in}(t) = \omega_{in}t + \Phi_n(t)$ and the instantaneous (angular) frequency as $\Omega_{in}(t) = d\Phi_{in}(t)/dt = \omega_{in} + d\Phi_n(t)/dt$.

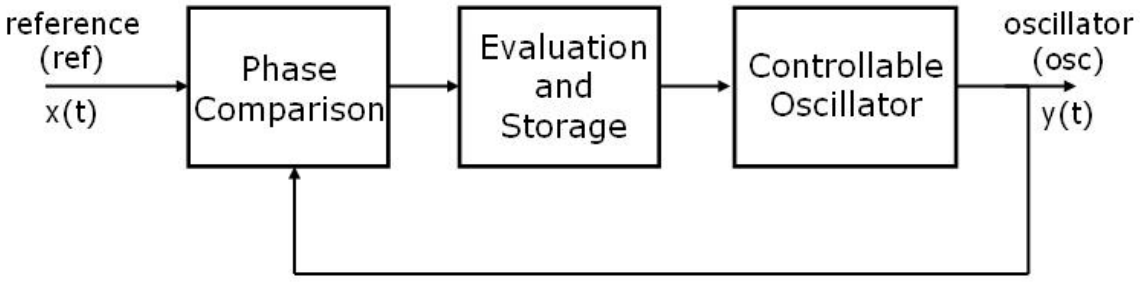


Figure 2: Phase-locked loop

The function of each block is as follows:

1. Comparison: This block compares the reference phase (and/or frequency) with the phase of the generated signal to generate an error signal proportional to the phase difference. The ideal transfer function of this block is K_{PD}, which is the gain of the phase detector ($V_{error} = K_{PD}\,\Delta\Phi$). In general, phase detectors (PD) or phase-frequency detectors (PFD) are used for detection. The PLL's transient behavior, capture range, and phase-lock characteristics are directly affected by the choice of the phase detector. The main properties that define a phase detector at the higher level are the transfer function, response to unequal input frequencies, and behavior dependencies on input signal amplitudes and duty cycles [12].
2. Evaluation and Storage: This block provides a control variable from the comparison and modifies its stored value (voltage or current) to apply to the

oscillator stage. A low-pass filter (LPF) is commonly employed for smoothing the variations caused by the input noise.

3. Controllable Oscillator: This nonlinear block generates an oscillation whose frequency is controlled by a lower frequency voltage or current input. The controllable oscillator appears in the form of a voltage-controlled oscillator (VCO) or a current-controlled oscillator (CCO) [13-15].

2.2 Phase-Locked Loop Architectures

The first application of a PLL was reported as early as 1932 by deBellescize [16]. Since then, different types of PLLs have been developed [17]. In general, PLLs can be classified into the four categories shown in Table 2 (software PLLs are outside the scope of this research). The four PLL types will briefly be described next.

Table 2: PLL implementation

PLL TYPE	COMPARISON	EVALUATION	STORAGE	OSCILLATOR
Linear PLL (LPLL)	Analog multiplier	LPF	Analog voltage on filter capacitor	VCO
Digital PLL (DPLL)	EXOR PD or JKPD	LPF	Analog voltage on filter capacitor	VCO
Charge-pump PLL (CPPLL)	PFD	Charge pump and LPF	Analog voltage on filter capacitor	VCO
All-digital PLL (ADPLL)	EXOR PD or JKPD or PFD	Digital LPF	Digital word	Digitally controlled oscillator (DCO)

2.2.1 The Linear PLL

The most basic phase-locking feedback loop is the linear PLL (Figure 3). It consists of an analog mixer phase detector (analog multiplier), a low-pass filter (LPF), and a voltage-

controlled oscillator. The VCO control voltage is the low frequency component of the multiplier output extracted by the LPF.

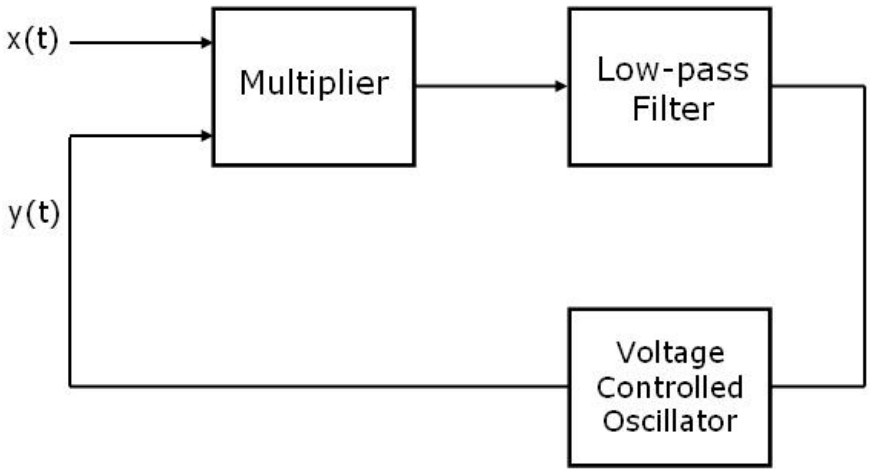


Figure 3: Block diagram of the linear PLL

The analog mixer phase detector generates an output $y(t)$ for inputs $x_1(t) = A_1 \cos\omega_1 t$ and $x_2(t) = A_2 \cos(\omega_2 t + \Delta\Phi)$:

$$y(t) = \alpha A_1 \cos\omega_1 t \cdot A_2 \cos(\omega_2 t + \Delta\Phi) \quad \textbf{(2)}$$

$$y(t) = \frac{\alpha A_1 A_2}{2}\cos\left[(\omega_1 + \omega_2)t + \Delta\Phi\right] + \frac{\alpha A_1 A_2}{2}\cos\left[(\omega_1 - \omega_2)t - \Delta\Phi\right] \quad \textbf{(3)}$$

where α is a proportionality constant and $\Delta\Phi$ is the phase difference of the input signals. For $\omega_1 = \omega_2$, the low-pass filtered phase-voltage characteristic can be written as

$$\overline{y(t)} = \frac{\alpha A_1 A_2}{2}\cos\Delta\phi \quad \textbf{(4)}$$

The sinusoidal characteristic, plotted in Figure 4, does not have a constant slope nor a monotonic feature. It can be linearized in the vicinity of $\pi/2$ to yield a phase detector gain of $K_{PD} = -\alpha A_1 A_2/2$:

$$\overline{y(t)} \approx \frac{\alpha A_1 A_2}{2}\left(\frac{\pi}{2} - \Delta\phi\right) \quad \textbf{(5)}$$

It is important to note that LPLL requires inputs that have the same frequency to enable the phase locking. The cosine multiplication does not generate any DC term if the two input frequencies are different, resulting in a zero average output. Therefore this phase detector cannot be used as a frequency detector. The input amplitude dependency and the nonlinear gain are the main disadvantages of using an analog mixer as a phase detector. Although it is not commonly employed in many recent systems, the LPLL led to the development and mathematical-modeling of current designs.

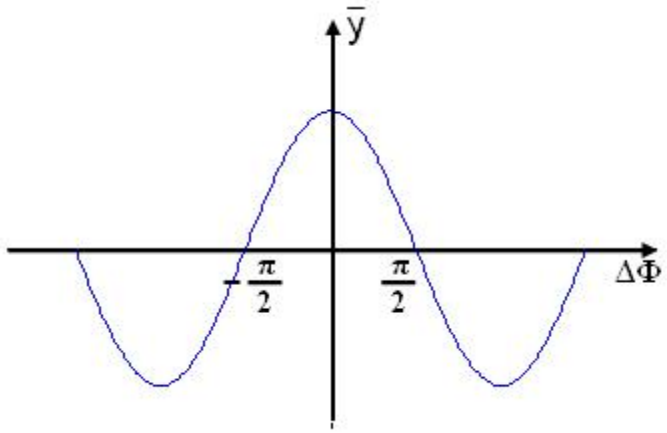


Figure 4: Characteristic of an analog mixer

2.2.2 The Digital PLL

The amplitude sensitivity and the nonlinear gain problems of the LPLL can be solved by using input signals that are large enough to drive the transistors of the multiplier cell to full switching. This yields the XOR phase detector implementation. This simple XOR operation is shown for various phase difference cases in Figure 5.

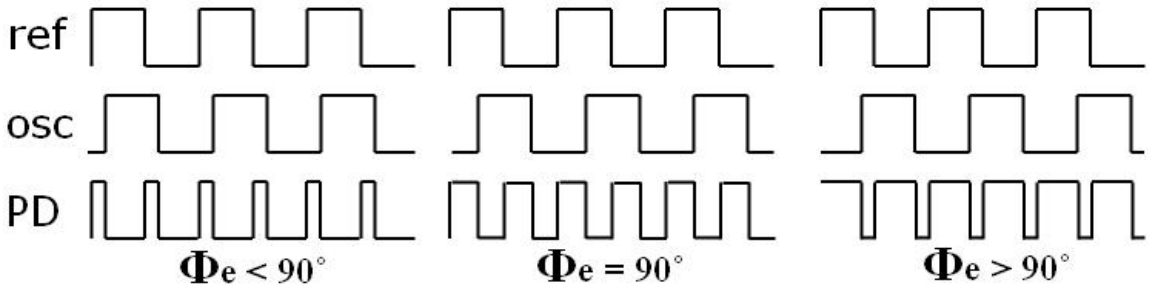


Figure 5: XOR phase detector behavior

As seen from the above figure, the output signal has twice the frequency of the input with a duty cycle linearly proportional to the phase difference with a value of 50% for quadratic inputs. This translates to phase detection characteristics as in Figure 6.

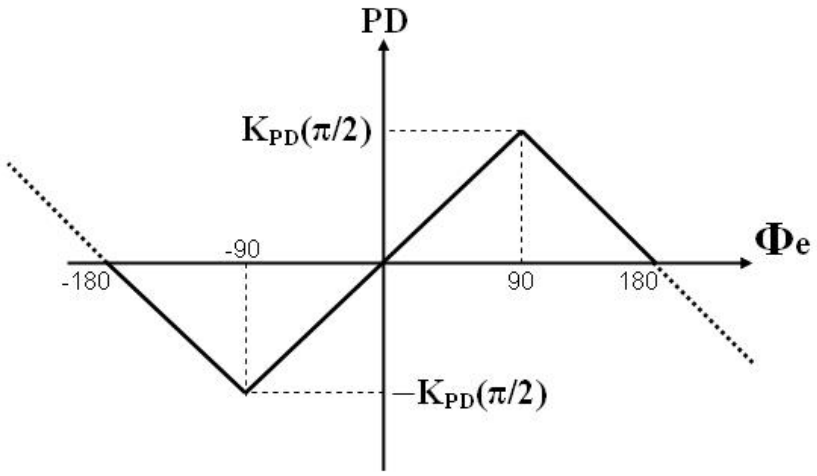


Figure 6: Characteristic of an XOR phase detector

Since the XOR operation is based on the overlapping of the signals rather than the transition time difference, the inputs without 50% duty cycle will lead to gain clipping at the above characteristic figure.

The input duty cycle sensitivity of these phase detectors introduces the requirement of edge-triggered parts in the phase detection process. A JK phase detector makes use of the JK flip-flops to solve the duty cycle sensitivity.

The JKFF output is set at the positive edge of the J input and reset at the positive edge of the K input. This behavior is demonstrated in Figure 7. The output is no longer sensitive to the input duty cycle and has the same frequency as the input.

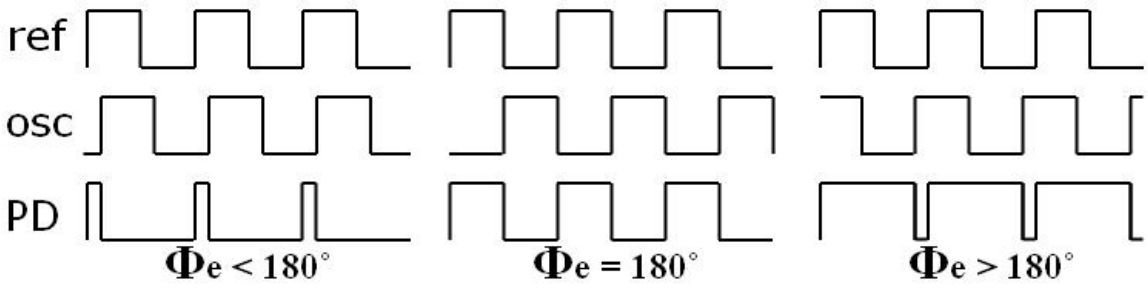


Figure 7: JK phase detector behavior

The linear gain is halved compared to the XOR phase detector while the monotonic range is doubled as demonstrated in Figure 8.

The general requirement on the input frequencies for the phase detectors can be relaxed by the JKPD to the correlation of being an integer multiple of each instead of having to be exactly equal. A divide-by-N block can be inserted in the DPLL (Figure 9) feedback loop to generate a VCO frequency that is N times the reference frequency.

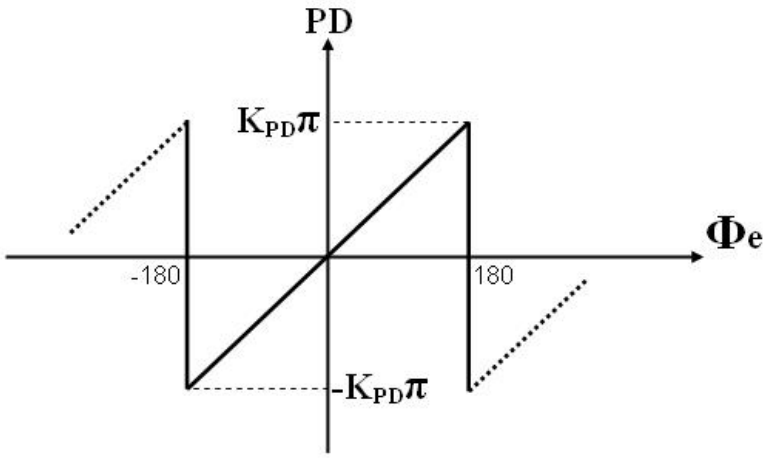


Figure 8: Characteristic of a JK phase detector

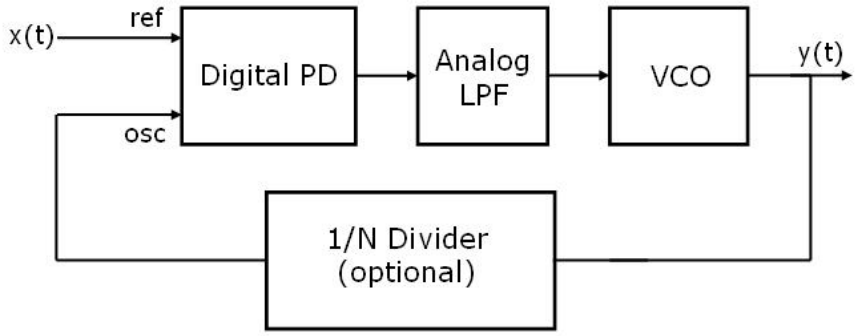


Figure 9: Block diagram of the digital PLL

Digital PLLs consist of all analog components other than the phase detector. Even though it is called digital, it is not a digital, sampled data system. The output of the phase detector is a continuous signal that is fed into an analog loop filter.

2.2.2.1 Low-Pass Filter

The stability characteristics and the dynamic behavior of the PLL depend on the loop filter. Loop filter sets the closed loop bandwidth, a key design parameter for noise

suppression, as lower bandwidth suppresses the input noise and higher bandwidth suppresses VCO noise.

The noise characteristics of a PLL also depend on the loop filter as it determines the closed loop bandwidth. Smaller bandwidth results in longer lock time but lower jitter; whereas larger bandwidth results in faster lock with worse jitter performance. The fact that input noise is low-pass filtered and the VCO noise is high-pass filtered through the loop to the output also makes the loop bandwidth a very important design parameter.

A passive low-pass filter is the general approach for high speed PLL implementation while active low-pass filters can be designed for smaller real estate or high gain which may be required to obtain zero steady-state phase error.

A first-order filter is used in most linear PLL designs. A passive lead-lag filter and its amplitude response are shown in Figure 10. Its transfer function $H_1(s)$ is given by

$$H_1(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \quad \textbf{(6)}$$

where $\tau_1 = R_1C$ and $\tau_2 = R_2C$.

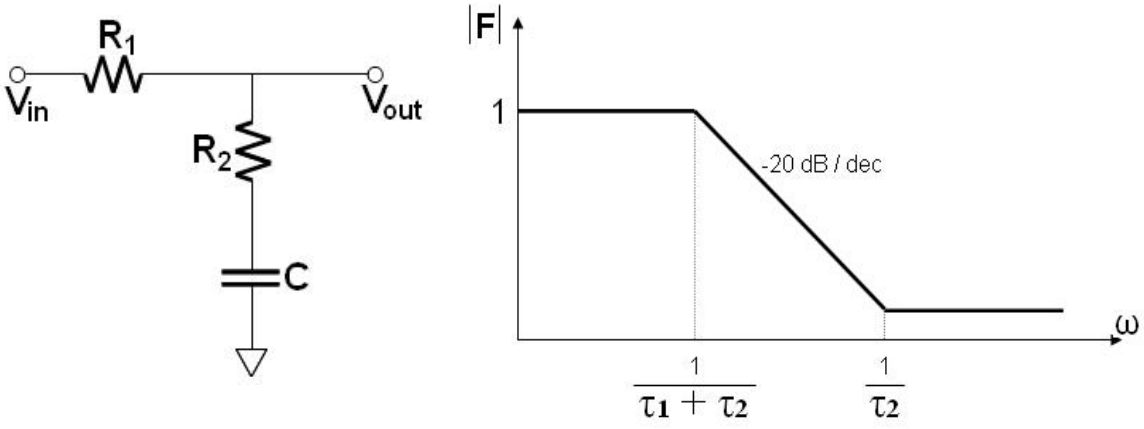


Figure 10: The passive lag filter schematic and amplitude response

Figure 11 shows an active lead-lag filter and the bode plot of the amplitude response. This active filter has a transfer function that is very similar to the passive lead-lag filter. One important difference is the gain term K_a, which can be assigned to a value greater than 1. Its transfer function $H_2(s)$ is given by

$$H_2(s) = K_a \frac{1 + s\tau_2}{1 + s\tau_1} \tag{7}$$

where $\tau_1 = R_1C_1$, $\tau_2 = R_2C_2$, and $K_a = -C_1/C_2$.

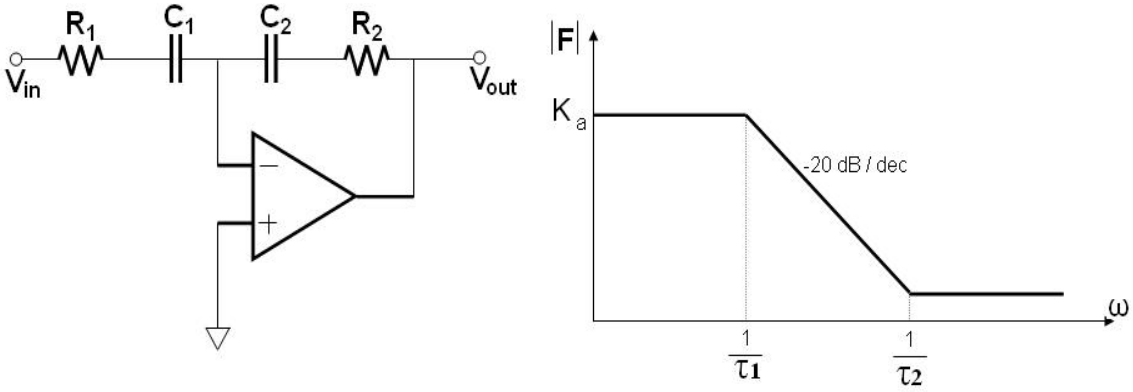


Figure 11: An active lag filter schematic and amplitude response

Another active filter in Figure 12 is referred to as "PI" filter which stands for the "proportional + integral" behavior. The PI filter has an infinite DC gain due to the pole at the origin. Its transfer function $H_3(s)$ is given by

$$H_3(s) = -\frac{1 + s\tau_2}{s\tau_1} \tag{8}$$

where $\tau_1 = R_1C_1$and $\tau_2 = R_2C_2$.

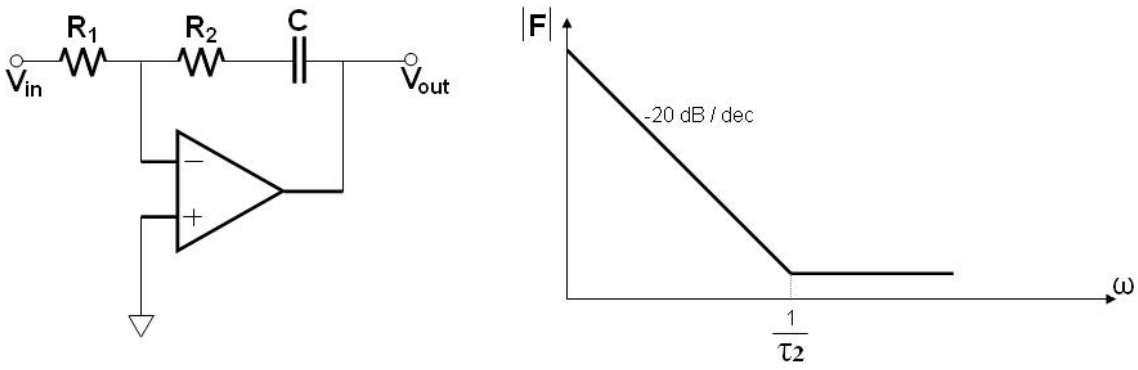


Figure 12: Active PI filter schematic and amplitude response

Instead of these simple one-pole filters, higher-order low-pass filters can be used. However, maintaining stability would be harder in higher-order systems as each additional pole introduces a phase shift.

2.2.2.2 Voltage Controlled Oscillator

As suggested by its name, a voltage-controlled oscillator (VCO) ideally generates a periodic signal with a frequency that linearly depends on the input (control) voltage $V_{ctrl}(t)$. Grounded input drives the VCO to run at its free-running frequency ω_{FR}. Assuming a linear gain of K_{VCO} (rad/s/V) for this block, which really is not true for practical VCOs, output frequeny is found to be:

$$\omega_{out} = \omega_{FR} + K_{VCO} V_{ctrl} \quad \textbf{(9)}$$

leading to an output in the form of

$$y(t) = A \cdot \cos(\omega_{FR} t + K_{VCO} \int_{-\infty}^{t} V_{ctrl} \cdot dt) \quad \textbf{(10)}$$

The excess phase output of the VCO, Φ_{out}, depends not only on the instantaneous value of $V_{ctrl}(t)$ but also on its history due to integration of frequency changes in time to form phase information. All these linear time-invariant (LTI) system assumptions on the simple PLL analysis give the following transfer function for the VCO in the s-domain with a pole at the origin due to integration.

$$\frac{\Phi_{out}}{V_{in}} = \frac{K_{VCO}}{s} \quad \textbf{(11)}$$

2.2.2.3 Loop Dynamics

The purpose of the negative feedback used in a PLL is to make the two input frequencies equal at the steady state, which also means the phase error, Φ_e, being constant (not necessarily zero). Φ_e is used to generate a proportional dc voltage at the PD output. This is the voltage controlling the VCO to generate the same as the previous cycle phase error after the low-pass filter attenuates higher frequency components.

Even though the nonlinear PLL operation cannot be formulated easily, the linearized model of the PLL in lock, shown in Figure 13, helps to gain intuition and understand the trade-offs in design. The transfer function of each block is also depicted on the same figure. The phase detector determines the phase difference of the input and the feedback signal, and, hence, is represented by a subtractor. The voltage transfer function of the low-pass filter is assumed to be $H_{LPF}(s)$. The VCO transfer function was shown to be K_{VCO}/s in the previous section. As a result, the open-loop transfer function is

$$H_O(s) = K_{PD} H_{LPF}(s) \frac{K_{VCO}}{s} \tag{12}$$

yielding the following closed-loop transfer function from reference phase input to VCO phase output:

$$H(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{K_{PD} K_{VCO} H_{LPF}(s)}{s + K_{PD} K_{VCO} H_{LPF}(s)} \tag{13}$$

The error transfer function, which relates the phase error to the input phase, can be defined by

$$H_e(s) = \frac{\Phi_e(s)}{\Phi_{in}(s)} = \frac{s}{s + K_{PD} K_{VCO} H_{LPF}(s)} \tag{14}$$

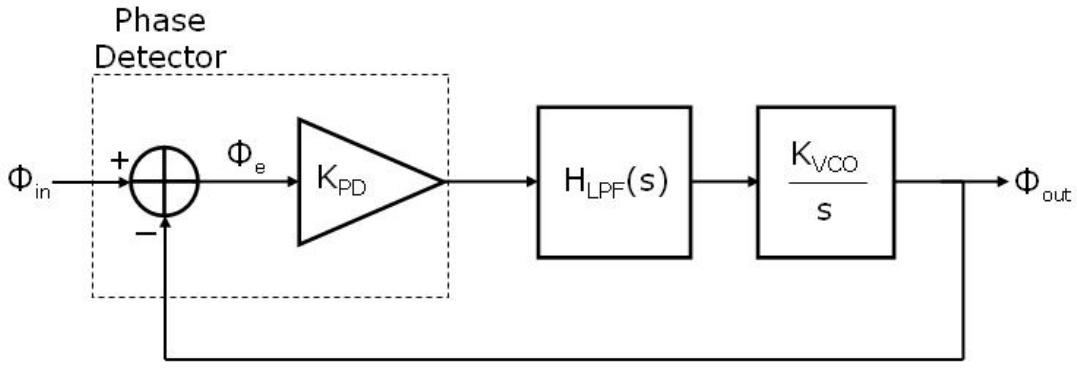


Figure 13: Linearized PLL model

The error transfer function can be useful to estimate the response of the loop to input deviations such as frequency step or phase step. The loop gain K, expressed in rad/s, is the product of the phase detector gain and the VCO gain.

$$K = K_{PD}\, K_{VCO} \tag{15}$$

The closed-loop transfer function reduces to:

$$H(s) = \frac{K}{\frac{s^2}{\omega_{LPF}} + s + K} \tag{16}$$

if the low-pass filter is implemented as a simple RC filter with

$$H_{LPF}(s) = \frac{1}{1 + \frac{s}{\omega_{LPF}}} \tag{17}$$

where $\omega_{LPF} = 1/(RC)$.

The dynamic behavior of the PLL can be analyzed after converting the denominator to the normalized form in control theory: $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ζ is the damping factor and ω_n is the system's natural frequency. Consequently,

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{18}$$

where

$$\omega_n = \sqrt{\omega_{LPF} K} \tag{19}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K}} \tag{20}$$

The direct relationship between K, ζ, and ω_{LPF} is an important drawback because it does not allow independent selection of K and ω_{LPF}. For example, increasing the loop gain reduces the phase error while degrading the settling behavior. In order to be able to set these parameters independently a passive lag filter, an active lag filter, or an active PI filter can be incorporated. The transfer functions for these filters were derived in Section 2.2.2.1. The closed loop transfer functions for each of these filters are

- Passive lag filter

$$H(s) = \frac{K\dfrac{1+s\tau_2}{\tau_1+\tau_2}}{s^2 + s\dfrac{1+K\tau_2}{\tau_1+\tau_2} + \dfrac{K}{\tau_1+\tau_2}} \tag{21}$$

- Active lag filter

$$H(s) = \frac{KK_a\dfrac{1+s\tau_2}{\tau_1}}{s^2 + s\dfrac{1+KK_a\tau_2}{\tau_1} + \dfrac{KK_a}{\tau_1}} \tag{22}$$

- Active PI filter

$$H(s) = \frac{K\dfrac{1+s\tau_2}{\tau_1}}{s^2 + s\dfrac{K\tau_2}{\tau_1} + \dfrac{K}{\tau_1+\tau_2}} \tag{23}$$

The natural frequencies and the damping factors for each of these cases are

- Passive lag filter

$$\omega_n = \sqrt{\frac{K}{\tau_1+\tau_2}} \qquad \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K}\right) \tag{24}$$

- Active lag filter

$$\omega_n = \sqrt{\frac{KK_a}{\tau_1}} \qquad \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{KK_a}\right) \tag{25}$$

- Active PI filter

$$\omega_n = \sqrt{\frac{K}{\tau_1}} \qquad \zeta = \frac{\omega_n\tau_2}{2} \tag{26}$$

These second-order loop functions can be utilized to determine the behavior of the system in lock. The lock state is when the jitter estimation is of interest. The stability of the PLL can be determined using classical techniques such as root locus, bode plots, or Nyquist plots.

2.2.3 The All-Digital PLL

Phase-locked loops are often part of a very large-scale integrated system on a chip. PLL designs with all-digital blocks have therefore been an attractive choice for some applications. The all-digital PLL's (ADPLL) digital nature reduces lock time, making it a valuable option for microprocessors with power management network [18-20]. Furthermore, the phase and frequency information can be more accurately stored using digital techniques. This is another important advantage of the ADPLL implemented in a submicron process as the leakage currents increase. Also, the ADPLL design can easily be transferred between technologies [21, 22]. Many of the complicated evaluation algorithms, such as Kalman filtering, can be implemented precisely using digital techniques trading with operational speed, the die size, and the design complexity. Most of these ADPLLs are not capable of providing true frequency synthesis as they require a high-frequency clock source [23, 24]. Figure 14 depicts a block diagram for a very simple ADPLL. An EXOR or a JK phase detector can be employed as well as a PFD. The PFD is a tristate device that can track both phase and frequency. The details of its operation are given within the next section.

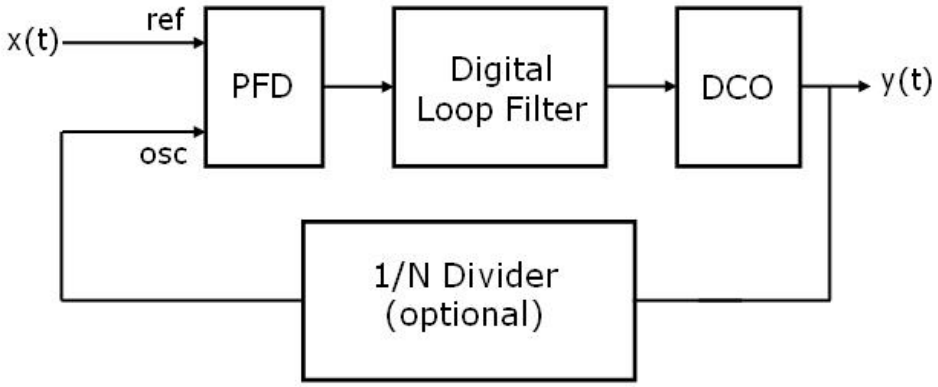


Figure 14: Block diagram of the ADPLL

2.2.4 The Charge-Pump PLL

The charge-pump PLL provides a useful solution to the phase-locking problem. The design is currently found in many high-speed and low-jitter systems. The CPPLL consists of a phase-frequency detector (PFD), a charge pump (CP), a loop filter, and an oscillator. The block diagram of a typical CPPLL that utilizes a first-order passive filter is given in Figure 15. It is different from the other approaches in that the PFD detects the phase while it tracks the frequency. A conventional PFD generates two output signals (UP and DOWN) and works like a tristable device as the fourth state (UP = DOWN = high) is inhibited. The behavior of these outputs for various input conditions is demonstrated in Figure 16.

The 3-state PFD output is used to modify the voltage on the loop filter capacitor by adding or removing charge through the charge pump [25]. More precisely:

- A current pulse (I_{CP}) to discharge the loop filter capacitor is produced when the VCO is leading the reference (UP = low, DOWN = high)
- A current pulse (I_{CP}) to charge the loop filter capacitor is produced when the VCO is lagging the reference (UP = low, DOWN = high)

- No charge/discharge pulses generated to keep the filter charge constant (UP = DOWN = low).

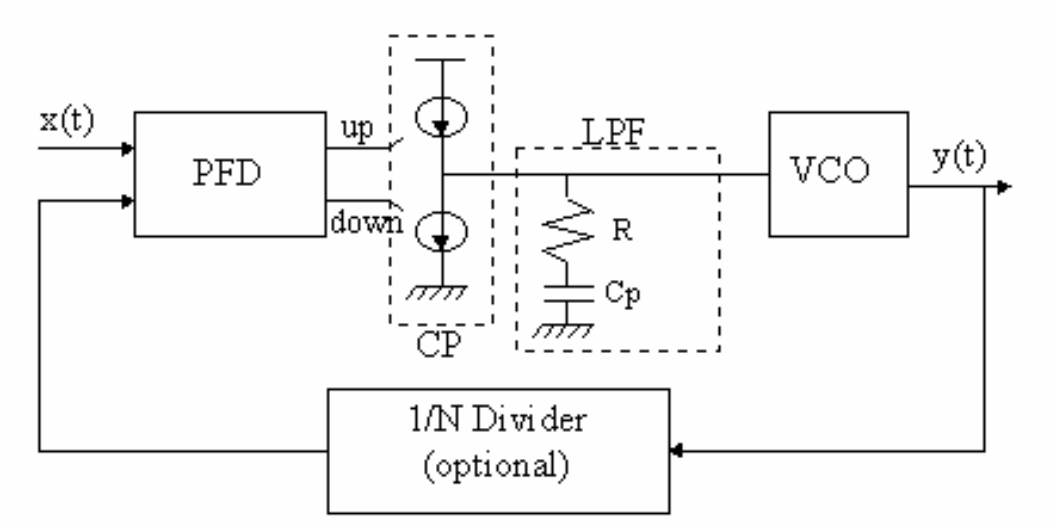


Figure 15: Block diagram of the CPPLL

The loop dynamics and the linear model of the CPPLL are discussed in this section; the implementation details for PFDs and charge pumps will be discussed in the next chapter.

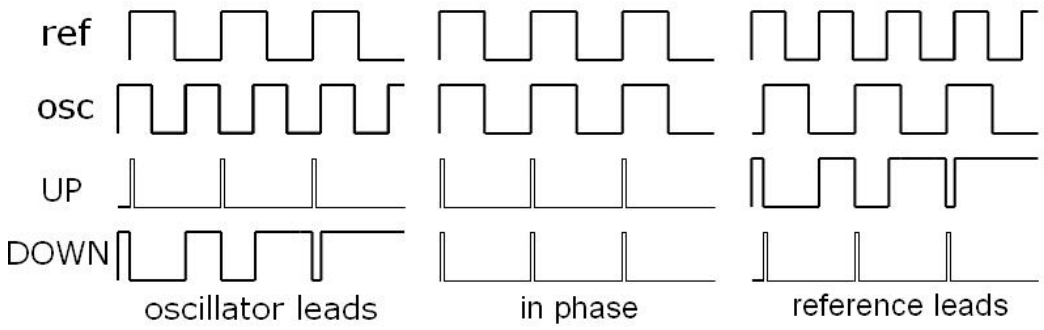


Figure 16: Phase-frequency detector behavior

Charge pumps offer an infinite gain for a static input phase difference, indicating that the transfer function of the PFD together with the charge pump contains a pole at the origin. The closed-loop transfer function of the PLL without a low-pass filter becomes

$$H(s) = \frac{\frac{K_{PFD}}{s}\frac{K_{VCO}}{s}}{1+\frac{K_{PFD}}{s}\frac{K_{VCO}}{s}} = \frac{K_{PFD}K_{VCO}}{s^2 + K_{PFD}K_{VCO}} \quad \textbf{(27)}$$

with two imaginary poles at

$$\omega = \pm\sqrt{K_{PFD}K_{VCO}} \quad \textbf{(28)}$$

Due to the two poles contributed by the charge pump and the VCO, the CPPLL cannot remain stable. To avoid instability, a zero has to be added in the open loop transfer function. This can be done either by inserting a series resistor in the loop filter or by using feedforward via an auxiliary charge pump [26]. The latter is accomplished by adding a fast signal path in parallel with the main charge pump. Illustrated in Figure 17, the auxiliary charge pump drives a dissipative RC network, R_2 and C_2. The closed loop transfer function thus becomes

$$H_{CP}(s) = \frac{I_{P1}}{2\pi C_1 s} + \frac{I_{P2}R_2}{2\pi(R_2C_2s+1)} = \frac{(I_{P1}R_2C_2 + I_{P2}R_2C_1)s + I_{P1}}{2\pi C_1 s(R_2C_2s+1)} \quad \textbf{(29)}$$

with a zero located at

$$\omega_Z = -\left(R_2C_2 + R_2C_1\frac{I_{P2}}{I_{P1}}\right)^{-1} \quad \textbf{(31)}$$

The auxiliary charge pump method introduces a pole at $\omega_P = -1/(R_2C_2)$, resulting in a third-order system. Furthermore, the voltage ripple across C_2 due to R_2 modulates the VCO frequency.

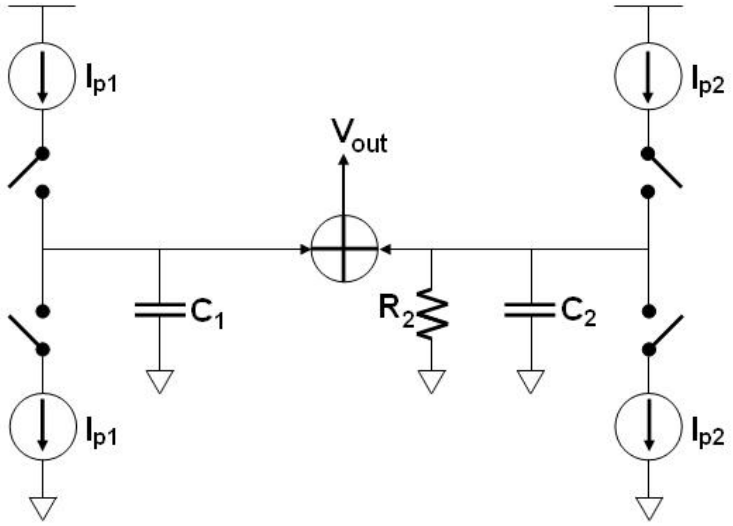


Figure 17: Addition of zero by an auxiliary charge pump

The use of a stabilizing series resistor, demonstrated in Figure 15, is more common in practice. A phase error of Φe = Φin – Φvco generates an average charge pump current of $I_{CP}/ 2\pi$. This average current corresponds to an average control voltage change given by

$$V_{ctrl}(s) = \frac{I\phi_e}{2\pi}(R + \frac{1}{C_P s}) \tag{32}$$

Hence, the closed loop transfer function is obtained as

$$H(s) = \frac{\frac{I}{2\pi NC_P}(RC_P s + 1)K_{VCO}}{s^2 + s\frac{I}{2\pi N}K_{VCO}R + \frac{I}{2\pi NC_P}K_{VCO}} \tag{33}$$

Thus, the system is characterized by

$$\omega_n = \sqrt{\frac{I}{2\pi NC_P}K_{VCO}} \qquad \zeta = \frac{R}{2}\sqrt{\frac{IC_P}{2\pi N}K_{VCO}} \tag{34}$$

$$\omega_Z = -\frac{1}{RC_P} \tag{35}$$

The derived continuous-time model of the loop depends on the assumption that the loop bandwidth is much less than the input frequency. The PLL state changes by a small amount during each cycle of the input if the frequency criterion holds. However, as the loop bandwidth becomes comparable with the input frequency, the continuous-time model fails, necessitating discrete-time analysis. In many applications, it is desired to maximize the bandwidth; however, Gardner has derived a stability limit for the loop bandwidth that can be written as [27]

$$\omega_n{}^2 < \frac{\omega_{in}{}^2}{\pi(RC_P\omega_{in} + \pi)} \tag{37}$$

Nonzero phase error and the limited capture range are the two major problems of linear and digital PLLs. The charge-pump PLL solves these problems by introducing an infinite gain by using the charge pump to detect a static phase difference at the input. On the other hand, a charge pump increases the complexity by introducing more parameters to the loop operation, and also decreases the stability by generating a second pole at the origin.

CHAPTER III

OSCILLATION CONTROL IN CHARGE-PUMP PLLs

Among the different PLL topologies discussed in Chapter II, charge-pump PLLs are widely used in contemporary communication systems due to the advantages they offer over traditional approaches. Fundamentally, an ideal charge pump combined with a PFD provides an infinite DC gain with passive filters, which results in unbounded pull-in range (limited by the VCO frequency range). As long as the PFD and the charge pump are ideal, zero static phase error can be achieved. The PFD and the charge pump however show non-ideal behavior when implemented in circuit. In 1996, VonKaenel et al. reported a PLL design for which they showed measured and simulated data for the phase jitter contribution of the various PLL components [4]. The experiments showed that the control blocks in a clean environment contributed 45.4% of the phase jitter. In general, the phase noise caused by the PFD is due to a possible dead-zone, a possible duty cycle dependency, or a possible unbalanced output generation. On the other hand, translating the timing information into an analog quantity, the charge pump is the dominant block in determining the phase noise.

The phase noise is observed as a dynamic clock skew in clock and data recovery applications and unwanted reference spur in frequency synthesis. Therefore, the practical issues in implementing PFDs and charge pumps need to be considered in a PLL design.

Several PFD and charge pump architectures in CMOS are investigated and their performances are compared in this chapter.

3.1 CMOS PFD Types and Comparison

The phase-frequency detector (PFD) determines the capture range of a PLL. The maximum operating frequency of the PFD is defined by the shortest time period during which correct PFD output signals can be generated when orthogonal inputs have the same frequency [28].

3.1.1 The Conventional PFD

In this design, the frequency information is coded at the output of a PFD that uses two D-flip-flops (DFF). The DFF outputs are denoted *UP* and *DN* (DOWN), respectively. Figure 18 shows the block diagram of the basic PFD. Assuming both outputs are initially low, a rising edge on the *REF* (reference) input causes the *UP* signal to go high. This indicates that the VCO frequency needs to be increased in order to match the input. Similarly, when the *VCO* input transitions high, the *DN* output rises. This state corresponds to the need to decrease the VCO frequency in order to match the input. When both outputs switch high, the AND gate propagates a reset signal returning the PFD to the zero state. Thus, the "*UP* = *DN* = high" state is suppressed by the feedback, and the PFD is essentially a three-state device. This behavior of the output signals is also demonstrated in Figure 18, where the minimum pulse width is determined by the reset path delay.

Ideally, this detector has an unlimited capture range. However, as the input frequencies approach each other, the DFFs get reset before any charge is fed onto the

filter capacitor by the CP; this defines the dead-zone. The presence of the dead-zone causes jitter in the locked PLL. It can be reduced by inserting inverters into the reset path to increase the reset delay. However, widening the reset pulse increases the time during which the two charge pump paths are simultaneously conducting. This short circuit alters the VCO control voltage and results in increased phase noise.

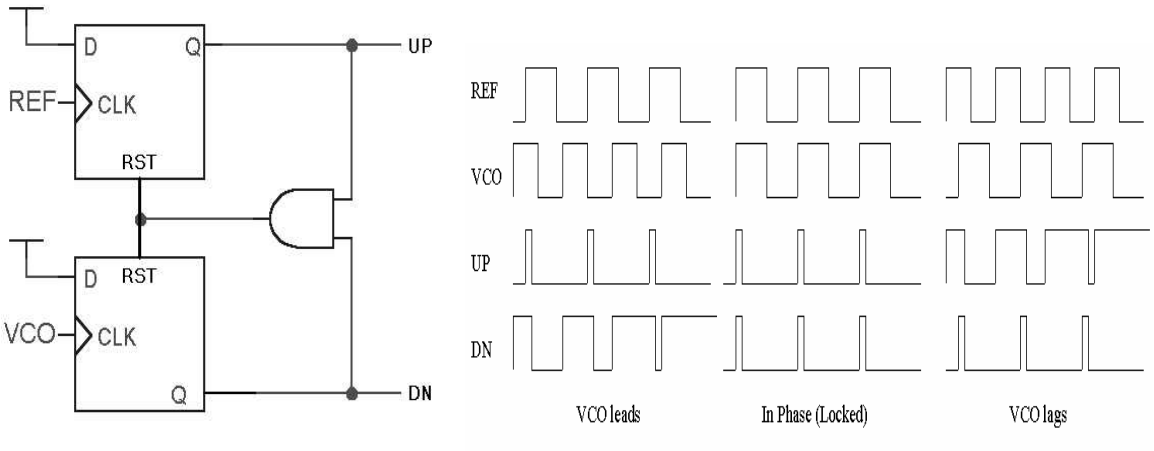
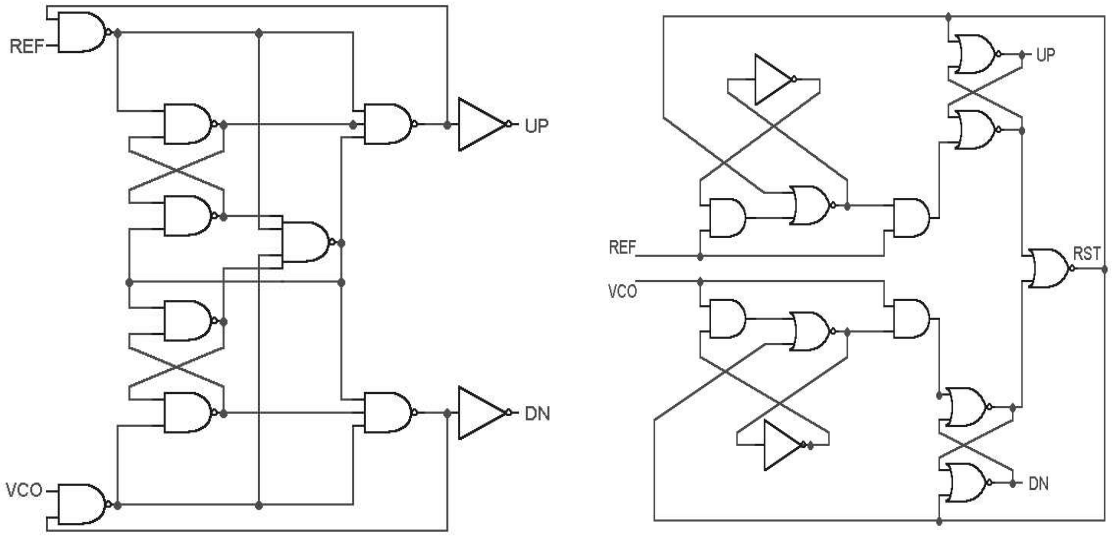


Figure 18: PFD block diagram and behavior

The DFFs also need to be matched. If one DFF resets earlier than the other, it can cause the reset signal to go to zero before the other DFF resets. Figure 19(a) shows the most common gate-level implementation of the PFD, where the reset path consists of three gate delays: NAND2, NAND3, and NAND4. NAND4 has three transistors in series for the pull-down path, hence slowing the PFD operation down and increasing the reset delay. This problem was solved in [10] using an optimized branch based implementation (Figure 19(b)). Shorter UP and DN pulses at steady-state result in lower jitter and better linearity without a dead-zone. This design is not superior to the NAND gate

implementation in terms of speed although it limits the number of serial transistors on each branch to two.

At high frequencies of operation, a low resistance path between VDD and GND is formed as internal nodes cannot completely be pulled up or down in conventional PFDs. This leads to high power-dissipation and a possible malfunction. Prescaler circuits can be used for frequency division at the front end of the PLL to avoid this problem. The drawback of this solution is proportionately increased steady state phase error with the division ratio.



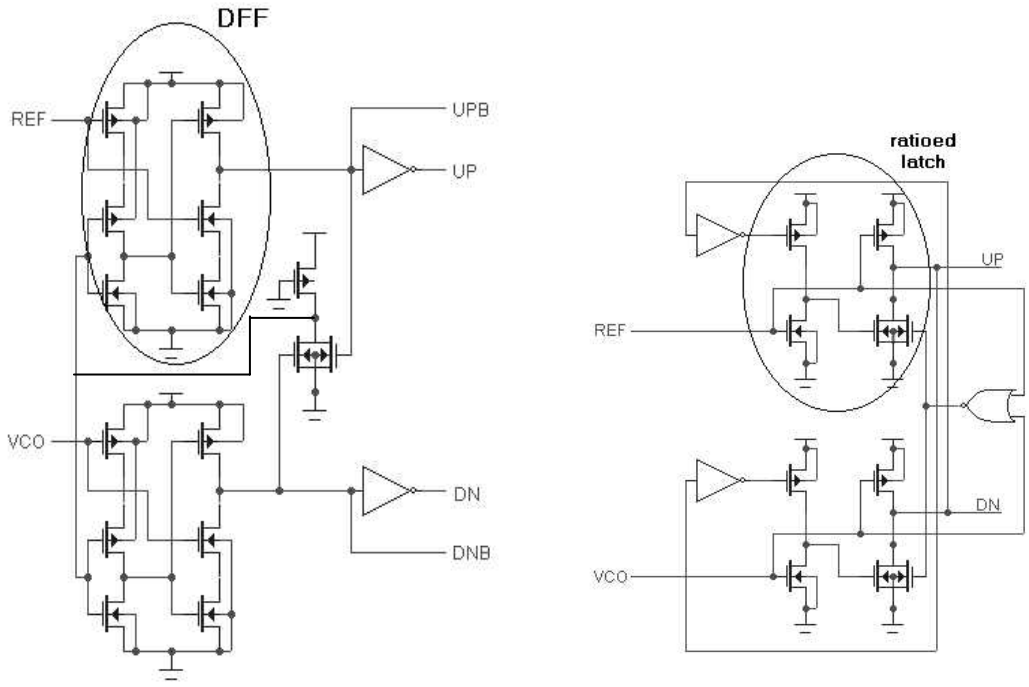
(a) (b)

Figure 19: Gate-level PFD (a) NAND based (b) branch based implementation

3.1.2 The PFDs with Improved D-Flip-Flops

The conventional PFD, also shown in Figure 18, consists of an AND gate and two DFFs. The DFF implementation, being an extensively studied topic, leads to many PFD design alternatives employing modified DFFs or latches for faster operation. Two of such PFDs are shown in Figures 20(a) [29] and 20(b) [30].

The true single-phase clock (TSPC) flip-flops are modified for the first design. A pseudo-NOR gate is used for high-speed operation. The reset path is shortened significantly. In the second design, the resettable-ratioed latches with secondary reset paths are used to achieve a short reset time. The design, however, is very sensitive to the process. For example, any threshold voltage variation can cause serious problems, such as generating a voltage-low output corresponding to a voltage-high input for the charge pump input transistors.



(a) (b)

Figure 20: PFD implementations (a) with modified DFF (b) with ratioed latch

3.1.3 Precharge Type PFD and Modified Precharge Type PFD

The precharge type PFD (pt-PFD, Figure 21(a)) is a very high speed circuit (no feedback path) that operates similar to the conventional sequential PFD. Existence of a dead-zone and input-limited capture range ($-\pi$ to π), however, are some major drawbacks of the

circuit. In addition, the phase sensitivity error is increased since each DFF is controlled by both inputs. In contrast with its fast operation, the pt-PFD suffers in terms of speed when the VCO is lagging the reference with a large frequency difference. At the VCO-lagging-state, the pt-PFD fails to detect all edges and the acquisition time increases substantially. This drawback was eliminated by a modified pt-PFD (mpt-PFD, Figure 21(b)) [31].

The mpt-PFD has a simpler structure than the pt-PFD, and acquires symmetry for the VCO leading and lagging cases. Although it operates slower than the pt-PFD, the mpt-PFD is still faster than the conventional PFD. The acquisition time is reduced significantly with the modifications, and the circuit consists of only 16 transistors.

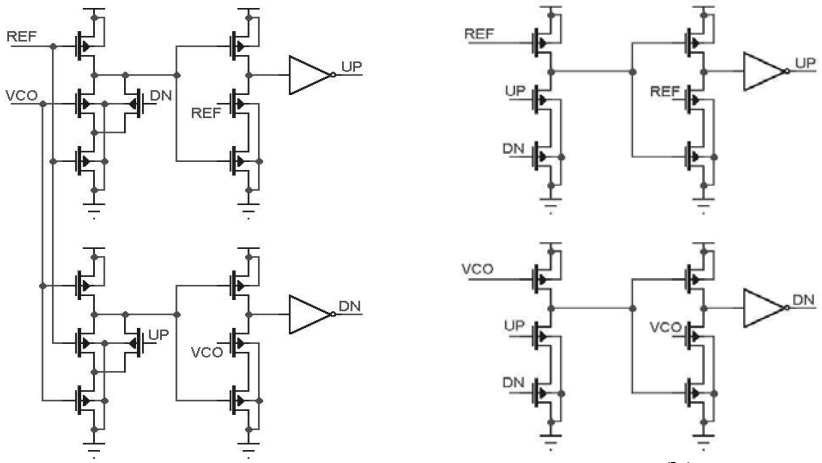


Figure 21: (a) Precharge type PFD (b) Modified precharge type PFD

3.1.4 NCPFD

The non-clock PFD (nc-PFD), Figure 22, is another pre-charged CMOS phase detector without a feedback loop [32]. It is useful for high-speed and low-jitter applications since

no dead-zone exists. However, the circuit suffers from input duty cycle dependency and the existence of a constant offset. Also, the phase sensitivity error is not low as each DFF is driven by both of the inputs, as in the pt-PFD case. The randomness in the lock-in time for a PLL employing the nc-PFD is another major drawback of the implementation.

The nc-PFD differs from other PFDs as it generates a 50% duty cycle output in case of lock rather than the minimum duty cycle output.

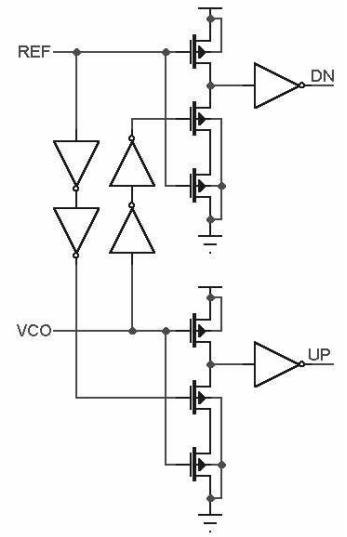


Figure 22: nc-PFD schematic

3.2 CMOS Charge Pump Types and Comparison

The charge pump (CP) is driven by the PFD to generate current pulses that add or remove charge from the loop filter capacitor. A simple charge pump diagram is shown in Figure 23. Requirements for an effective charge pump circuit can be summarized as follows:

1. Equal charge/discharge current at any charge pump output voltage

2. Minimal charge-injection and feed-through (due to switching) at the output node

3. Minimal charge sharing between the output node and any floating node, i.e. MOS switches at off position.

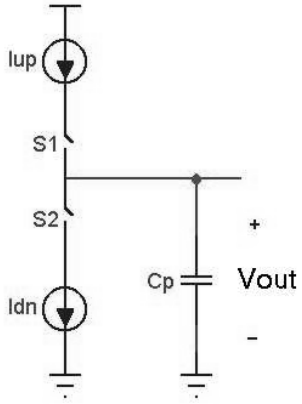
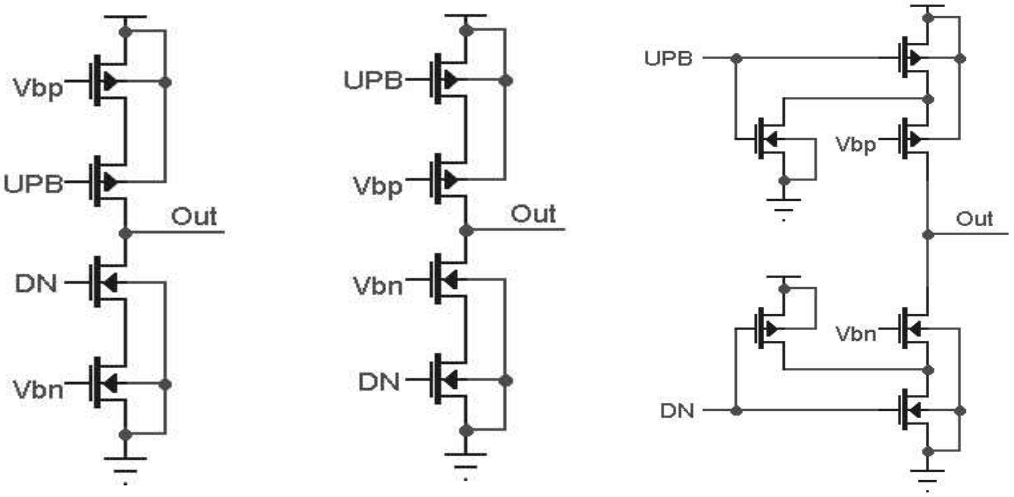


Figure 23: Charge pump

3.2.1 Single-Ended Charge Pumps

A single-ended charge pump is frequently used due to its lower power consumption and autonomous operation without an additional loop filter. A simple implementation of the charge pump and two of its variations are shown in Figure 24.



(a) (b) (c)

Figure 24: Single-ended charge pump variations

The bias voltages, Vbp and Vbn, are usually generated by a replica-bias circuit from a reference current to get the best matching between the charge (I_{UP}) and the discharge (I_{DN}) currents. The simplest version (Figure 24(a)) suffers from both direct charge-injection to the output node and charge sharing. The former problem can easily be solved either by inserting a drain to source shorted dummy transistor on each side of the switch transistors or by shifting the switches towards the rails as shown in Figure 24(b) [10]. However, the charge-sharing problem still exists for both designs due to the floating nodes in certain modes. A further modification to the design was made by inserting charge removal transistors to eliminate charge sharing as depicted in Figure 24(c) [33]. Not only a large reduction in the phase offset, but also the reduction of the intrinsic $1/f$ noise is achieved by this method with some sacrifice in the output linearity [34]. The nonlinearity is caused by the reverse-currents as the output voltages approach the rail voltages.

In addition to these slightly modified charge pumps, more complicated designs have been developed recently. These architectures are discussed next.

3.2.1.1 Charge pump with an Active Amplifier

Figure 25 shows the charge pump with an active amplifier; where the UP and DN signals from the PFD and their complements perturb the output voltage [28, 35-37]. When UP=1 and DN=0, the S1 and S4 switches turn on, charging the output by the pull-up current (I_{UP}). The voltages of the nodes N2 and N1 are equalized by the unity gain buffer during this state without N2 affecting the output. This voltage equalization eliminates the

charge-sharing problem appearing at the instances of switching. Although it suffers from charge injection, the design is useful when the loop filter capacitance is comparable to the parasitic capacitances.

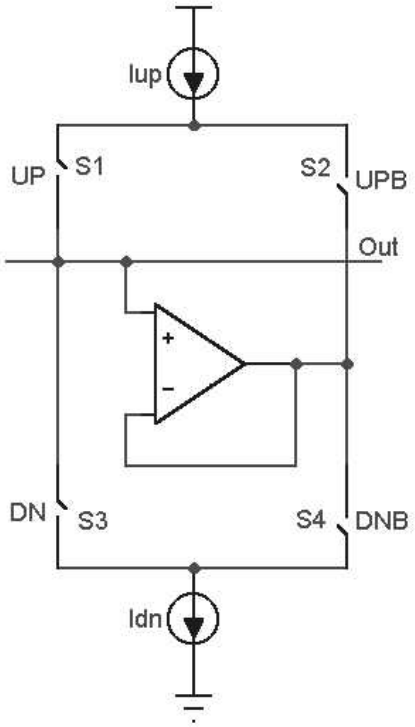
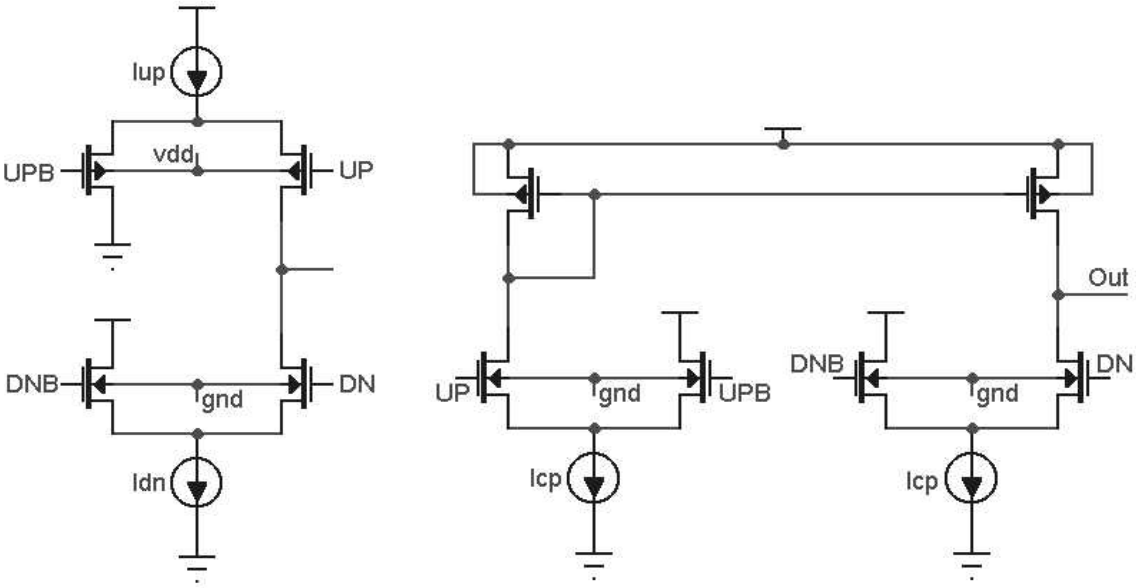


Figure 25: Charge pump with a unity-gain amplifier

3.2.1.2 Charge pump with Current Steering Switches

Two charge pump implementations with current steering switches are demonstrated in Figure 26. Both of them operate similar to the basic charge pump configuration shown in Figure 24(a), which has the charge sharing and the charge-injection problems. But an advantage of this design is that the differential current switches decrease the clock-skew by improving switching time. The only difference between the two designs, shown in Figure 26, is the use of only NMOS switches in the second circuit to avoid the inherit

mismatch of PMOS and NMOS devices [38]. The PMOS mirror in Figure 26(b) can be replaced by two current sources to transform the system into a differential charge pump.



(a) (b)

Figure 26: Charge pumps with current steering switches

3.2.1.3 Current Steering Amplifier Charge pump

This implementation (Figure 27) does not employ any switches; therefore, there are no floating nodes, and consequently no charge sharing takes place [25]. The forward-bias currents of the diode connected NMOS FETs are controlled by the UP and DN signals to be equal to I_{PMOS} or a portion of I_{PMOS}. The forward-biased diode voltage change corresponding to these two bias currents can easily be designed to be ten times lower than the maximum voltage swing (VDD) to reduce charge injection by more than 90%. The current subtraction at the output decreases the p-substrate noise due to the common mode effect. The output linear region is wide since every node has a single transistor on the

path to the rail. All these make this design useful for implementing a charge pump with low current to increase the resolution for a given capacitance. However, the low output impedance makes the charge/discharge currents more sensitive to the output voltage, causing small deviations from the linear characteristic.

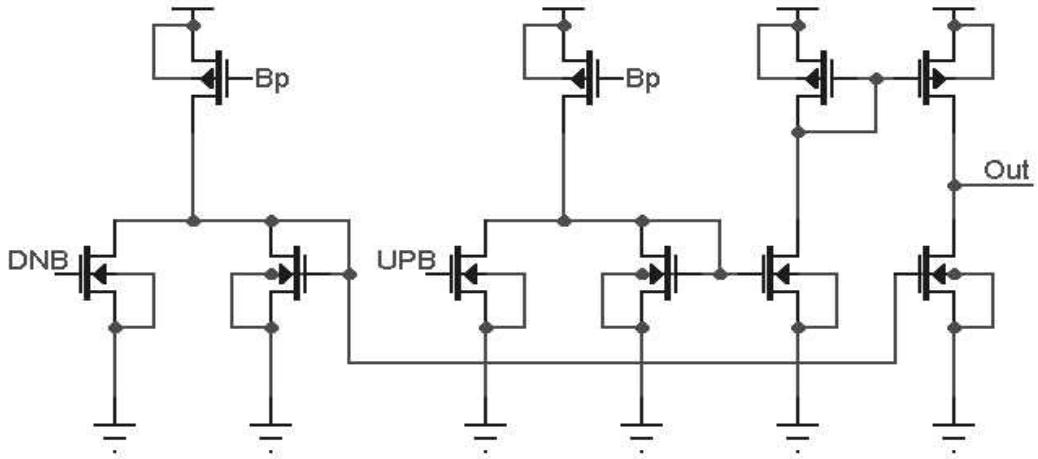


Figure 27: Current steering amplifier charge pump

3.2.1.4 Charge pump with an Improved Output Resistance

The usage of cascoded current mirrors can basically increase the output resistance of a simple charge pump. An example of this is the circuit given in Figure 28 [39]. In this design, the transistors M1 and M14 form charge pump switches; M4-M13 form the cascoded current mirrors; M2, M3, and M15 form the replica biasing; MC1 and MC2 reduce the charge coupling to the gate. This complicated design has higher output resistance and reduced charge injection. However, the decreased output range and charge sharing are the major problems with this implementation.

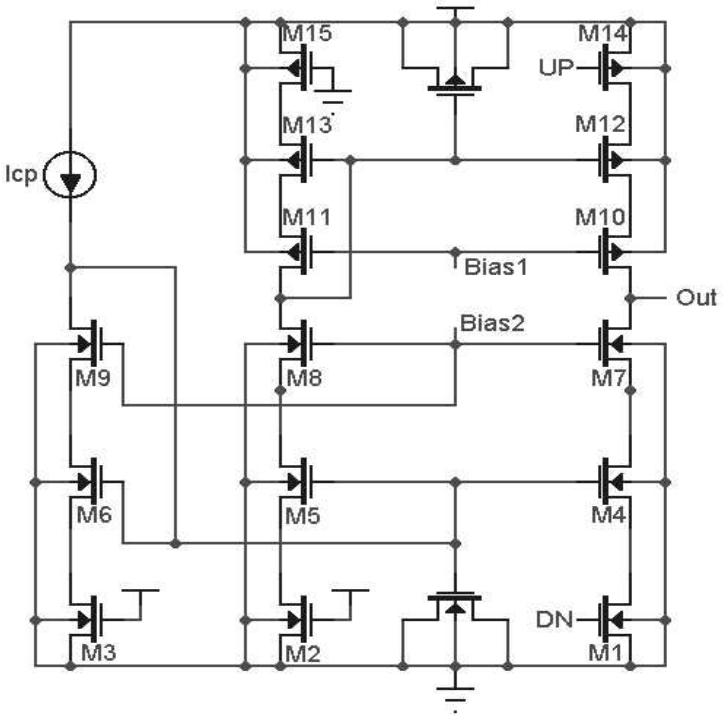


Figure 28: Charge pump with an improved output resistance

3.2.2 Differential Charge Pumps

A differential charge pump has two analog outputs: FST (FAST) and SLW (SLOW). These analog voltages are perturbed such that, when one is charged the other is discharged. In the locked state both outputs remain constant.

A differential charge pump in a PLL usually requires an additional loop filter and a common-mode feedback (CMFB) circuitry [13, 26, and 40]. Moreover, the power dissipation is increased due to the constant current biasing. Yet, the differential circuits have many advantages especially at very high frequencies. In addition to the leakage current in the submicron process, the supply, ground, and substrate noise in high-speed circuits become very significant sources of jitter. Using differential circuits extends these

limitations, as the leakage current and the supply noise behave like a common-mode offset with dual output stages. Also, the switch mismatches between the NMOS and the PMOS don't affect the circuit performance in a differential charge pump. Fully symmetric circuits cancel the offset due to the inverter delay between the input signals and their complements. The range of the output voltage compliance is doubled as well.

3.2.2.1 Conventional Differential Charge pump

Figure 29 shows the schematic of the conventional differential charge pump [41].

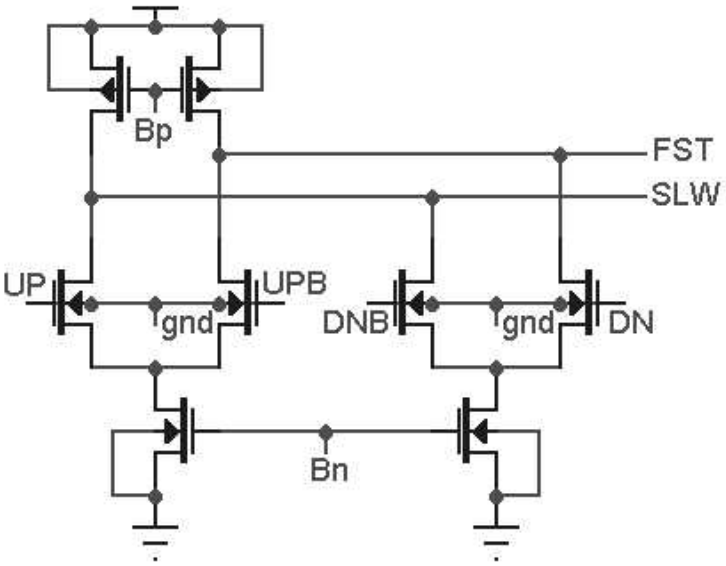
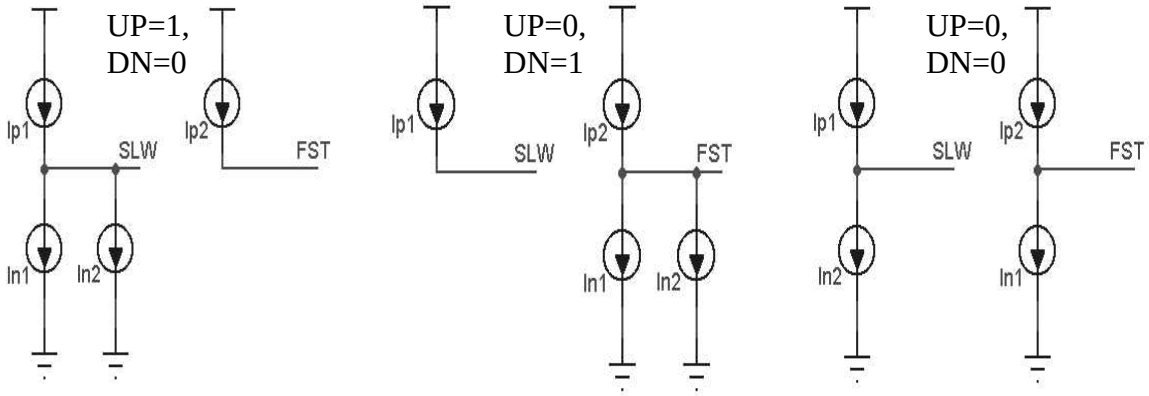


Figure 29: Conventional differential charge pump

The two current sources and the two current sinks need to be identical for the symmetry in charging and discharging. The operation of this design is shown in Figure 30. This design solves the charge-sharing problem since there is no floating node at any instant. However; charge injection, high power consumption, and current-source sensitivity to the output voltage are the main drawbacks of the circuit.



(a) (b) (c)

Figure 30: Conventional charge pump operation

3.2.2.2 Self-Biased Charge pump

A fully differential self-biased charge pump is given in Figure 31 [41].

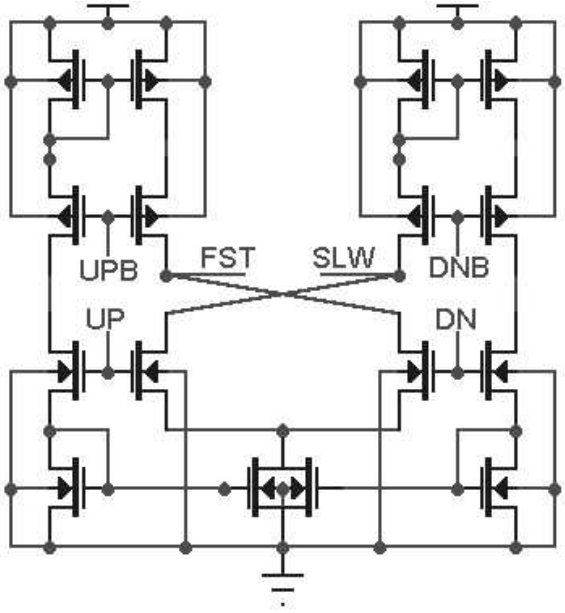


Figure 31: Self-biased charge pump

The current mirrors establish the internal current paths from the external ones in order to charge/discharge the output nodes. The current flow takes place only at the charging/discharging modes, decreasing the power dissipation. The output nodes float in the lock condition, reducing the PLL phase noise due to the current mismatch at lock. The slow operation, charge sharing and charge injection are the disadvantages of the circuit.

3.2.2.3 Differential Charge pump with an Improved Output Resistance

A differential charge pump with increased output impedance was proposed by Rhee [39]. As seen in Figure 32, the cascoded current mirrors are used to attain high-impedance outputs, thus achieving a better linearity during the charging and discharging periods. Furthermore, the folded PMOS current mirrors increase the circuit performance in low voltage applications.

This design doesn't require any additional circuitry for common-mode feedback. The bottom most NMOS transistors realize this operation by two of them being biased with the external common-mode voltage and the other two by the differential outputs.

This complicated design with five external bias voltages requires a careful calibration for good performance.

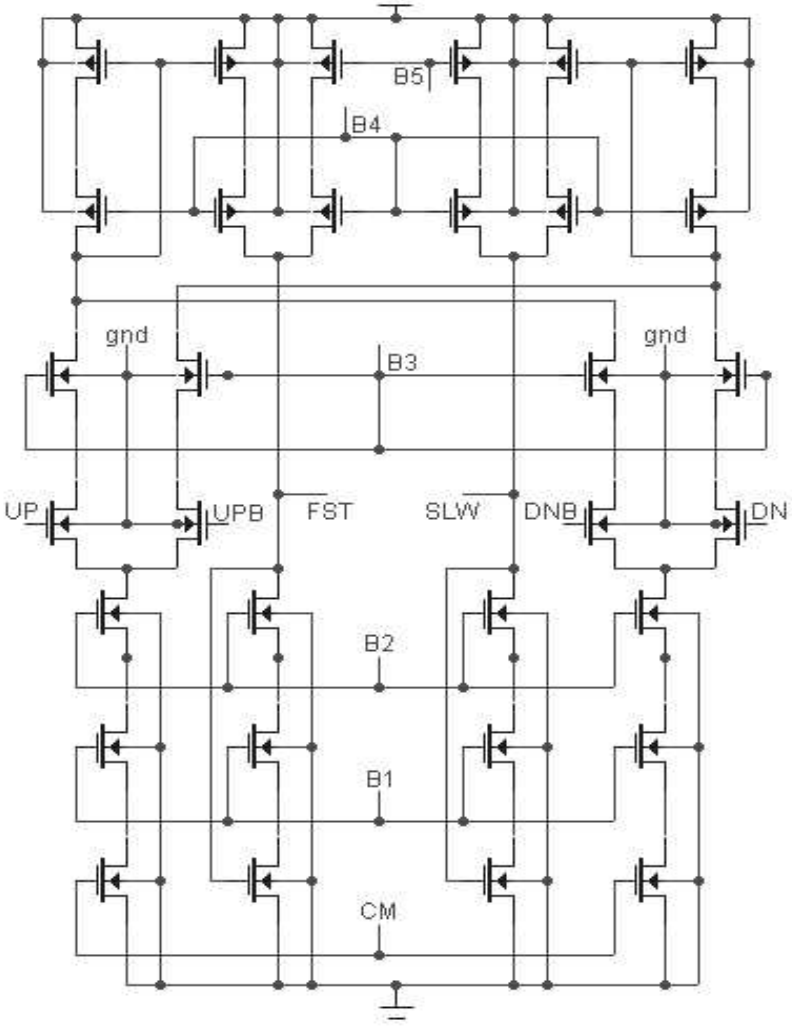


Figure 32: Differential increased output resistance charge pump with CMFB

CHAPTER IV

SINGLE-ENDED CONTROL FOR MULTI-GHz CPPLLs

As pointed out in Chapter III, charge-pump PLLs are widely employed inside integrated circuits since they can be integrated in a standard CMOS process and have the ability to eliminate DC phase offset with just a passive loop filter. However, owing to the complex loop characteristic and required precision of analog blocks, the design is not straightforward.

This chapter describes the design of low-jitter single-ended CPPLLs in a standard submicron CMOS process.

4.1 Design of a Low-Noise 1.8 GHz CPPLL

This section begins with the implementation and design challenges of each PLL block, concludes with the demonstration of the PLL performance by means of test results.

4.1.1 Phase-Frequency Detector Design

A conventional PFD that was previously discussed in Section 3.1.1, Figure 33, is implemented in 0.18 μm TSMC (Taiwan Semiconductor Manufacturing Company) CMOS technology. The layout for the circuit with external reset feature is shown in Figure 34. This sequential PFD has a monotonic phase error transfer characteristic over the full clock-cycle (independent of the duty cycle). All of the subblocks are implemented by using static gates, and the transistors are sized optimally for a charge-

pump driven as the load. The operation of this circuit is shown in Figure 35 for the three possible input combinations: the VCO frequency leading the reference frequency, the VCO frequency lagging the reference frequency, and the VCO frequency in phase with the reference frequency. The figure shows rail-to-rail input signals for the PFD; however, the same proper operation is observed as long as the input-low voltage is below 0.45 V and the input-high voltage is above 0.9 V for a power supply voltage of 1.8 V.

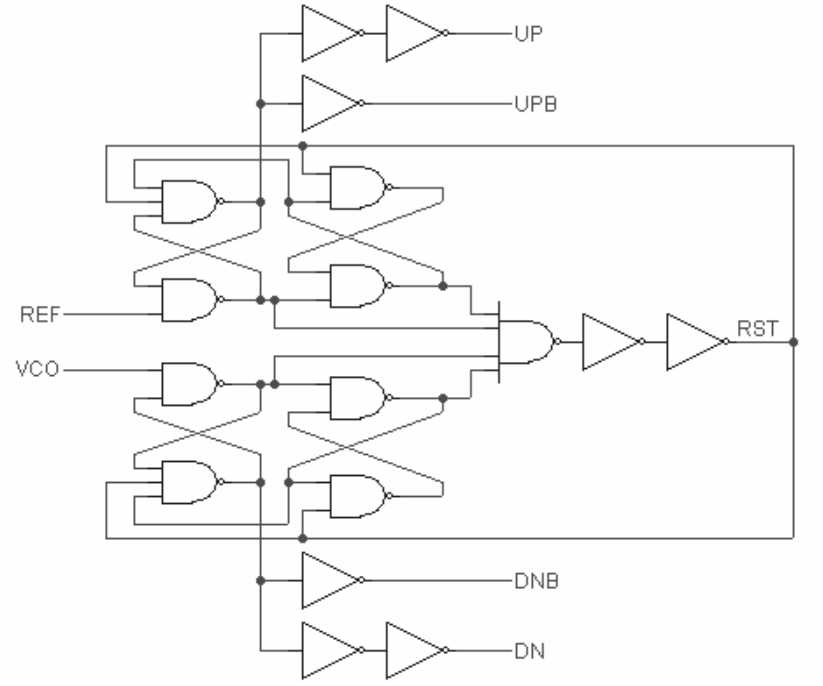


Figure 33: Phase-frequency detector schematic

The setup time in Figure 35 is 0.4 ns, and the reset pulse is 0.2 ns wide. The setup and reset delay of the PFD as a function of the supply voltage is shown in Figure 36. The setup delay varies from 0.5 ns to 2.5 ns, while the reset delay varies from 0.2 ns to 1.13 ns because of the increasing delay of the multiple-input gate on the feedback path. The maximum operating frequency of this PFD is simulated to be around 600 MHz (with

parasitics and the loading charge pump), and the delay between the output signals and their complements is less than 0.05 ns. The steady state characteristic for the dead-zone is discussed together with the charge pump in the next section.

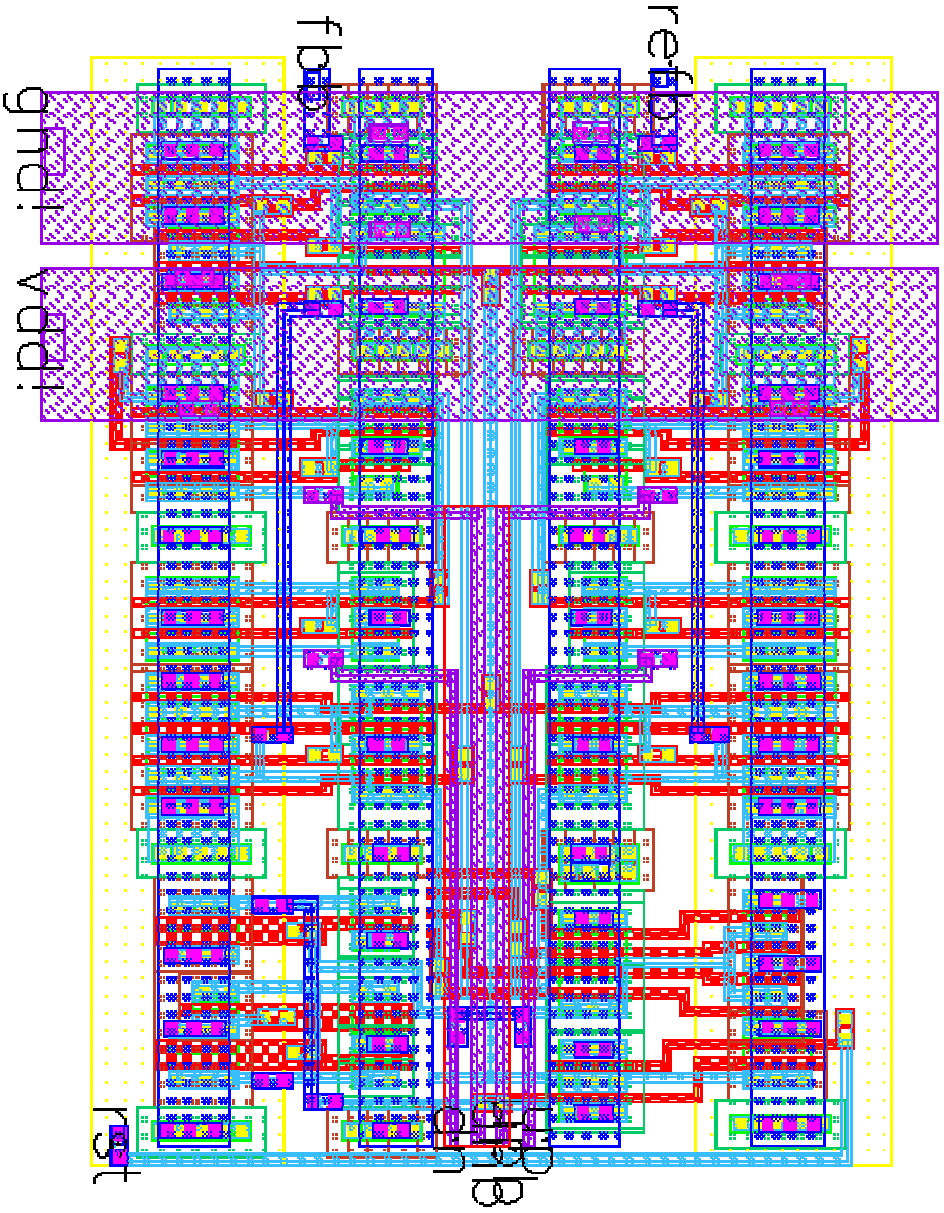


Figure 34: Phase-frequency detector layout

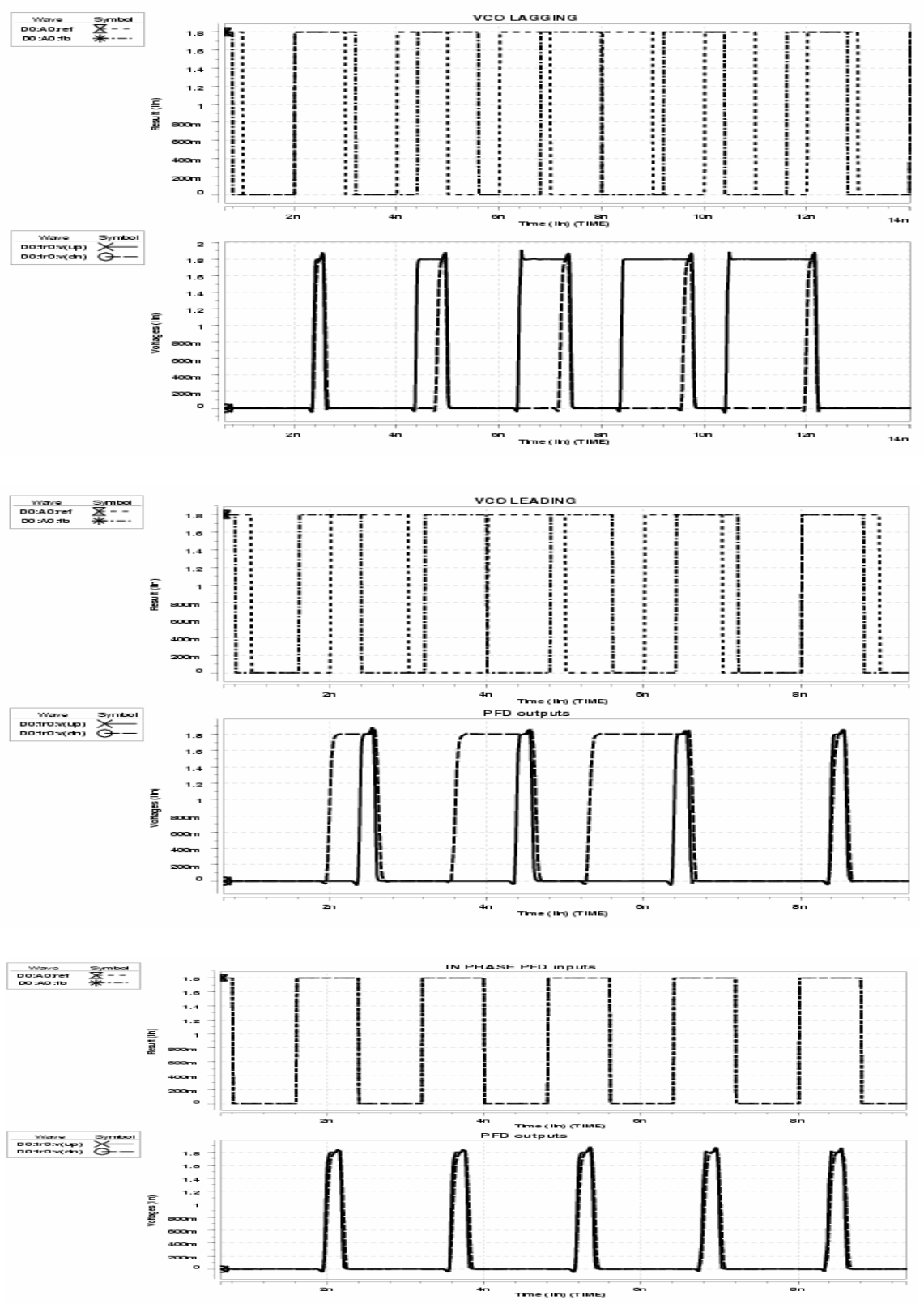


Figure 35: Phase-frequency detector operation

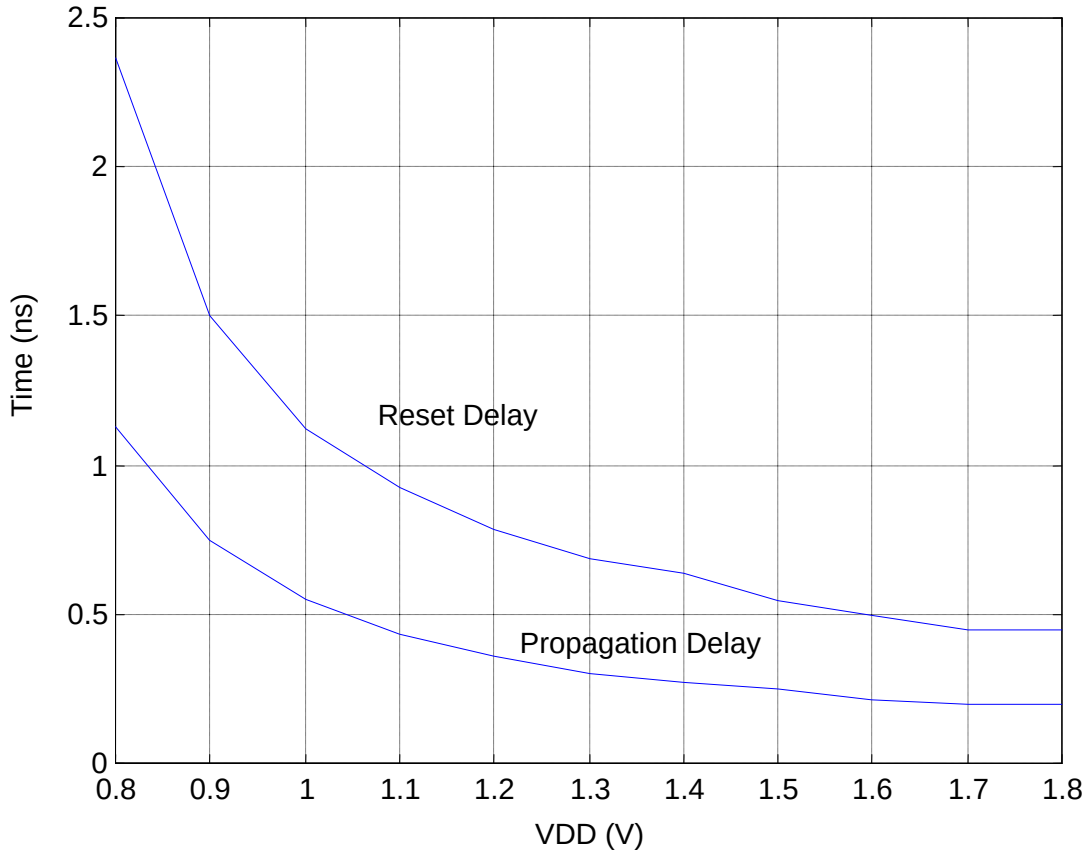


Figure 36: Reset delay and setup time variation with VDD

Since the internal nodes of the PFD are not completely pulled up or pulled down at high frequencies, high power consumption cannot be avoided. This is demonstrated in Figure 37. Note that the supply current is mostly negligible at low frequencies, whereas the static current is nonzero for high frequency operation. The average power versus the frequency is shown in Figure 38, where the average power is measured for orthogonal PFD inputs that have equal frequencies.

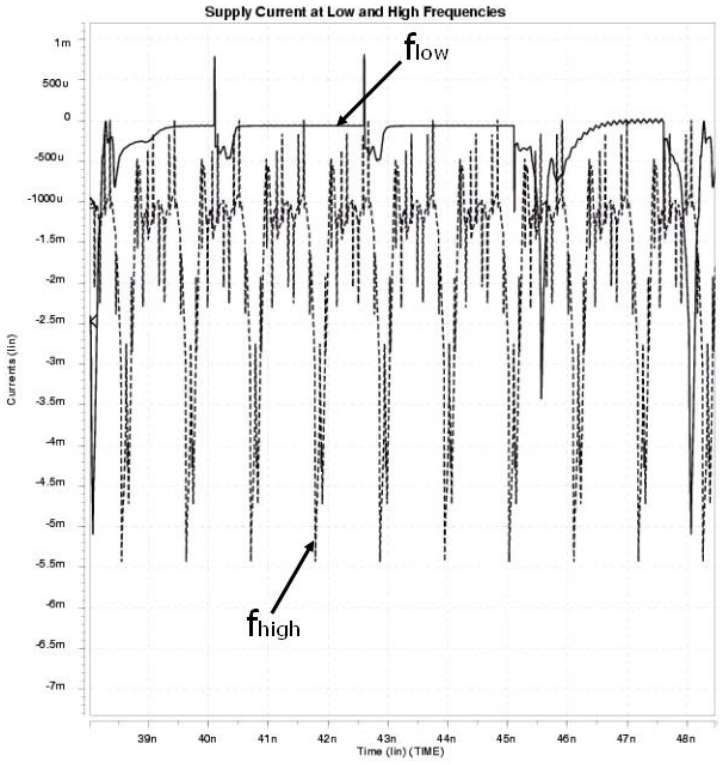


Figure 37: Supply current at low and high frequencies

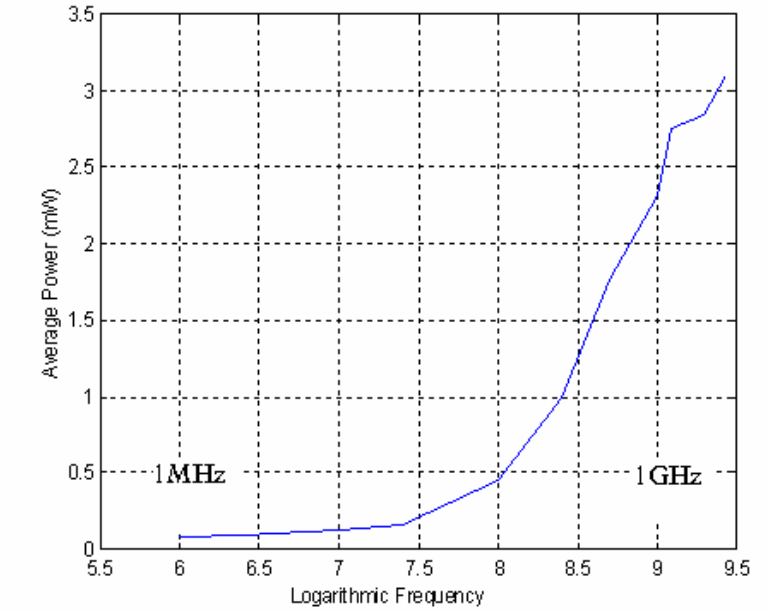


Figure 38: Average power versus frequency

4.1.2 Single-Ended Charge Pump Design

Zero static phase error can be achieved in a PLL as long as the PFD and the charge pump are ideal. The charge pump, however, shows non-ideal characteristics when implemented in CMOS. In a conventional charge pump, the switching transistors controlled by the UP and DN signals are directly connected to the output node. When the switches are turned off, the source voltages of the switches are pulled to each rail (VDD and GND). When one of the switches is turned on, the charges on the output capacitor would be shared with the charges at the respective internal node to induce glitches in the charge pump current. As discussed earlier, these glitches result in increased phase noise and power level of the PLL spurs. A new charge pump circuit, shown in Figure 39, was recently proposed by Hung et al [42] to reduce this charge-sharing problem. The order of the switching transistors and the current source transistors are reversed in this charging/discharging block. The current glitches now occur at the sources of the output transistors instead of their gates to turn them on softly with RC time constants at their sources. Moreover, the bypass capacitors C1 and C2 help to further attenuate the glitches by providing additional paths to ground. Two additional switches M14 and M15 are needed to reduce the fall time of the current pulses by providing low-impedance charging/discharging paths. These transistors, however, cause reverse currents at the output nodes, which results in a decreased output range (Figure 40). The reference current is generated on chip and a replica-biasing circuit is utilized to reduce the current mismatch in the current mirrors.

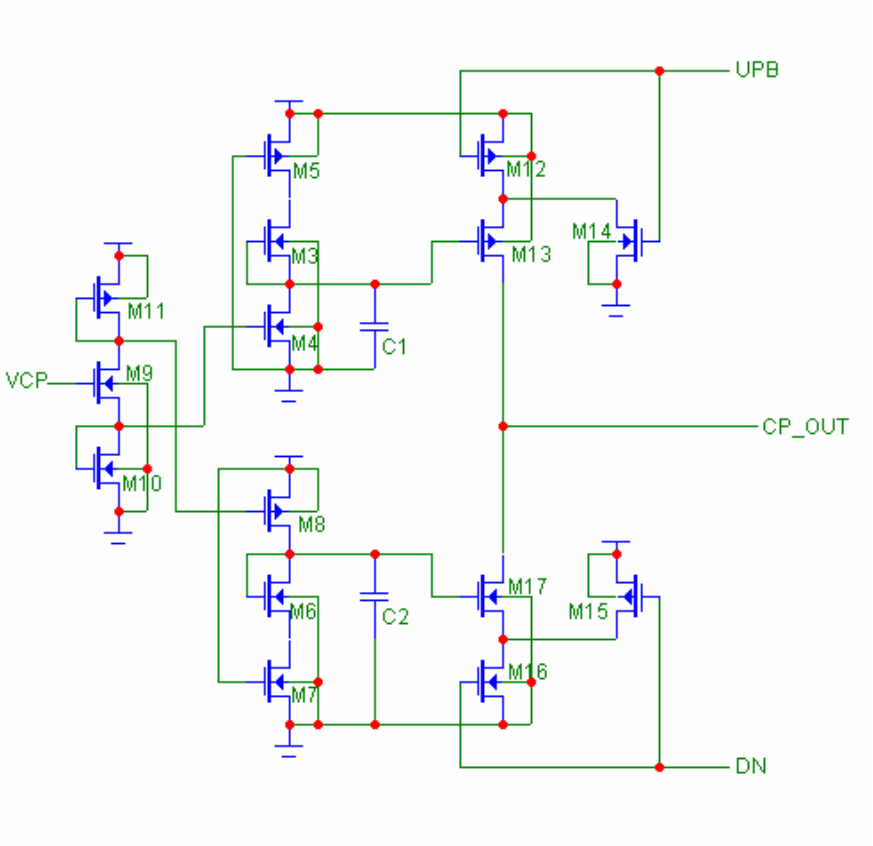


Figure 39: Circuit schematic of the single-ended charge pump

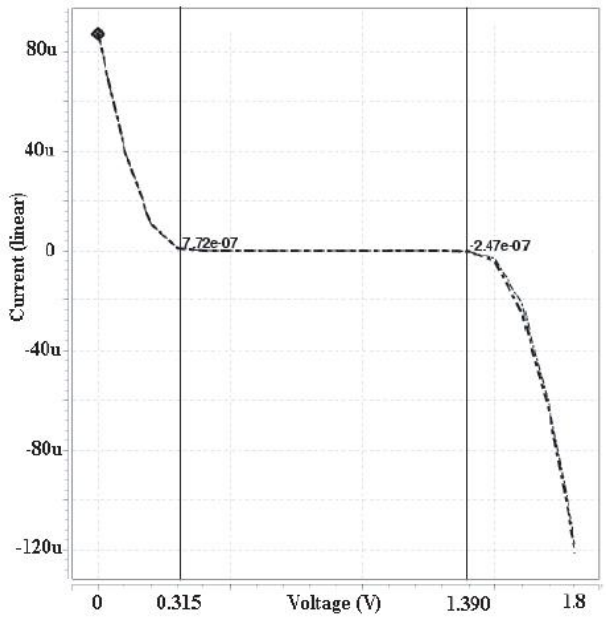


Figure 40: Charge pump output linear range

The PFD reset pulse width was simulated to be 0.2 ns in the previous section. The charge pump can charge and discharge the output node properly for an input pulse of 200 ps. This is demonstrated in Figure 41. A 200 ps discharging pulse followed by an equal width of a charging pulse bring the output voltage to its starting value. Figure 41 also shows the output current during this operation. It is extremely important not to detach the charge pump design and the PFD design to resolve the dead-zone problem. For example, if the charge pump could not respond properly to 200 ps pulses, the reset pulsewidth could have been increased by inserting extra inverters in the feedback path.

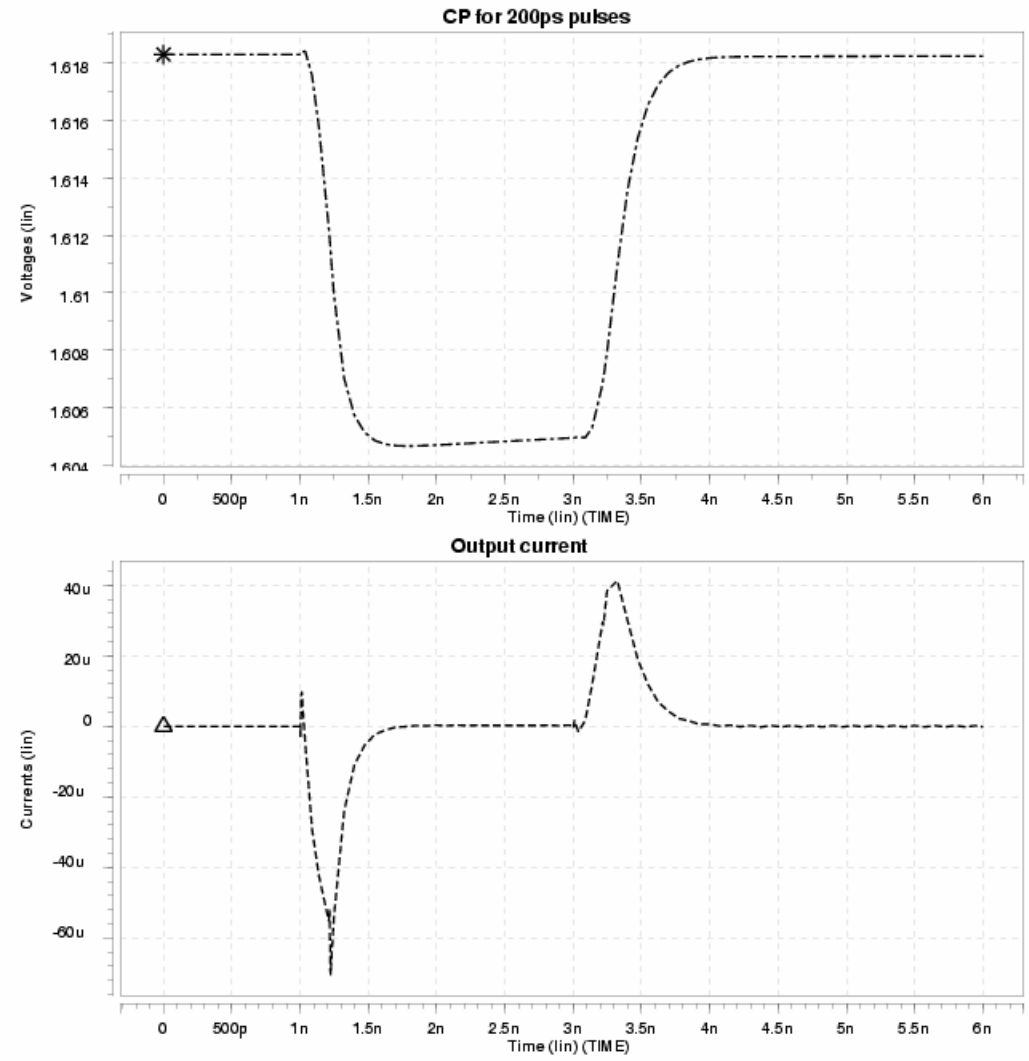


Figure 41: Charge pump response to 200 ps input phase difference

4.1.3 Differential Ring Oscillator with Single-Ended Control

An oscillator is a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal. A basic ring-oscillator consists of an odd number, *N,* of inverter stages connected in a positive feedback loop as shown in Figure 42. Suppose initial voltage at every node is equal to the trip point of the inverters. Assuming all stages are identical and there's no noise in the system, the system would remain in this state. However, this is not the case as noise sources disturb each node voltage, yielding a growing waveform. Eventually, the waveform on each node is a larger voltage swing. The frequency of the oscillation for an N-stage system will be $1/(2NT_d)$ where T_d is the propagation delay of a single stage.

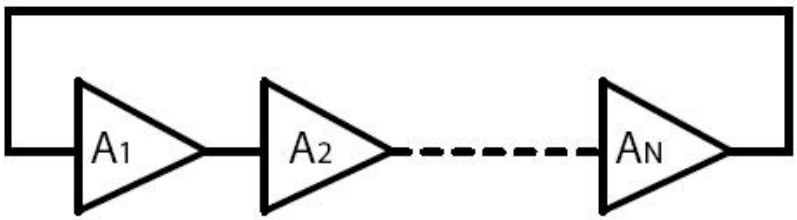


Figure 42: Ring oscillator using delay stages

Ring-oscillators are widely used in communications systems due to their simplicity, wide tuning-range and ease of implementation. Thus, various optimization and circuit design techniques that can improve their performance are well studied [43].

The most important parameters in the VCO design are phase noise, jitter, center frequency, tuning range, and linearity. The tuning range is the range of frequencies bounded by the maximum and minimum oscillation frequencies. A linear VCO gain is desirable because the tuning nonlinearity degrades the settling behavior of phase-locked

loops [44]. Important concerns in the design of low-jitter VCOs are the variations of the output phase and frequency as a result of noise on the control line and the power supply.

Delay Stage

A differential delay stage is employed in order to achieve good power supply noise rejection. Figure 43 shows a saturated delay stage with cross-coupled PMOS load. The regenerative PMOS transistors provide rail-to-rail output signals via the full switching of the FETs. The latch circuitry reduces the delay of the stage, allowing higher frequency of operation. The full switching of the transistors also reduces the flicker noise [34].

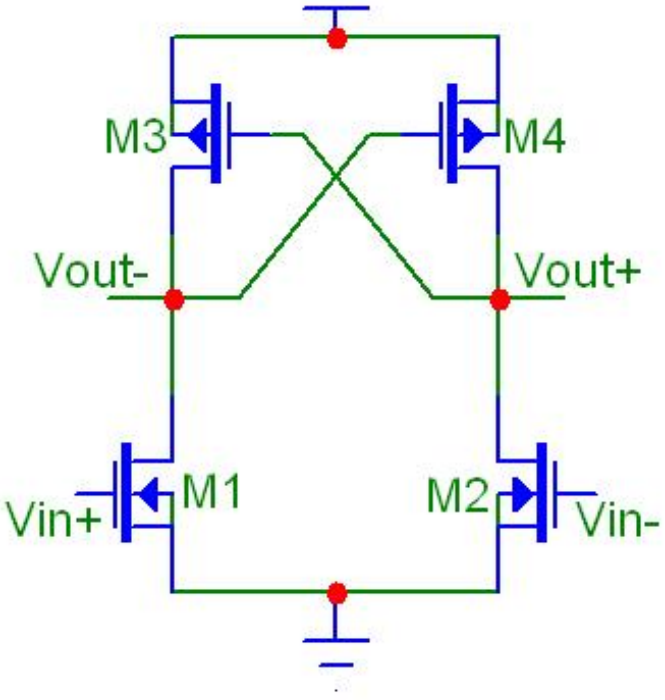


Figure 43: Saturated delay stage with cross-coupled PMOS load

Next, a delay control option needs to be built-in for the given delay stage. The most common approach is to include a tail current source, demonstrated in Figure 44.

However, this design does not only limit the signal swing, but also results in excessive noise due to the upconversion of the tail transistor low-frequency noise near the oscillation frequency [6, 8].

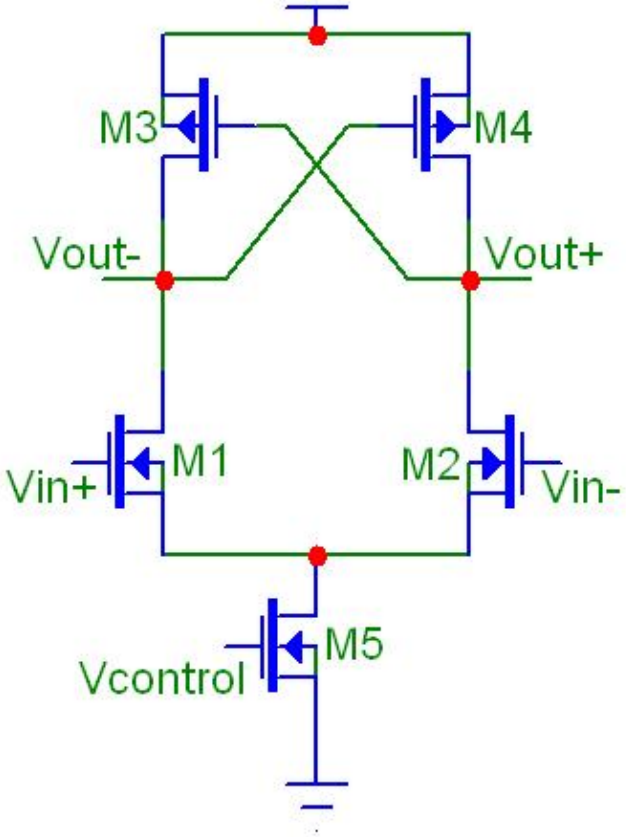


Figure 44: Saturated delay stage with tail current control

The tuning method chosen for implementation is controlling the strength of the latch [45, 46]. This can be accomplished by inserting MOS resistors in the feedback path as shown in Figure 45. Increasing the gate voltages of M3 and M4, reduces the FET resistance, increasing the positive feedback gain of the latch. This makes it harder to switch the output nodes, thus increasing the stage delay. Similarly, decreasing the control voltage increases the oscillation frequency. The feedback resistors require very careful

sizing, because there is a design tradeoff between the tuning range and linearity. Increasing the resistive FET sizes allows the feedback to get relatively stronger to increase the frequency tuning range at the low-end. A slight degradation in maximum frequency may be observed due to the increased parasitic capacitance at output nodes with bigger FETs. In contrast, smaller resistive FETs decrease the tuning range while resulting in a more linear characteristic.

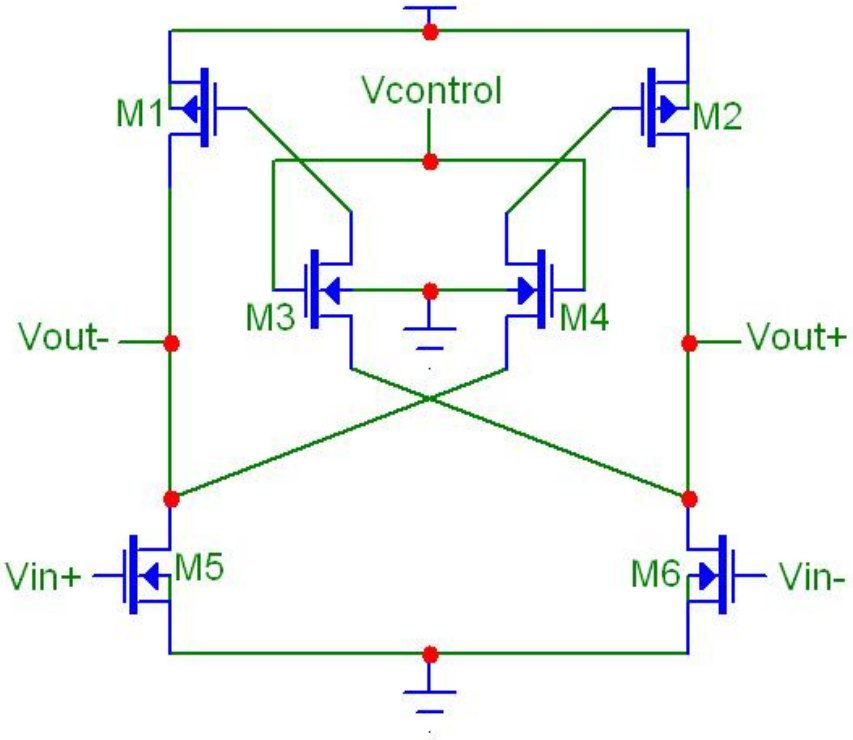


Figure 45: Saturated delay stage with latch strength control

Architecture

A multiple-pass loop architecture adds auxiliary feedforward loops that work in conjunction with the main loop [37, 47]. This architecture reduces the delay of the stages below the smallest delay possible in a conventional loop.

A pair of inputs can be added to the saturated delay stage, depicted in Figure 46, to employ the designed delay stage in a multiple-pass oscillator architecture. Transistors M5 and M6 build the main loop, while M7 and M8 are the secondary transconductance stages. The secondary inputs need to be weaker than the main loop to increase the oscillation frequency without disturbing the proper operation.

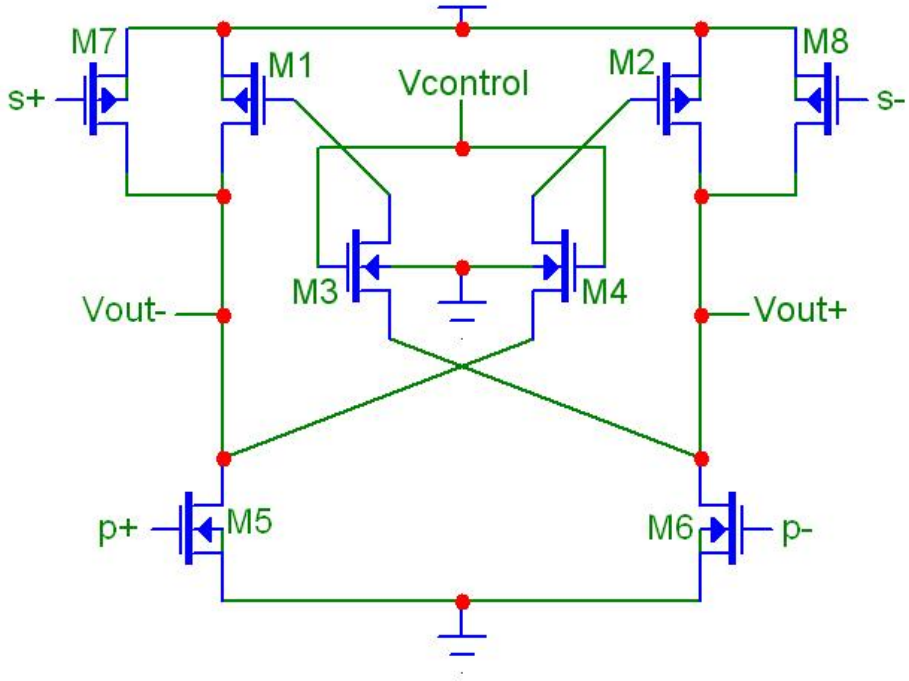


Figure 46: Saturated delay stage with secondary differential control

(P-, P+) and (S-, S+) stand for the primary and secondary differential inputs for the gain stage, respectively. This architecture is identified as the look-ahead ring oscillator by Mneatis [48].

A 9-stage multiple-pass ring oscillator is utilized in this work. Auxiliary feedforward paths are formed by passing over one stage, shown in Figure 47. The layout for the 9-stage ring in TSMC's 0.18 μm technology is also shown in Figure 48.

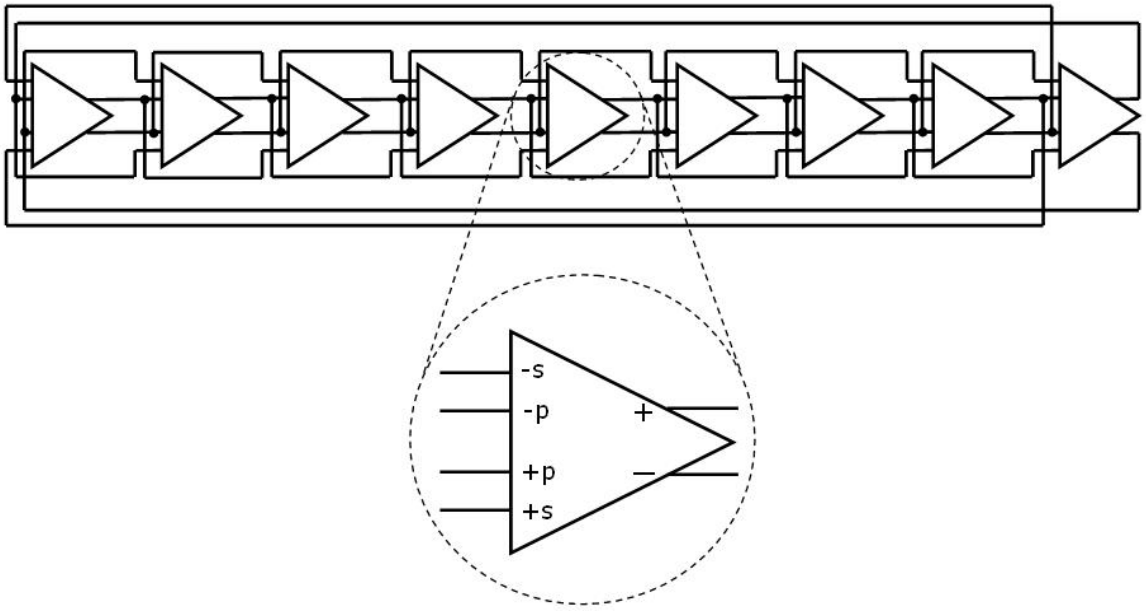


Figure 47: 9-stage multiple-pass ring oscillator architecture

The transistor sizing for the delay stage utilized in this architecture is shown in Table 3 for TSMC's 0.18 μm process.

Table 3: Transistor sizing for the saturated delay stage

Transistor	Width (μm)	Length (μm)
M1, M2	27	0.2
M3, M4	0.6	0.4
M5, M6	36	0.2
M7, M8	16	0.2

It is important to note that this oscillator has a single ended control, however it is constructed by differential delay elements. Employing differential stages yields 50% duty cycle, thus improving the spectral purity of the output frequency.

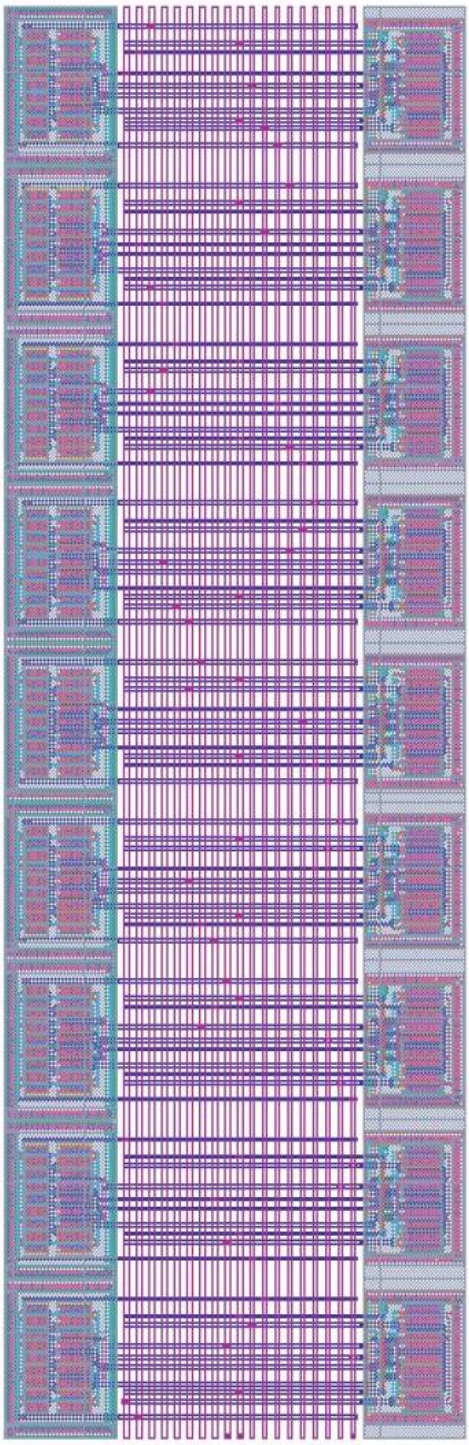


Figure 48: 9-stage multiple-pass ring layout

Simulation and Measurements

Simulation and measurement results were used to extract the voltage-frequency characteristic curves in Figure 49. The two curves show good agreement where a maximum difference is 4%. The power consumption of the oscillator changes from 92 mW to 112 mW within the tuning range that is simulated to be 1.16 GHz to 1.93 GHz. The measured silicon output tunes from 1.1 GHz up to 1.86 GHz for the same control voltage range. The voltage-frequency curve is fairly linear for an input range of 0.9-1.8 V.

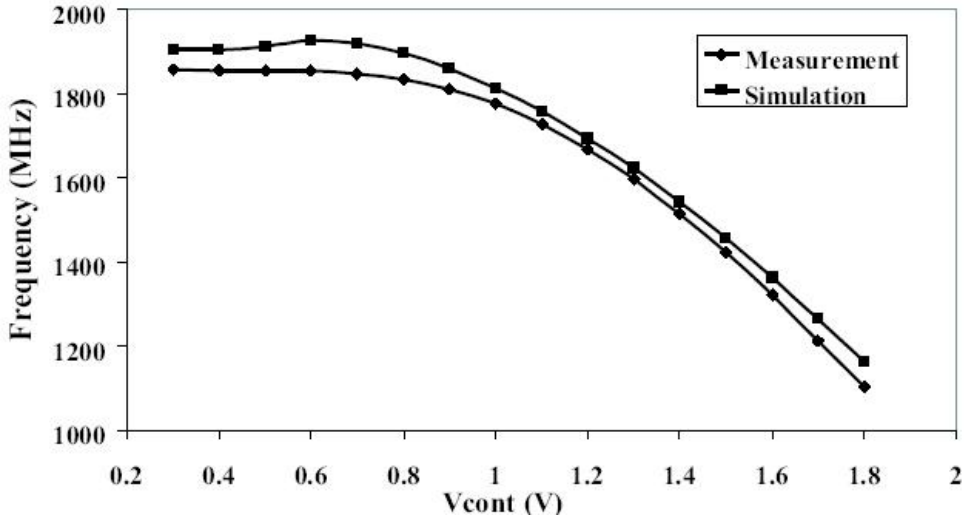


Figure 49: 9-stage VCO characteristic

The phase noise is estimated by SpectreRF [49] simulations as -112.84 dBc/Hz at 1 MHz offset from a 1.82 GHz center frequency. The measurement result at the same operating point is extracted as -105.5 dBc/Hz. This number is obtained by using the measurement of divide-by-two output spectrum shown in Figure 50. From the divided output data, the phase noise of the ring oscillator can be found using the equation

$$L(\Delta f) = SB - 10\log(RBW) - 20\log\left(\frac{\Delta f}{\Delta f_m}\right) + 20\log\left(\frac{f_o}{f_m}\right) \quad \textbf{(38)}$$

where L(Δf) is the phase noise at a phase offset of Δf from a center frequency of f_o extracted from a sideband noise measurement (SB) at Δf_m offset from f_m. The resolution bandwidth (RBW) of the spectrum analyzer appears in the equation, because more noise is included in the analyzed spectrum with increasing bandwidth.

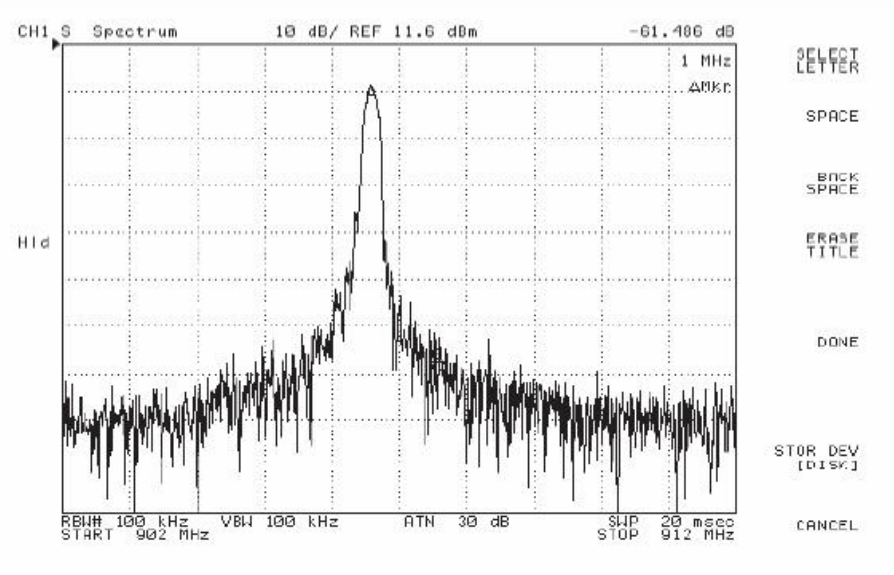


Figure 50: Measured 9-stage VCO spectrum at ½ output

4.1.4 Auxiliary circuits

The auxiliary circuitry (Figure 51) designed for the oscillators include dividers, buffers, enable switches, and differential to single-ended converters (DTOS). Dividers are needed to construct a closed phase-locked loop and also to ease the requirements on the testing equipment. The oscillator enable switches are included to disable certain parts on the die, reducing the electrical coupling. The buffers are utilized to optimally drive bigger loads without degrading the circuit performance. The DTOS blocks convert

differential signals to single ended for common-mode noise rejection. Also, testing single-ended signals is more trivial and the designed PFD does not require differential input signals.

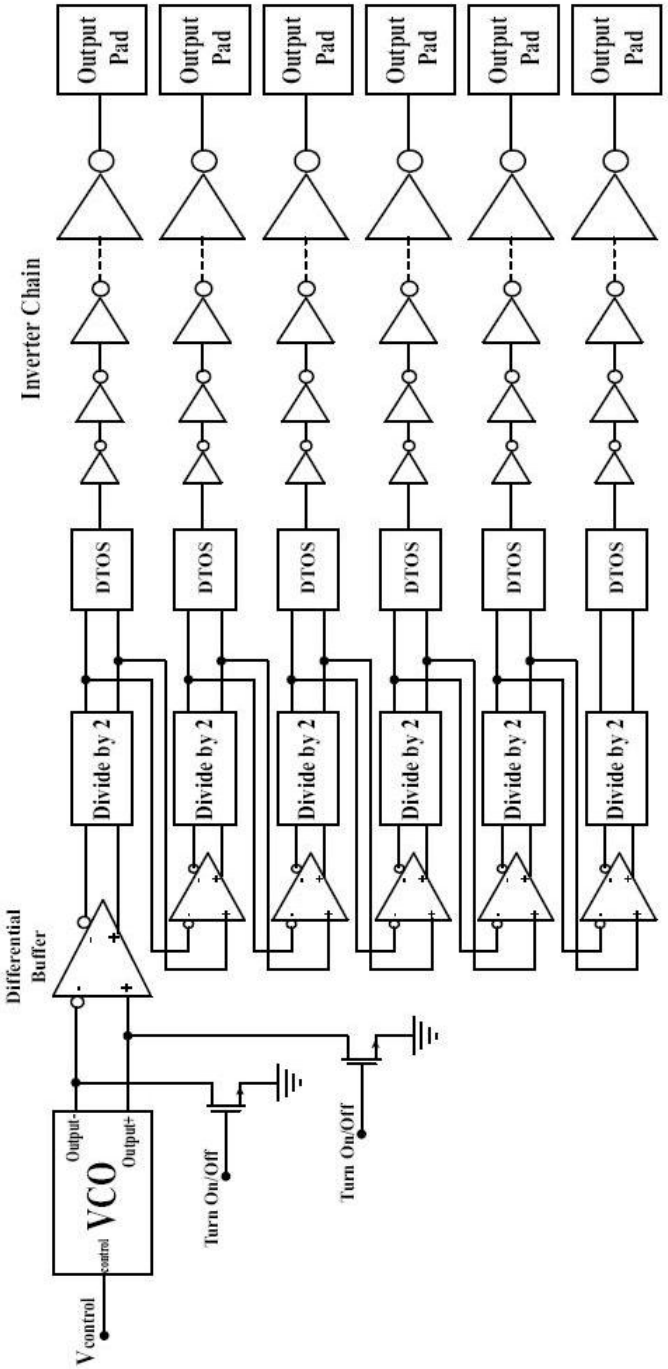


Figure 51: VCO auxiliary circuitry

The divider (divide-by-2) is simply built with a D-flip-flop (DFF) whose inverted output is fed back into the data input as shown in Figure 52. The master-slave DFF is composed of two differential multiplexers, as depicted in Figure 53. The differential multiplexers are built with resistors instead of PMOS loads and current-mode logic is utilized for speed (Figure 54).

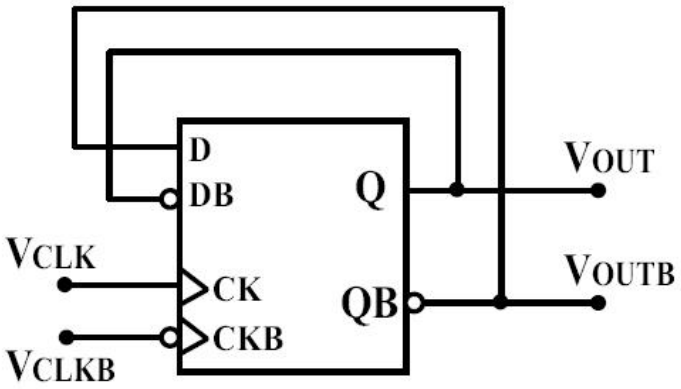


Figure 52: Divide-by-2 schematic

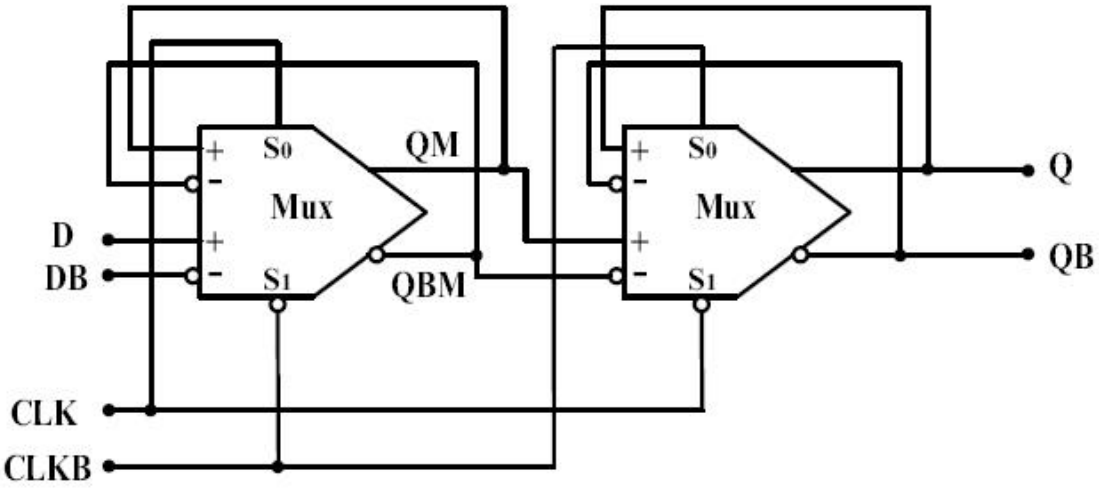


Figure 53: DFF schematic

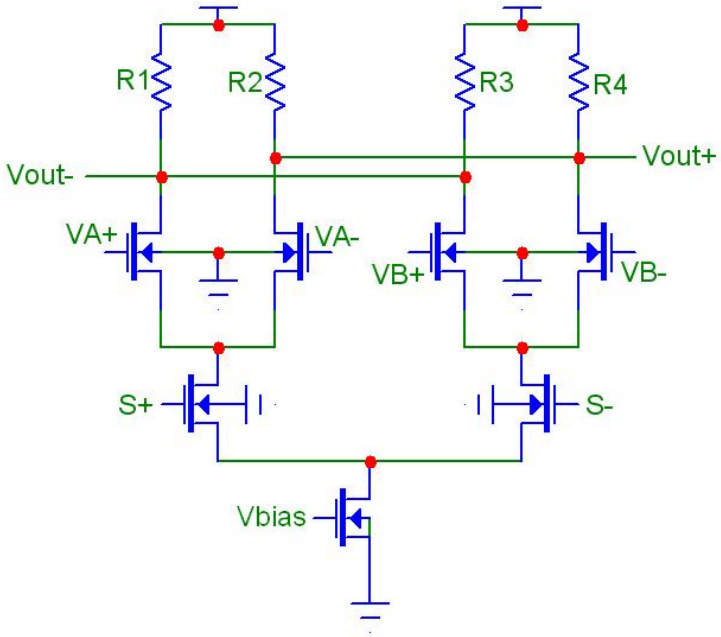


Figure 54: Current-mode multiplexer schematic

The schematic for the high-speed front-end differential buffer is given in Figure 55. The buffers, followed by the dividers, are designed to operate up to 6+ GHz.

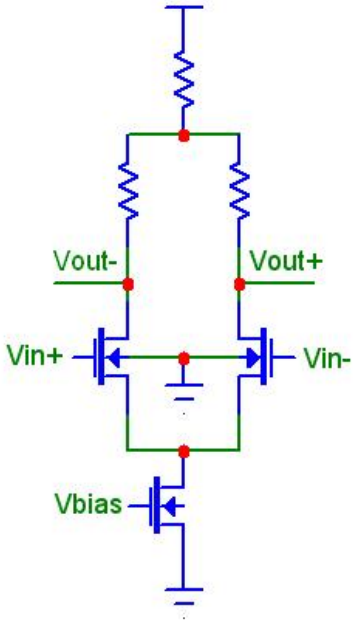


Figure 55: Current-mode buffer schematic

The down-converted oscillator outputs (divided by 2, 4, 8, 16, 32, 64) are converted to single ended signals before driving the output pads through inverter chains. The differential to single-ended conversion is done by the DTOS block demonstrated in Figure 56. The differential input pair converts the input voltage into differential current signals, which are then folded and merged to form a single-ended voltage.

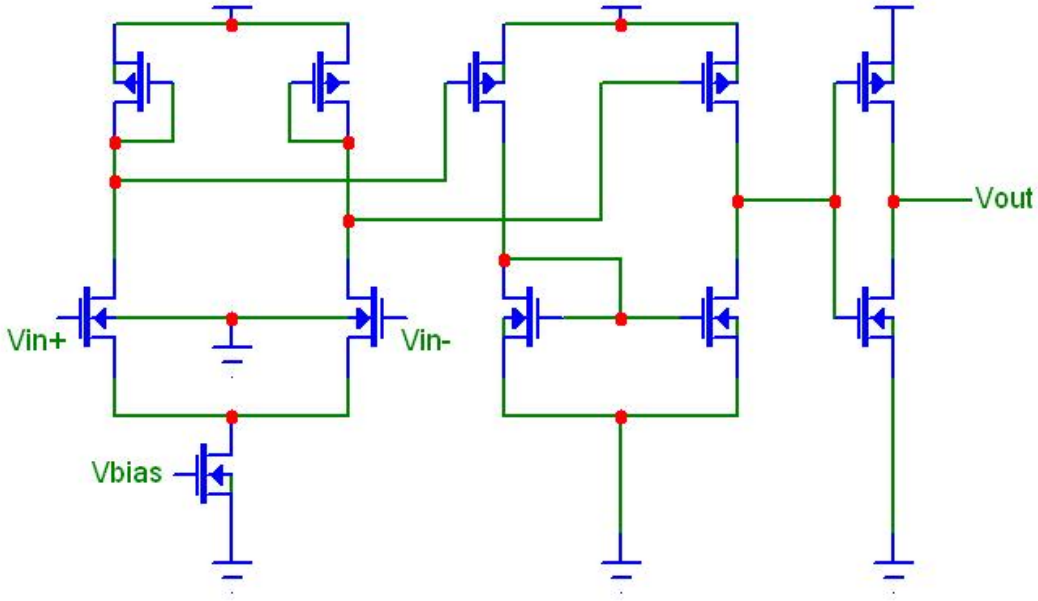


Figure 56: Differential to single-ended converter

Electrostatic discharge circuits and DC bias capacitors are also designed to finalize the oscillator design. The layout for the 9-stage ring oscillator and the auxiliary blocks is given in Figure 57.

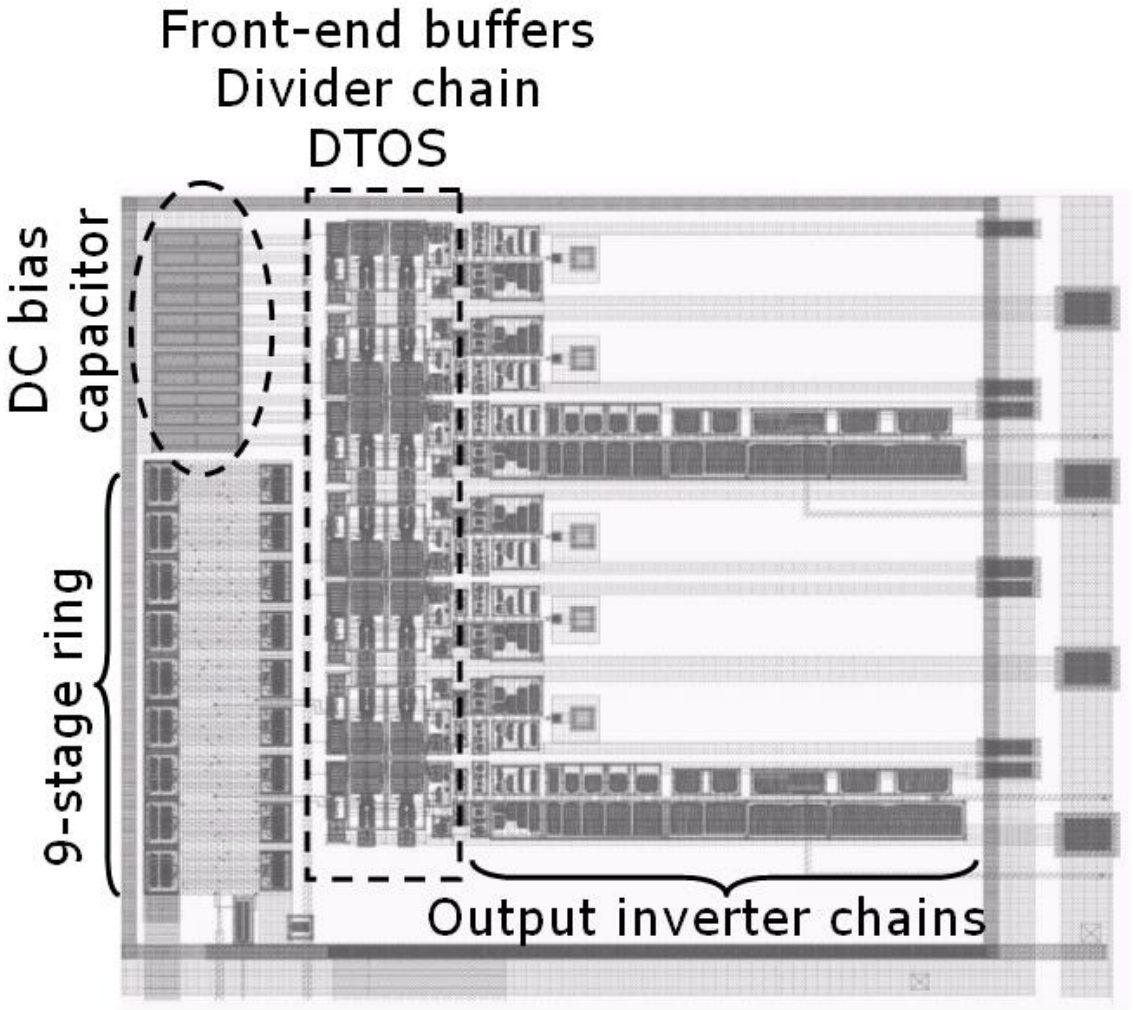


Figure 57: 9-stage VCO layout

4.1.5 PLL Test Results

Oscillator characterization is followed by the construction of the control loop shown in Figure 58. An external loop filter is employed to have some form of flexibility within the PLL system without another pass of the silicon.

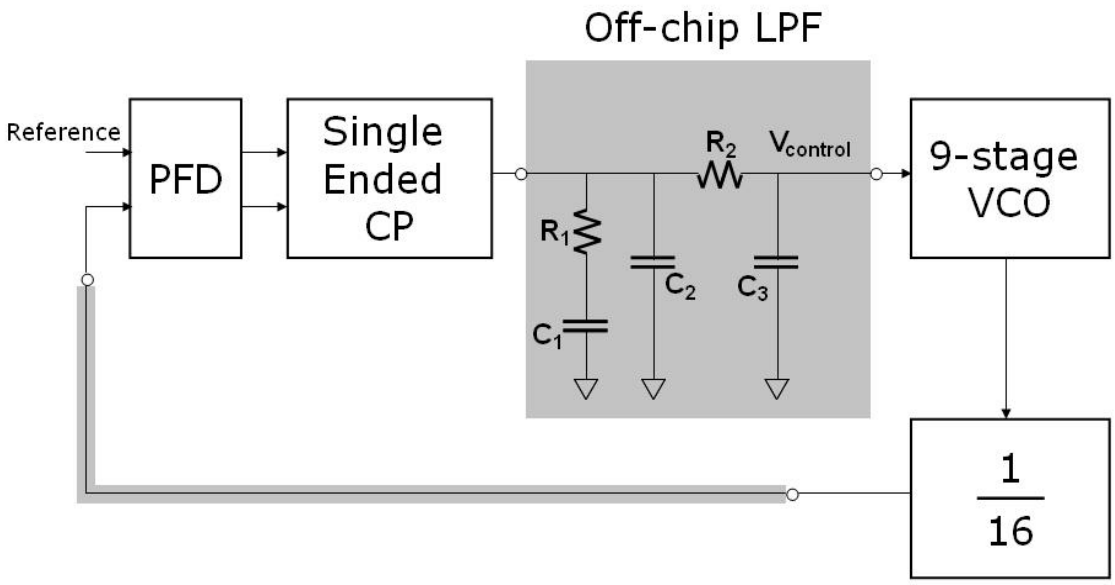


Figure 58: Single-ended PLL test setup with 9-stage VCO

The maximum operating frequency of the PFD/CP blocks is measured as 500 MHz. The division ratio, N=16, on the feedback path guarantees the proper phase comparison by limiting the input range from 74 MHz to 115 MHz. The first-order loop filter is designed for a bandwidth around 600 KHz (R1= 680 Ω, C1= 0.01 μF, C2 = 50 pF).

Divider outputs running above 100 MHz generated an output-high voltage at 2.5 V and an output-low voltage at 1.5 V. Thus, the feedback input of the PFD could not be pulled-down below its input-low voltage, causing improper operation by flattening out

the VCO frequency at its maximum. This problem with the voltage levels was solved with 100 Ω pull-down resistors connected to the divider outputs.

The loop is then tested for lock-in properties over the oscillator range. The lock-in range of the PLL was slightly narrower than the corresponding VCO operation range since the control voltages could not move out of the [0.2 V, 1.6 V] interval.

Table 4 summarizes some measurement results at 1.8 V power supply and ambient temperature.

Table 4: The 1.8 GHz PLL measurement summary

PLL with 9-stage ring VCO	
VCO Range (MHz)	1120 - 1860
Lock-in Range (MHz)	124.4 – 128.5
Internal Freq. (MHz)	1180 - 1840
Division Ratio	16
VCO Gain (MHz/V)	770
I_{CP} (μA)	100
Open-Loop Phase Margin	81
Closed-Loop BW (KHz)	625.5
RMS jitter (ps)	1.7
Phase Noise (-dBc/Hz)	116

4.2 Design of a Low-Noise 5.8 GHz Charge-Pump PLL

This section aims to prove that single-ended CPPLLs are useful in today's multi-GHz applications such as 10 Gbps Ethernet (Figure 59). A virtual 10 Gbps overall transfer rate using two samplers with a serial input data stream requires low noise PLLs at 5 GHz. In order to show that these specifications are achievable in 0.18 μm CMOS, the maximum lock-in frequency is next investigated using the same control scheme and a 3-stage ring oscillator for maximum speed.

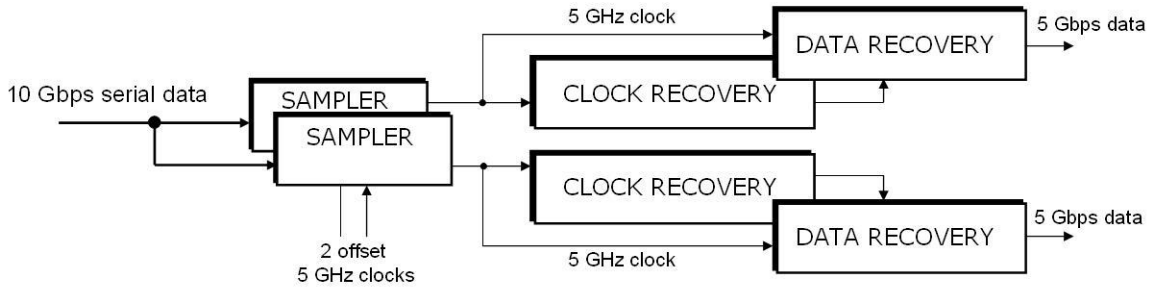


Figure 59: 10 Gbps Ethernet architecture

4.2.1 Ring Oscillator for Maximum Speed

The frequency of the oscillation for an N-stage system is already mentioned to be $1/(2NT_d)$ where T_d is the propagation delay of a single stage. Although it is possible to build two stage oscillators [13, 50, 51], the minimum number of stages to sustain a stable oscillation is three. For a 3-stage ring oscillator, the maximum frequency depends on the minimum delay of a single stage. A fast delay stage is already described in Section 4.1.3. How the multiple-pass ring architecture can improve the oscillation frequency is discussed in the design of a 9-stage oscillator. In this section, the saturated delay stage will be employed in a 3-stage multiple-pass ring oscillator to achieve maximum operating

frequency (Figure 60). The layout for this ring is given in Figure 61. This ring is used with the auxiliary circuitry, which was described earlier with the 9-stage oscillator, as shown in Figure 62.

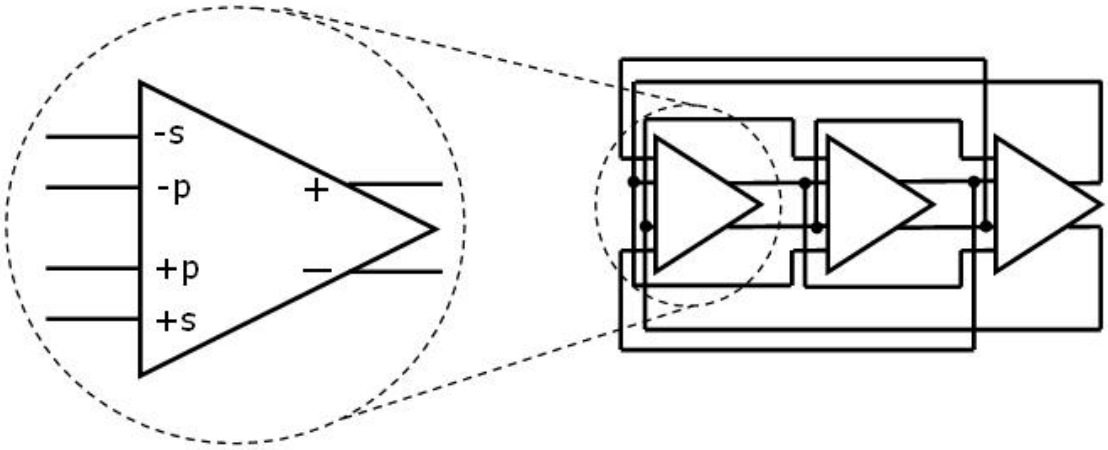


Figure 60: 3-stage multiple-pass ring oscillator architecture

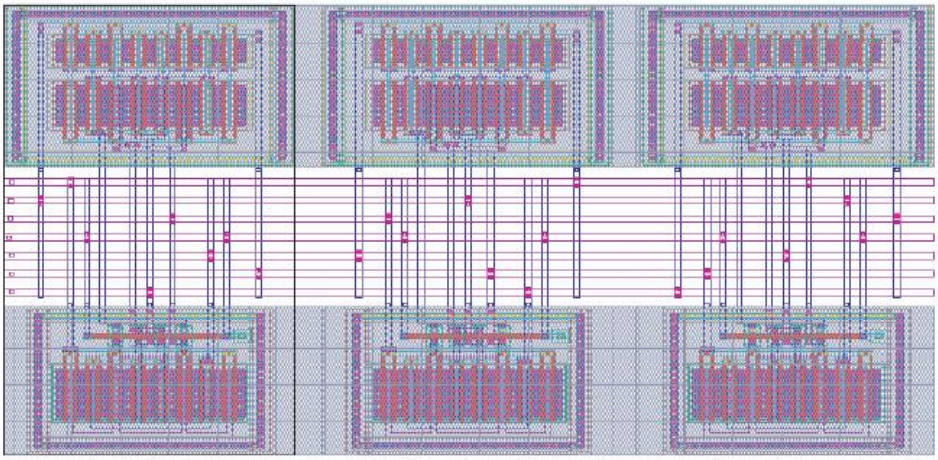


Figure 61: 3-stage multiple-pass ring layout

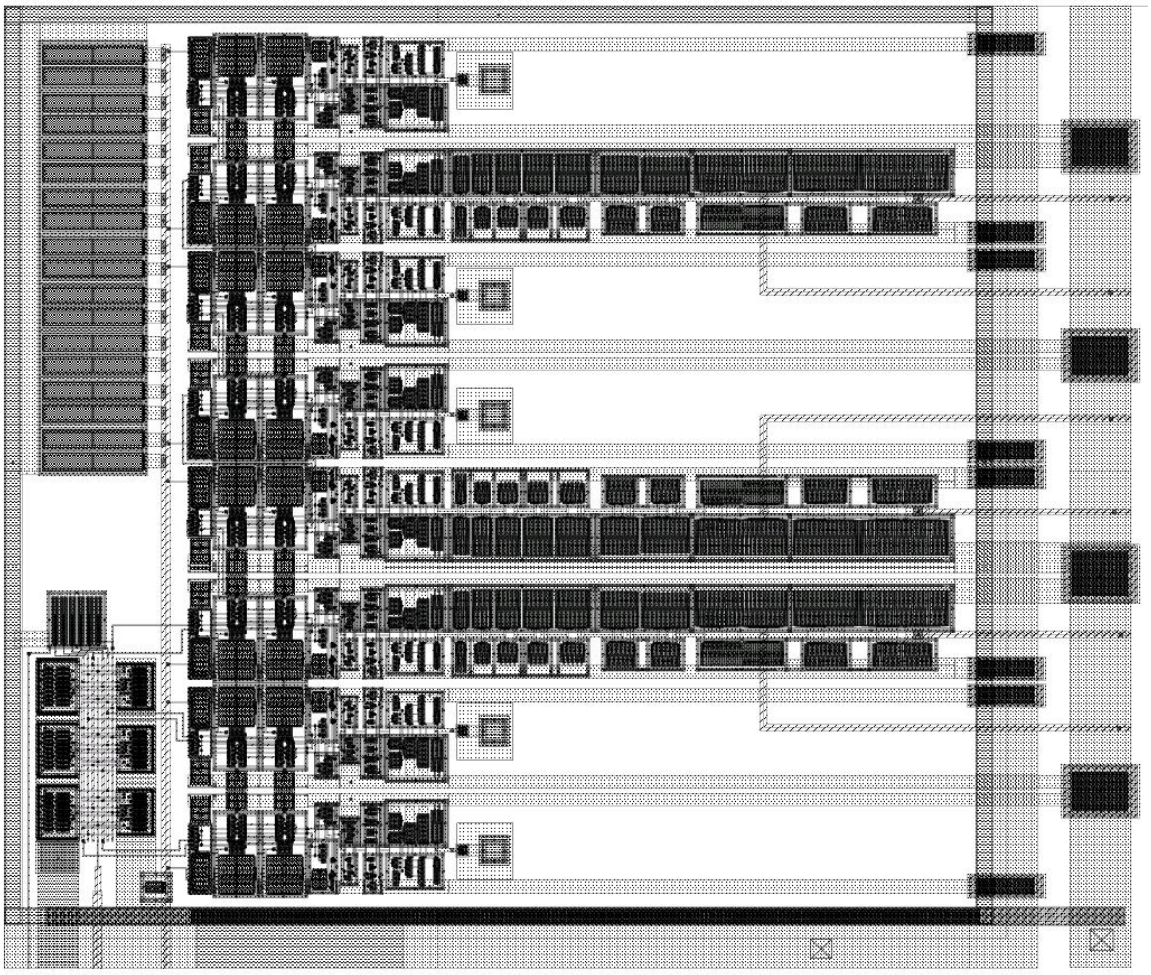


Figure 62: 3-stage VCO layout

Simulation and Measurements

Simulation and measurement results are presented in Figure 63. The two curves agree to within 3%. The power consumption of the oscillator changes from 40 mW to 50 mW within the tuning range that is simulated to be 5.18 GHz to 6.11 GHz. The measured silicon output tunes from 5.35 GHz up to 6.11 GHz for 0.3-1.8 V control range.

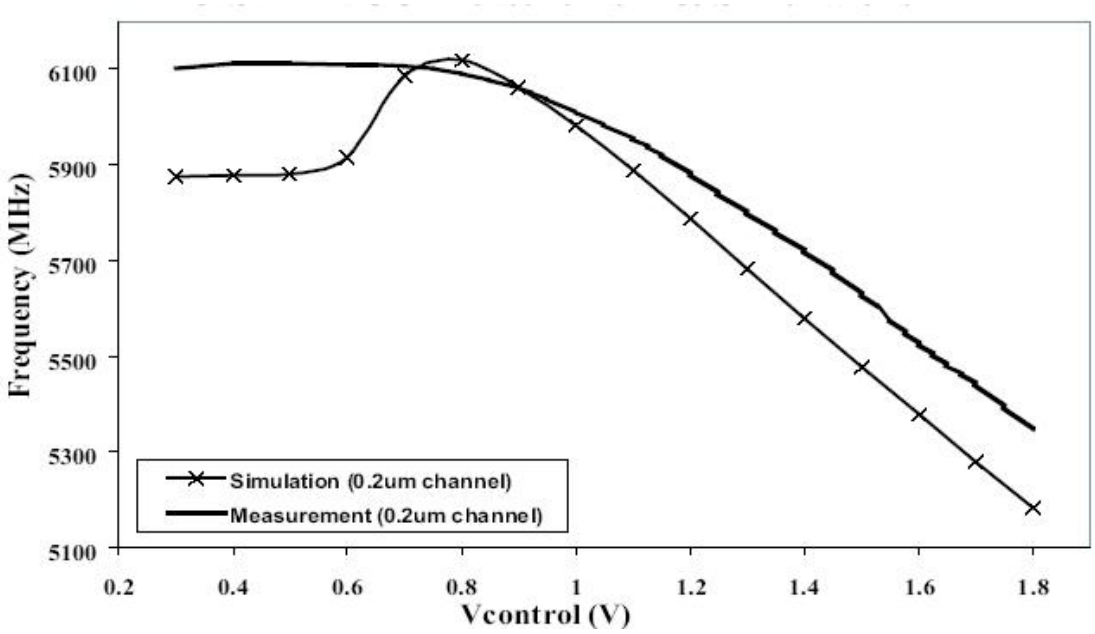


Figure 63: 3-stage VCO characteristic

SpectreRF simulations estimate the phase noise as -99.5 dBc/Hz at 1 MHz offset from a 5.79 GHz center frequency, as illustrated in Figure 64. The measurement result at the same operating point is extracted as -99.4 dBc/Hz by using the measurement result in Equation 38. The spectrum measurement at the divide-by-four output of the 3-stage VCO is shown in Figure 65.

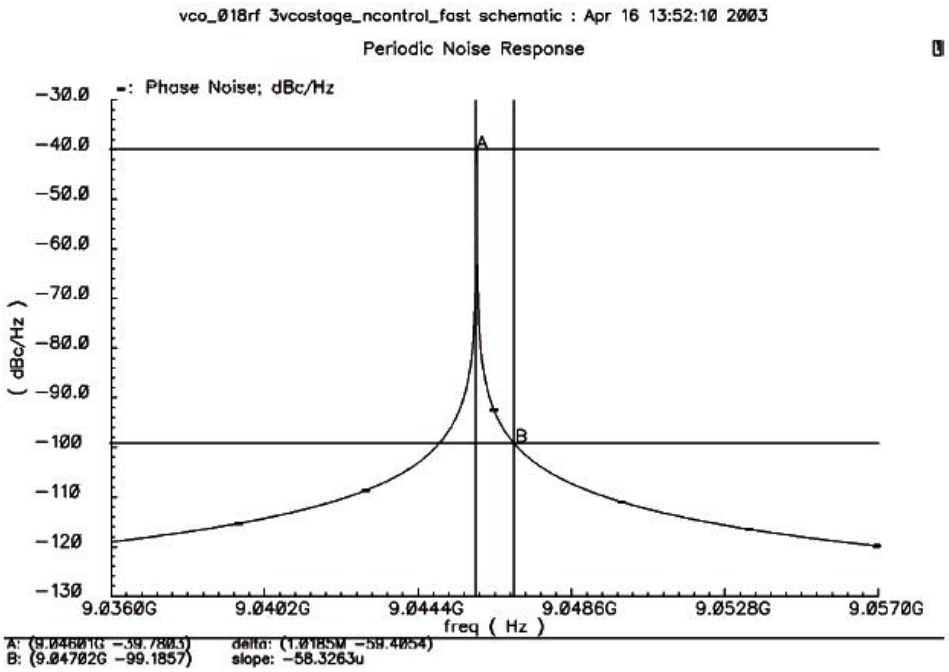


Figure 64: Phase noise simulation at 5.79 GHz center frequency

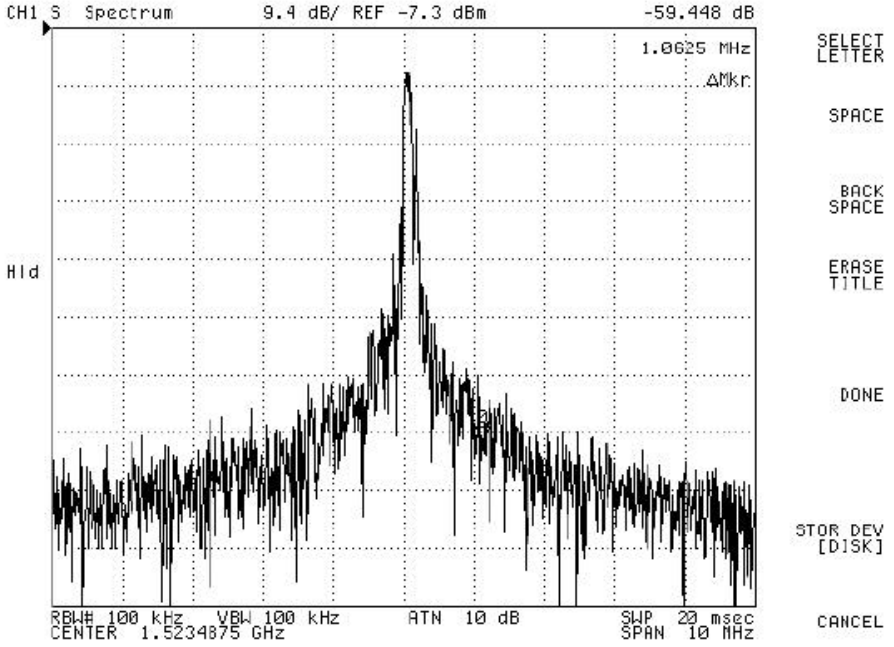


Figure 65: Measured 3-stage VCO spectrum at ¼ output

4.2.2 PLL Test Results

The same PFD, single-ended charge pump, external loop filter and divider blocks are utilized to build a PLL that can internally run up to ~6 GHz. The testing block diagram is given in Figure 66. The feedback division ratio of the loop is set to 32 to guarantee the proper phase comparison by limiting the input range to 166-182.5 MHz.

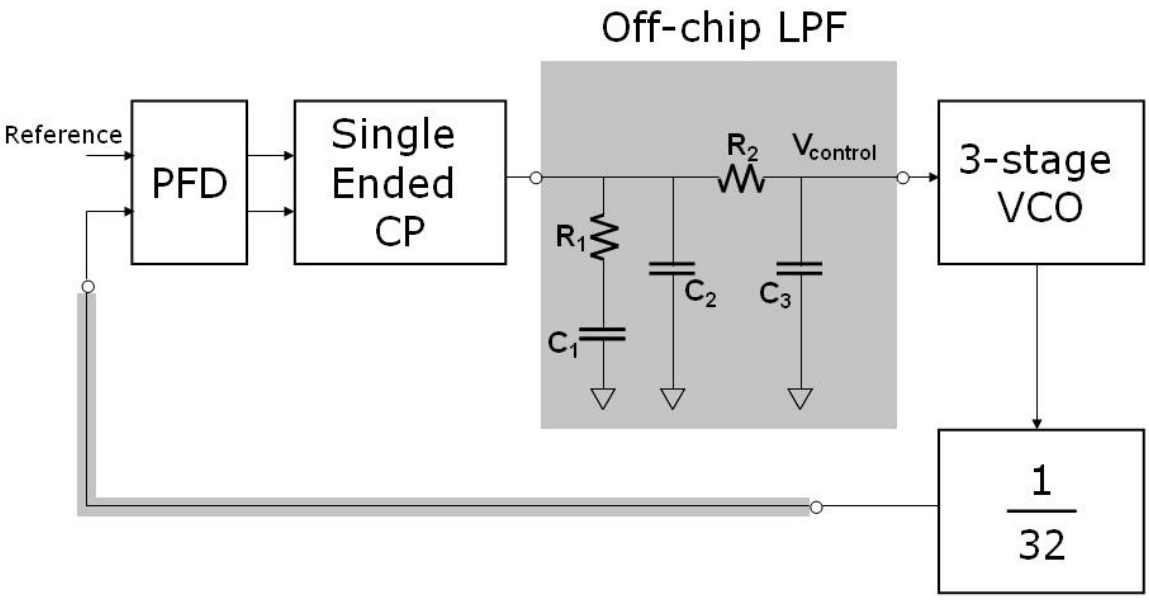


Figure 66: Single-ended PLL test setup with 3-stage VCO

Table 5 summarizes some measurement results at 1.8 V power supply and ambient temperature. These results show that the single ended CPPLL architecture that employs ring oscillators can serve as a timing solution in multi-GHz data communication applications.

Table 5: The 5.8 GHz PLL measurement summary

PLL with 3-stage ring VCO	
VCO Range (MHz)	5162 - 5930
Lock-in Range (MHz)	166 - 182.5
Internal Freq. (MHz)	5310 – 5840
Division Ratio	32
VCO Gain (MHz/V)	793
I_{CP} (μA)	100
Open-Loop Phase Margin	73.4
Closed-Loop BW (KHz)	248.4
RMS jitter (ps)	2.6
Phase Noise (-dBc/Hz)	110

CHAPTER V

DIFFERENTIAL CONTROL FOR MULTI-GHz CPPLLs

Most of the differential oscillators in literature utilize a single-ended control line, as in the PLLs in Chapter IV. The advantage of a single-ended control line is the reduction of area and power. It is, on the other hand, very critical to examine the performance of a differential control in high performance PLLs.

This chapter describes the design of low-jitter differential CPPLLs in a standard submicron CMOS process through a 2.5 GHz PLL design. Due to the fact that a differential path requires more power, an LC oscillator is used to gain headroom in power consumption.

In this chapter the challenges in differential control path design are addressed. Differential oscillator control typically requires the use of a differential charge pump and an extra loop filter. The exceptionally performing charge pump in the single-ended loop is next developed for a fully differential PLL. The differential charge pump design, however, is not an easy task, because it requires a common-mode feedback (CMFB) correction scheme. Then, an LC oscillator with differential fine-tuning is described. The chapter is concluded with PLL measurement results; the analysis/comparison for the designed PLLs is left to the next chapter.

5.1 Design of a CPPLL with differential control

5.1.1 Differential Charge Pump Design

A differential charge pump, whose advantages over single-ended charge pumps were discussed in Section 3.2.2, is designed next. A differential charge pump can utilize the single-ended charging/discharging block for low charge sharing and low charge injection if pulsed as shown in Figure 67. The clocking of the switches in the figure guarantees to decrease one of the node voltages while increasing the other and to keep them unchanged in case of lock.

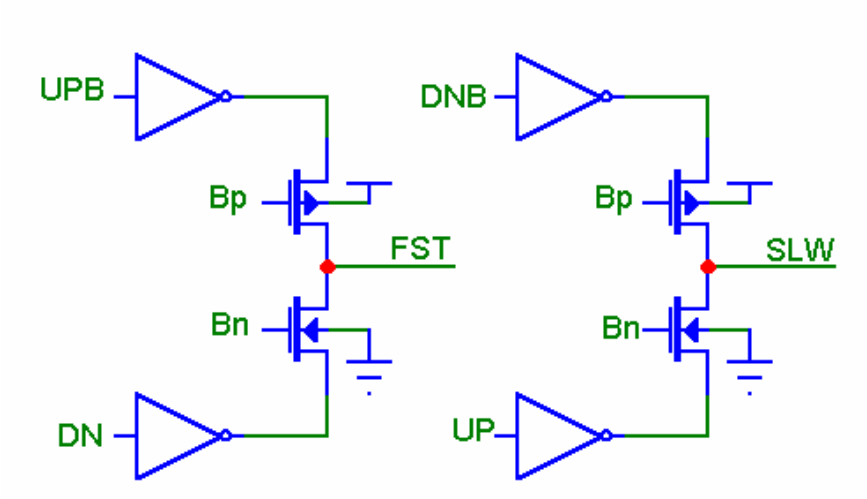


Figure 67: Differential output generation blocks with proper switches

Due to the unavoidable mismatches between the NMOS and PMOS current sources in the charge pump, a net current would flow to the loop filter even when the PLL is in lock. This current causes the two differential control voltages FST (FAST) and SLW (SLOW) to drift independently of each other. Moreover, the differential PLL loop only corrects for differential control signal, but not for the common mode. The drifting common-mode voltage then saturates the charge pump to make the pull-in of the VCO

impossible. Inserting a common-mode feedback circuit in the charge pump would solve this problem. The common-mode correction scheme proposed in this work is shown in Figure 68. In this implementation, the common-mode voltage of the FST and SLW signals is sensed and compared with a common-mode reference V_{CMO}, which usually is set to be the mid-rail voltage. Also the low-pass filter capacitor voltages, rather than the charge pump outputs, can be used to generate the common-mode voltage. The respective connection is depicted with dashed lines in Figure 68. This connection would reduce the injection of any possible noise at the charge pump output to the feedback branch.

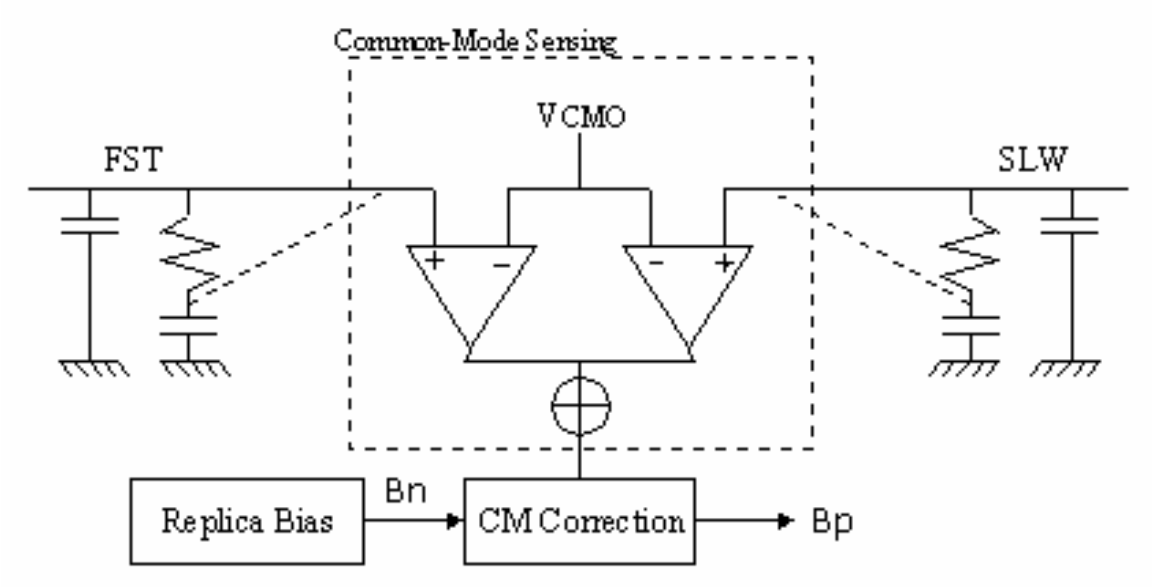


Figure 68: Common-mode feedback scheme

When the output common-mode level V_{CM} is equal to V_{CMO}, the PMOS bias voltage Bp is generated by replica biasing to equalize the charging and discharging currents. If V_{CM} goes below V_{CMO}, Bp is reduced to increase the charging current and slightly pull-up the output common-mode. Similar correction takes place if V_{CM} is above

V_{CMO} by decreasing the charging current. CMOS implementation of the common-mode block with the replica biasing is given in Figure 69.

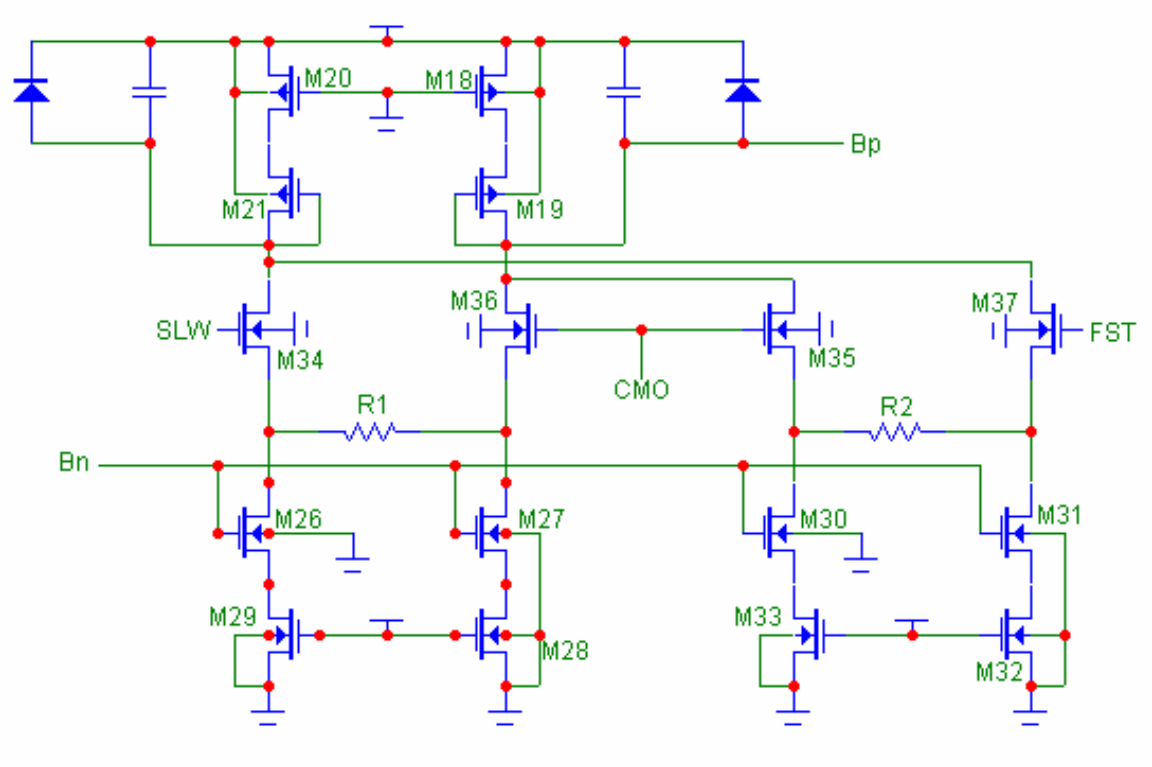


Figure 69: Common-mode feedback circuit

The common-mode sensing circuit is basically a transconductance amplifier, whose linearity can be increased for a wide input range by using bigger resistors, R1 and R2. However, these bigger resistors pull the DC gain down, increasing the steady state error. The transistors M18, M20, M28, M29, M32, and M33 are inserted so that the charging and discharging currents can be more accurately scaled. The capacitors at the bias nodes help to reduce charge injection as in the previously discussed single-ended charge pump while increasing the stability of the DC bias voltage. The diodes have no

effect on charge pump performance. Yet, they are inserted to discharge metal during the etching process so that the characteristics of the current sources do not change.

It is important to note that common-mode correction takes place only when the charging branches of the charge/discharge blocks are conducting because of the switches in the feedforward path. This fact introduces a low-bandwidth constraint for the common-mode feedback system to be modeled as a stable continuous time system. Common-mode correction over the sampled output data has advantages such as less loading of the feedback on the feedforward operation and decreased noise susceptibility against its continuous-time counterpart. The open-loop stability analysis, shown in Figure 70, is done with the charging and the discharging paths on. The common-mode feedback loop bandwidth is designed to be 3 KHz with a phase margin of 76 (180 – 104) degrees. The common-mode feedback transconductance gain is designed to be 40 μA/V. Implemented in TSMC's 0.18 μm technology, the layout of the differential charge pump, consuming an area of 150x130 μm^2, is shown in Figure 71.

The differential output voltages for the VCO leading case are shown in Figure 72(a). The FST output is being discharged while the SLW output is being charged in the simulation. Although the output voltages of the charge pump can be driven to the rails by fast input switching in one direction, linear charge pump operation is limited to 1.07 V/output (Figure 72(b)). The reason for a nonlinear operation out of the 0.32 V-1.39 V range is the reverse currents at the outputs due to additional switching transistors on the charging/discharging paths. The charge pump current is set to 100 μA and the power supply voltage to 1.8 V in the simulations.

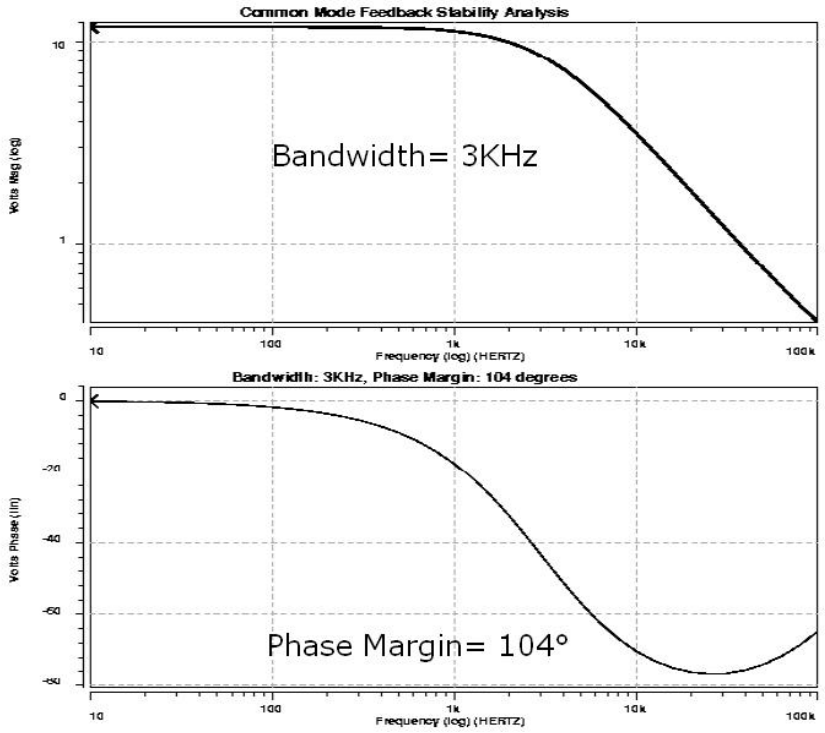


Figure 70: Common-mode feedback stability

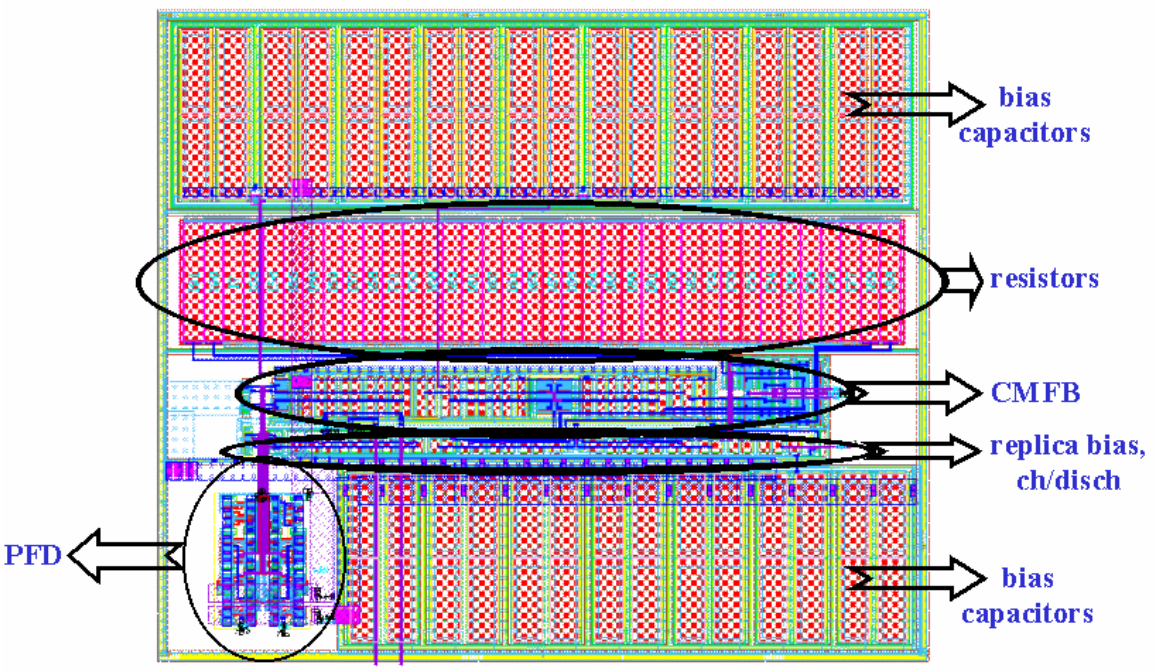
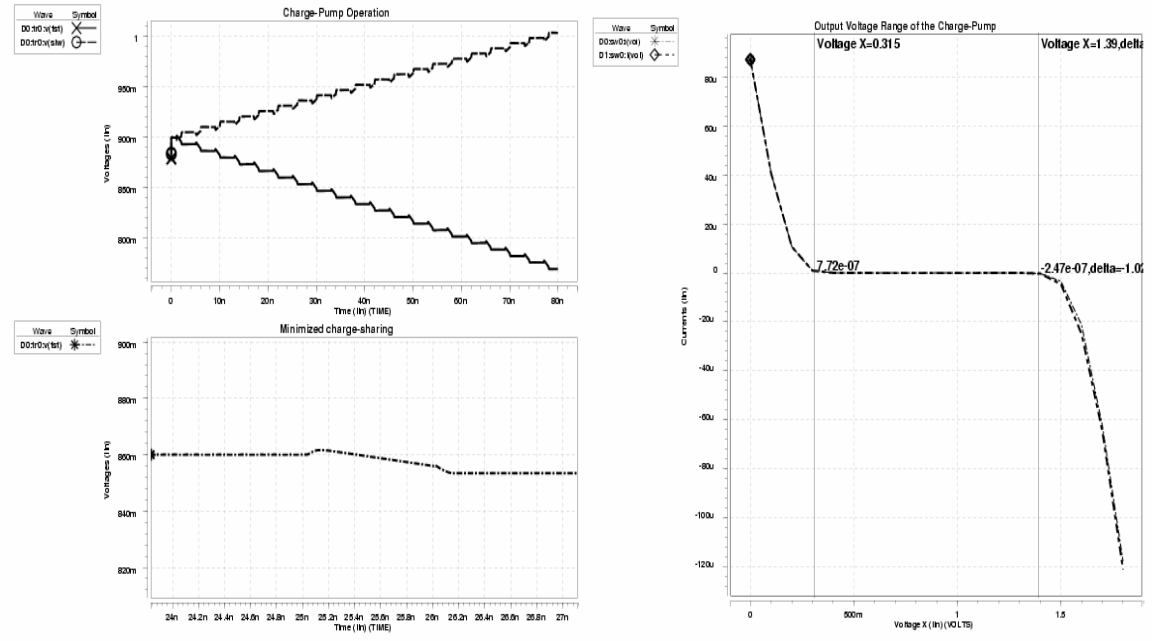


Figure 71: Layout for the differential charge pump

Properties of the designed charge pump can be summarized as:

- high output resistance
- decreased charge sharing
- decreased charge injection
- decreased 1/f noise
- decreased output voltage range.



(a) (b)

Figure 72: (a) Charge pump operation and (b) output voltage range

The amount of the phase offset due to current mismatch is given by

$$\Phi_{offset} = 2\pi \frac{\Delta t_{on}}{T_{ref}} \frac{\Delta i}{I_{CP}} \quad \textbf{(39)}$$

where ϕ_{offset}, Δt_{on}, T_{ref}, Δi, and I_{cp} are the static phase error, the turn-on time for the PFD, the reference clock period, the current mismatch, and the charge-pump current respectively [39]. According to this equation, reducing the PFD turn-on time and the current mismatch in the charge pump can minimize the phase offset [52]. Above minimum turn-on time of the PFD, however, is needed to eliminate the dead-zone. Therefore, the current mismatch needs to be reduced to attain low phase error. Current matching at any output voltage level is maintained by the proposed charge-pump with common-mode feedback.

5.1.2 LC Oscillator Design

Regardless of their narrow tuning range, LC oscillators continue to make their way into various high-performance applications through extensive research in RF design. The gradually increasing popularity of LC oscillators does not only depend on the fact that they exhibit substantially less phase noise than ring oscillators, but also their high slew rate at high frequencies [53]. Furthermore, LC oscillators can potentially operate from lower supply voltages than ring oscillators can [54]. The issues of the LC oscillator design are discussed in this section.

The performance of LC oscillators profoundly depends on the features of inductors and varactors. LC oscillators in the literature are mainly implemented in customized CMOS processes to increase the quality factor of inductors (up to 50) [55]. The cost, however, is significantly increased for these modified processes, and monolithic integration may sometimes be unfeasible due to additional steps.

The circuit schematic for the LC oscillator is shown in Figure 73. An external bias current, I_{bias}, is mirrored to provide static current to the oscillator tank. The cross-

coupled NMOS and PMOS transistors compensate for the energy loss in the LC tank by introducing negative resistance. The use of cross coupled PMOS devices in addition to the NMOS devices allows more symmetry between the rise time and fall time of the output waveforms. The output signal symmetry reduces the upconversion of low frequency noise (such as flicker noise) into phase noise [8] by improving the duty cycle. The addition of PMOS devices however increases output parasitic capacitance to limit the tuning range.

The importance of differential frequency tuning is already discussed. In this LC VCO, four varactors (two PMOS and two NMOS) are employed instead of two as in a conventional design [56]. The cross-section of an accumulation mode NMOS varactor, NMOS built in an N-well, is shown in Figure 74 [57, 58].

As the gate voltage increases, the device enters more into the accumulation region. Then, the silicon surface becomes highly conductive, driving the gate capacitance to its maximum value. As the gate voltage decreases, the depletion region widens and the capacitance approaches its minimum value. The capacitance versus the gate-to-source voltage (C-V) characteristic is given in Figure 75.

MOS varactors in this design have a gate length above the minimum to decrease the significance of gate overlap capacitance, increasing the dynamic range. However, it is important to note that increasing the gate length increases the resistance between source and drain terminals, thus degrading the Q. Multiple MOS devices are utilized (fingering) to implement each of the varactors, maximizing the Q factor.

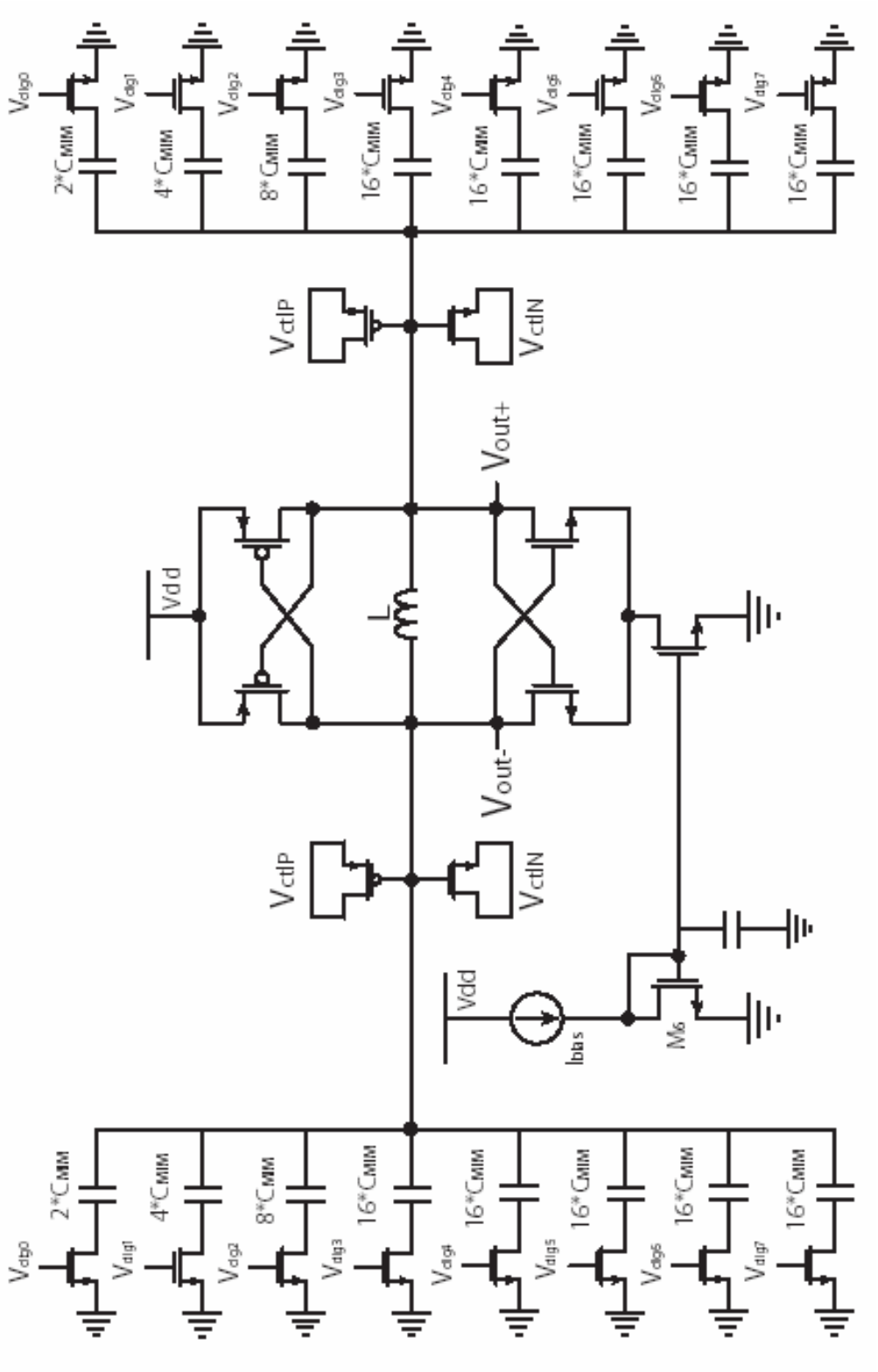


Figure 73: LC oscillator schematics

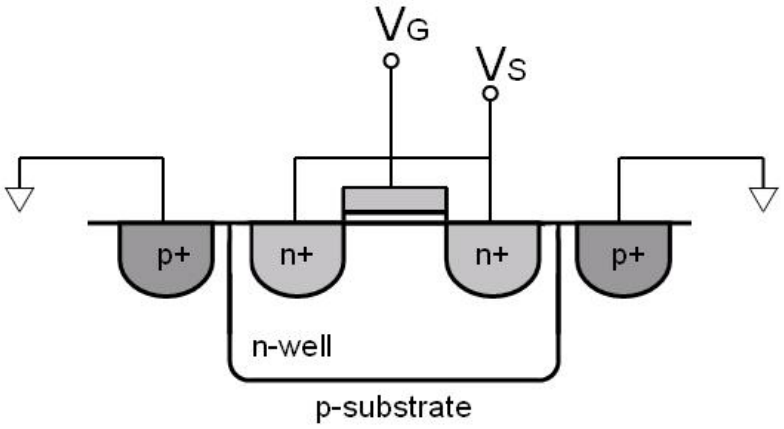


Figure 74: Accumulation mode varactor

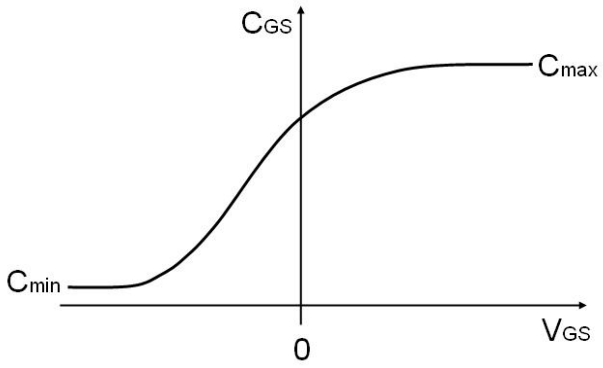


Figure 75: C-V characteristic

The Q factor for an accumulation mode varactor is usually an order of magnitude higher than the Q factor for a spiral inductor (~10). Therefore, the spiral inductor mostly determines the Q factor of the LC tank. The most critical component that determines the phase noise for the LC VCO is hence the on-chip spiral inductor. The inductor, shown in Figure 76 is drawn using the thick top metal layer offered by the mixed-mode process, guaranteeing low series parasitic resistance (L= 2.4 nH, R= 2 Ω). The top-thick metal

layer is a big advantage as low series resistance is needed and the metal width cannot be effectively increased due to skin effect and capacitive coupling. An octagon shape is chosen as a good approximation to a circle. A circle is the optimum shape with the shortest perimeter for a given enclosed area, thus increasing the self-resonant frequency of the inductor. In other words, the capacitive coupling of the inductor to the substrate determines the highest frequency that the device can be used as an inductor. The inner turns of the inductor are removed, keeping the inductor hollow. The hollow design reduces the energy losses caused by the eddy current [59].

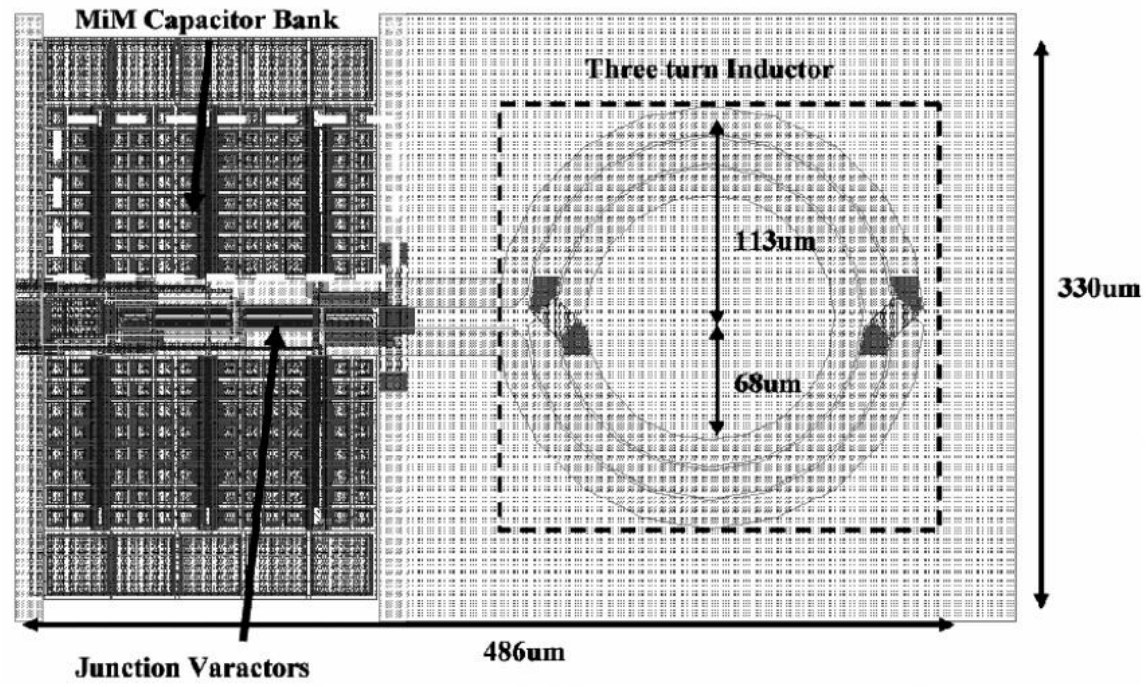


Figure 76: LC oscillator layout

Due to the process, voltage, and tempereature (PVT) variations, the limited tuning range of the LC VCO, and lack of perfect models for spiral inductors, it is risky to design an LC VCO to run at a certain frequency. Therefore, coarse-tuning control is added by digitally adjusting the capacitive loading at the output nodes. Binarily-weighted metal-insulator-metal (MiM) capacitors and appropriately sized transistor switches put the coarse tuning into effect. The symmetric loading capacitor blocks, along with proper sizing, can also be spotted in Figure 73.

Figure 77 demonstrates both tuning effects by sweeping the differential control voltage at various digital control levels. Figure 78 shows the same characteristics extracted from measurements. The measured VCO has a monotonic tuning range of 1.9 GHz- 3.05 GHz. Despite the similarity of simulation and measurement data, the actual oscillator is slower than the simulations predict possibly due to insufficient modeling of inductors in this process. Also the Q factor of the inductor is degraded by the automatic filling process of MOSIS that is applied to any multi-project chip to meet the minimum density requirements for CMP (chemical mechanical polishing). The dummy layers of metal and poly inserted under the inductor increase losses due to magnetic coupling. The losses on these conducting layers, together with the substrate losses, cause a large degradation in the overall quality factor and reduce the inductance value.

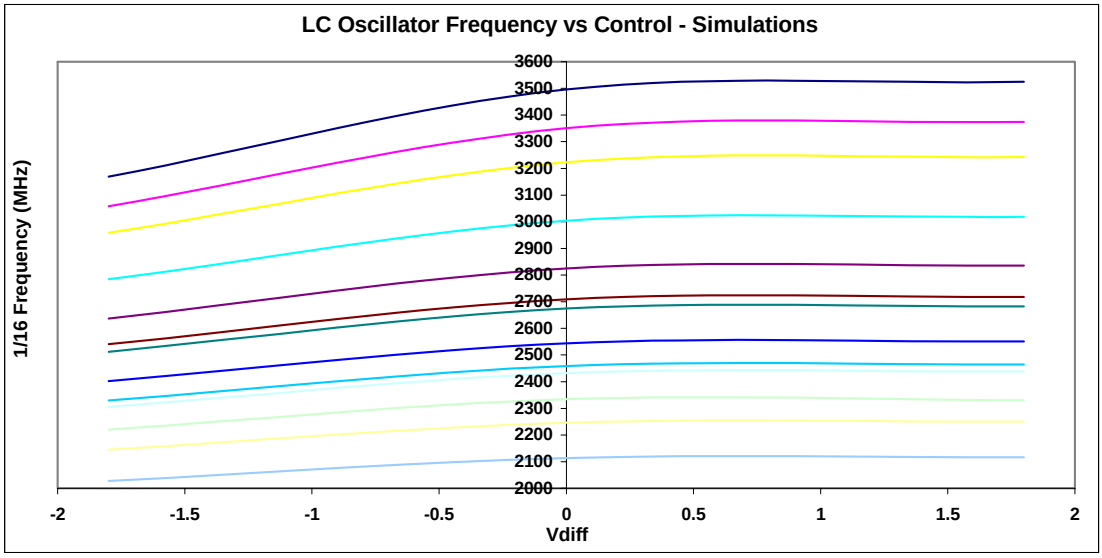


Figure 77: Simulated LC oscillator characteristic

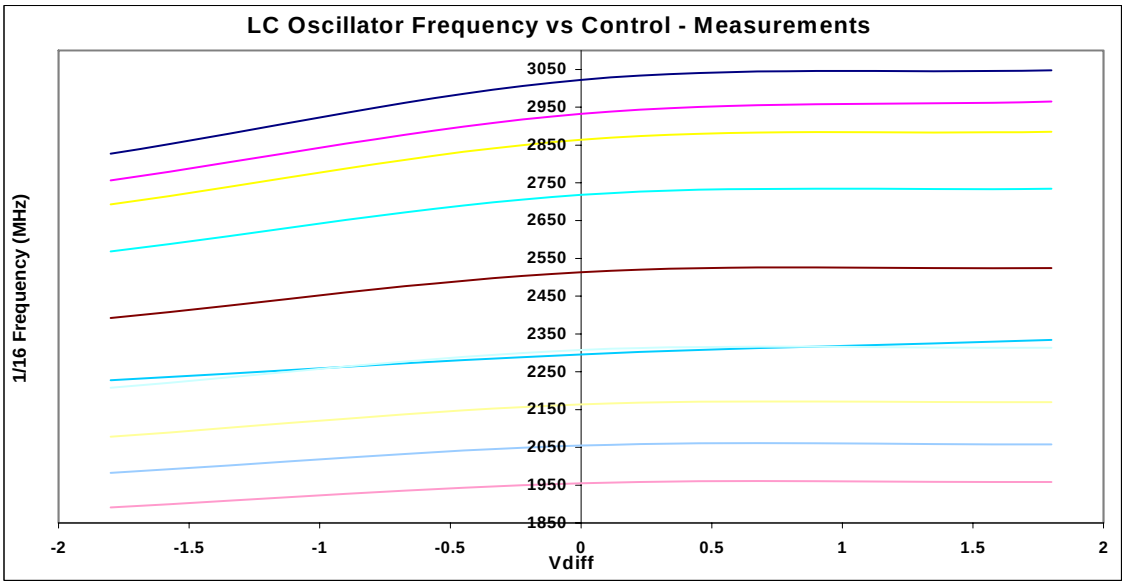


Figure 78: Measured LC oscillator characteristic

Power spectrum analysis of the LC oscillator's divide-by-16 output is illustrated in Figure 79. The phase noise of the 1/16 output is measured as –83.8 at 100 KHz offset from the center frequency, 157.8 MHz. This measurement is used to calculate the free-

running VCO phase noise at 1 MHz offset from 2.5 GHz center-frequency as –99.8 dBc/Hz using Equation 38.

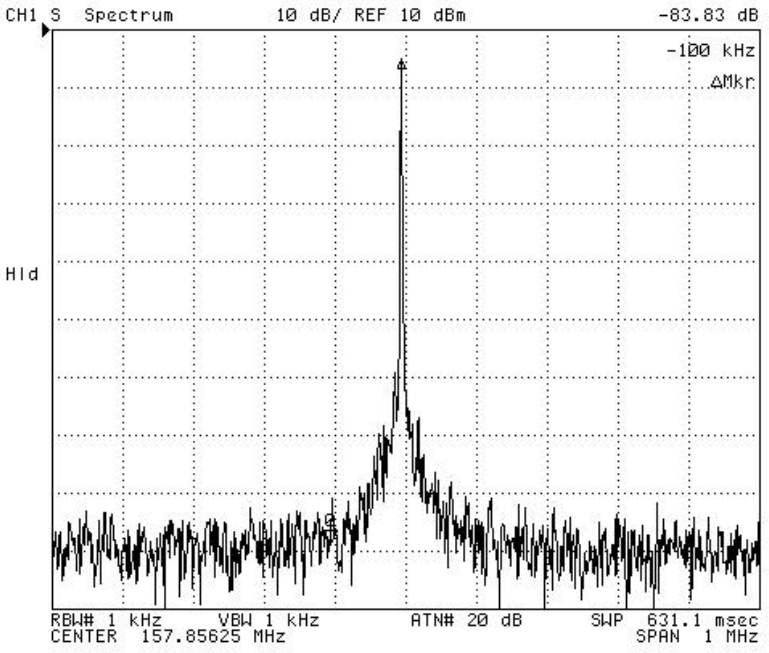


Figure 79: Measured power spectrum of the LC oscillator's 1/16 output

LC oscillator performance is summarized in Table 6.

Table 6: LC oscillator performance summary

LC Oscillator	
Power supply voltage (V)	1.8
Bias current (mA)	2
VCO range (GHz)	1.89 – 3.05
Coarse-tuning range (%)	42.7
Fine-tuning range (%)	2.7 – 8.9
RMS jitter (ps)	13 – 60
Phase noise @1MHz offset from 2.5GHz (-dBc/Hz)	99.8

5.1.3 PLL Test Results

After characterizing the oscillator, a second-order control loop is constructed as shown in Figure 80. Even though internal loop filters are preferable in terms of noise performance, the external loop filter is employed to have some form of flexibility within the PLL system without another pass of the silicon.

The maximum operating frequency of the PFD/CP blocks is measured as 450 MHz. The division ratio, N=16, on the feedback path guarantees the proper phase comparison by limiting the input range from 118 MHz to 190 MHz. The first-order loop filter is designed such that a couple hundred KHz of bandwidth is assured at all characteristic curves of the VCO. Lower loop bandwidth can cause stability problems since the system contains two coupled loops (CMFB loop and phase-locked loop). Because the time constants of the two loops are two orders of magnitude different, the stability is guaranteed for the chosen filter (R1= 680 Ω, C1= 0.01 μF). The loop is tested to lock-in correctly over the whole range, which means the CMFB control is functioning as designed. Table 7 summarizes some measurement results for third-order loop filter at 1.8 V power supply and ambient temperature, while Figure 81 demonstrates the lock state at 2.5 GHz of VCO frequency.

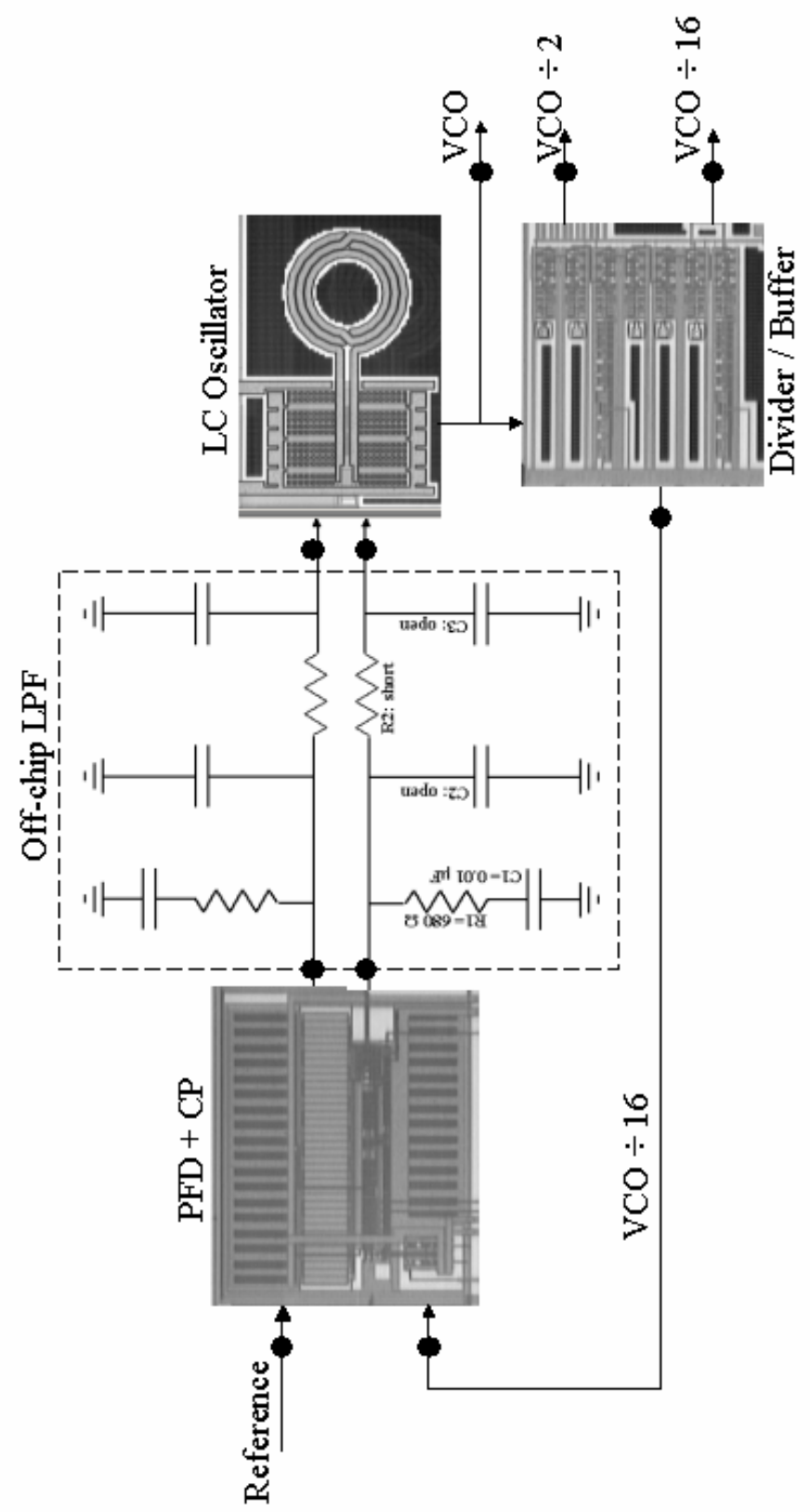


Figure 80: PLL test setup

Table 7: The 2.5 GHz PLL measurement summary

2.5 GHz PLL with LC VCO	
Output lock-in range (MHz)	2402-2518
Input lock-in range (MHz)	150.1-157.4
Division ratio	16
C_1 (nF)	10
C_2 (pF)	50
C_3 (pF)	50
R_1 (Ω)	680
R_2 (Ω)	1500
Phase margin	54.92
PLL bandwidth (kHz)	54.36
Output RMS jitter (ps)	3.5
Phase noise @ 1MHz offset (-dBc/Hz)	123

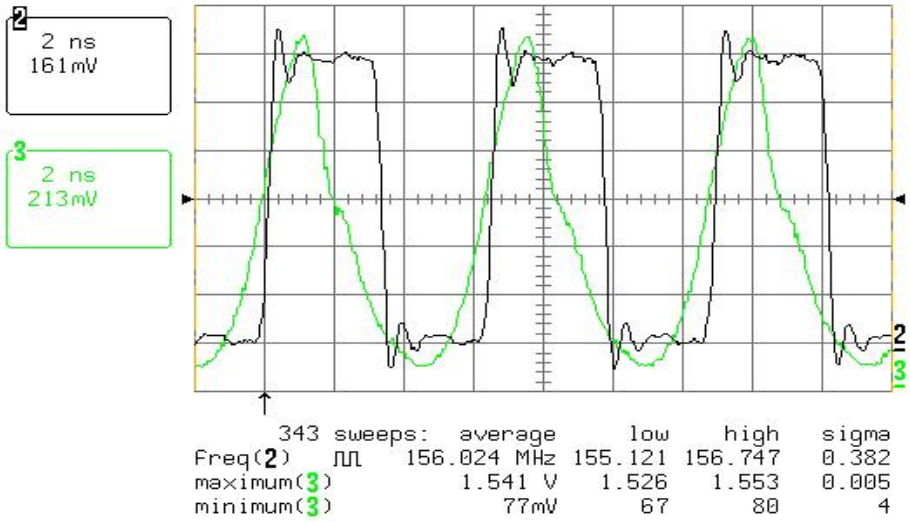


Figure 81: Phase-locked state at f_{VCO}= 2.5 GHz

The PLL output has also been examined in the frequency domain. Divide-by-2 and divide-by-16 output power spectrums are illustrated in Figures 82 and 83 respectively. The output is dramatically improved in the lock mode when compared to

the free-running VCO. The locked output (–123 dBc/Hz phase-noise at 1 MHz offset from 2.5 GHz) is also confirmed to be cleaner than the reference. The input reference power spectrum is shown in Figure 84.

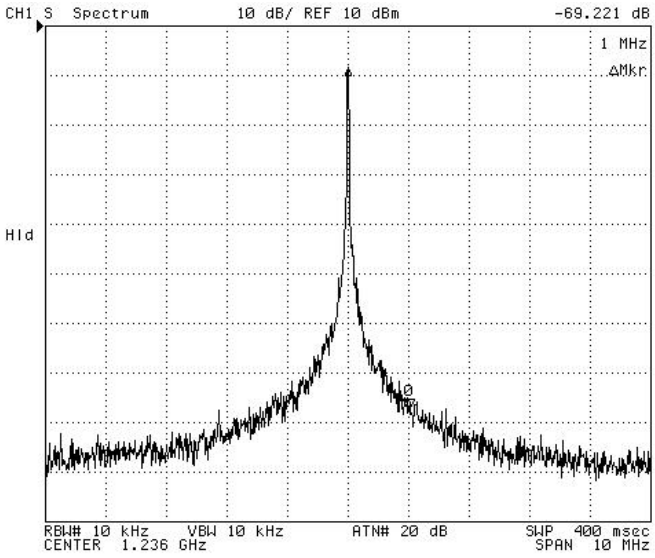


Figure 82: Measured phase noise of the ½ output

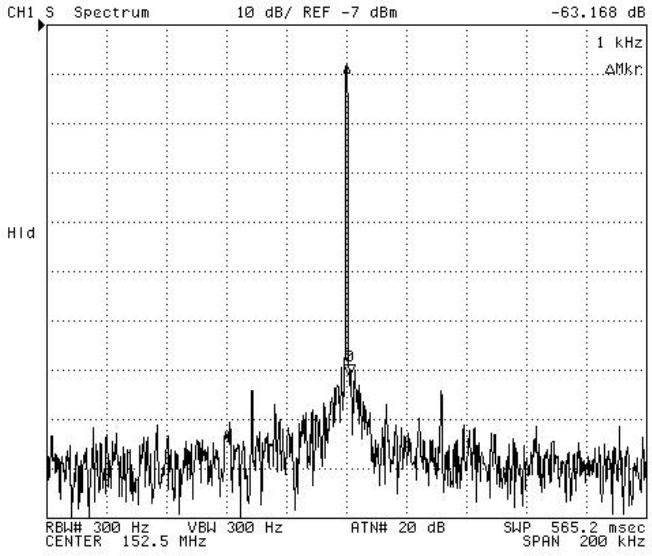


Figure 83: Measured phase noise of the 1/16 output

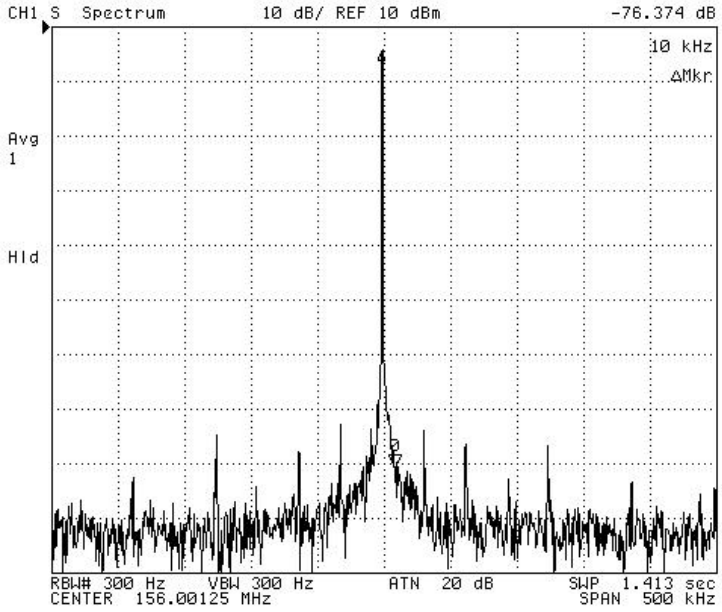


Figure 84: Measured phase noise of the input reference

5.2 Physical design considerations

In addition to the device noise that is fundamental and cannot be totally removed, part of the phase noise derives from systematic factors. Some of these systematic factors are device mismatches, power supply fluctuation, ground bounce, and cross-talk. These factors can - to a good degree- be avoided by a careful system/device layout.

Advanced layout techniques were applied throughout this work to minimize the mismatches between the circuit and the layout [60]. Higher performance can be achieved by considering these techniques at different hierarchical levels as summarized in Table 8 in a bottom-top manner.

Table 8: Layout considerations

Level of Design	Layout Technique	Improvement
Basic components (transistors, resistors, and capacitors)	Stacked layout	- Reduced parasitic capacitance - Improved matching - Reduced effects of physical parameter gradients and local variations
	Dummy component	- Reduced mismatch (boundary-dependent undercut effect)
Analog cells	Common centroid topology	- Improved matching
	Multiple VIAs	- Reduced parasitic resistance - Increased reliability
	On-chip coupling capacitors at DC bias nodes	- Reduced DC bias noise
Routing	Matched and short bus lengths	Reduced parasitic capacitance Reduced mismatches of signals between the stages
	Decoupled parallel analog and digital lines (larger distance or ground line in between)	- Reduced noise injection due to capacitive coupling
	Complimentary signals crossing analog bus	
Power supply connections	Analog and digital supplies merging as close to the pad as possible	- Reduced digital noise coupling
	Wide supply buses at the top metal (thick metal)	- Reduced parasitic
Substrate biasing	Guard rings	- Reduced substrate noise by shielding - Latch-up prevented
Floor planning	Critical analog components placed far from digital elements (including switches)	- Reduced crossing of analog and digital signals (lower coupling) - Isolated critical blocks by well shielding
	Common centroid topology	- Improved matching
Pads	Electrostatic discharge protection within the custom designed analog I/O pads	- Reduced risk of destroying the chip
Pins	Middle pins assigned to most critical signals	- Reduced parasitics on critical paths
	Separate power pins for analog and digital blocks	- Reduced digital noise coupling

The prototype chip has been fabricated using a non-epi 0.18-μm n-well six-metal CMOS technology. Figure 85 shows a microphotograph of this chip consisting of two different PFD/CP designs, an integrated LC oscillator, a three-stage ring oscillator, a nine-stage ring oscillator, a new digital PLL, and a regulator block.

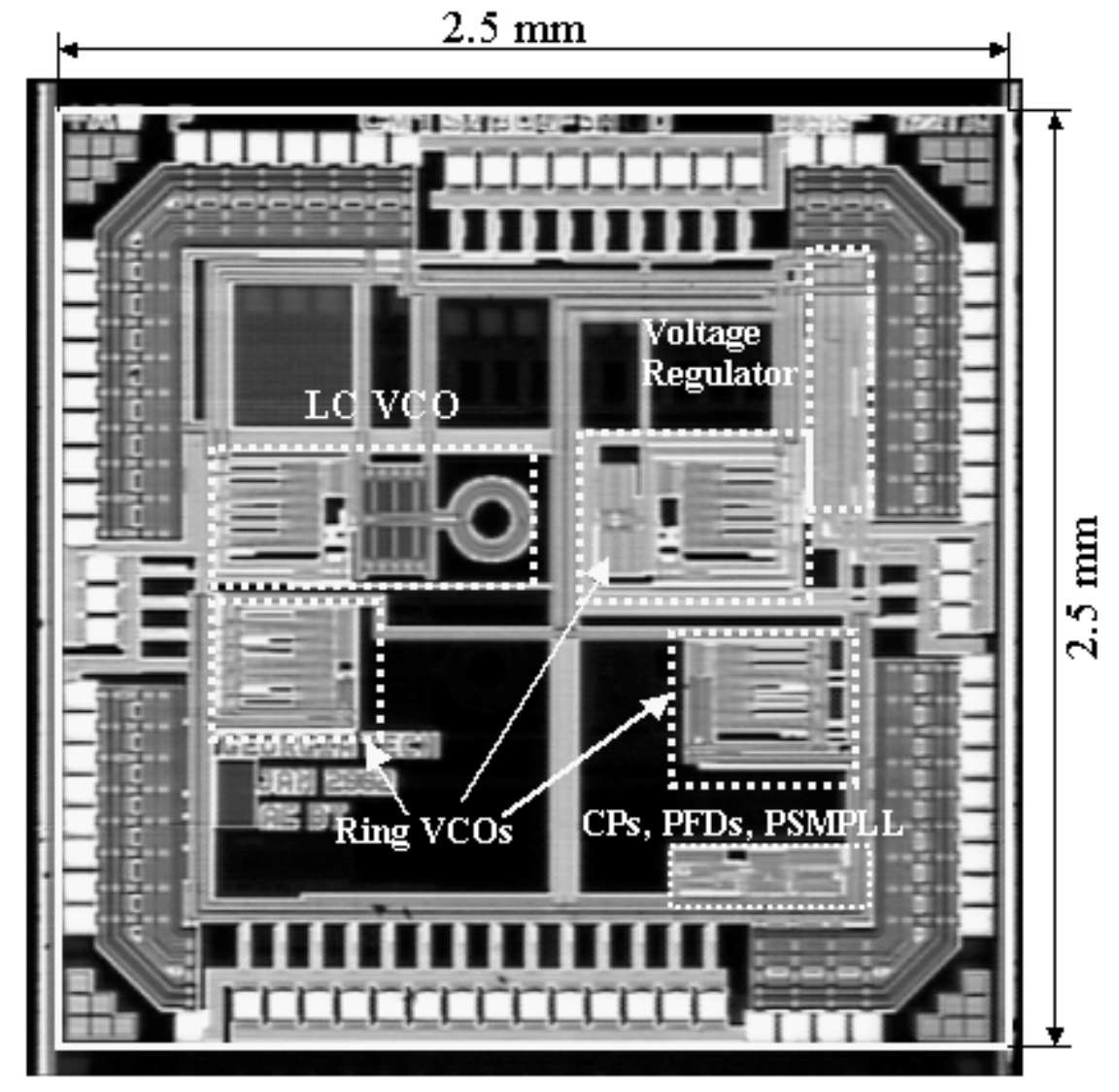


Figure 85: Chip microphotograph

CHAPTER VI

PLL DESIGN SUMMARY

Major PLL design considerations will be discussed in this chapter. The chapter will start with the performance boundaries of ring and LC oscillators where theoretical limits and measurement results will be demonstrated for a better understanding of the trends. Then, considerations on the oscillator parameters will be discussed towards the PLL performance. The designed PLLs will be summarized with a comparative study to explain where this work fits in the literature. The comparison will be seized according to multiple performance metrics including maximum frequency, phase noise, and jitter. General characteristics and design guides for high performance PLLs will be extracted with possible problems in the implemented control scheme and possible future solutions.

6.1 LC versus Ring Oscillators

Even though the measured Q factor of the LC VCO was slightly lower than 5, quality factors up to 14 can be achieved in standard CMOS [61, 62]. Meanwhile, the effective Q factor for conventional ring oscillators is no higher than 1.55 [6]. Ring oscillators employ multiple stages of active switches that contribute to the output noise, whereas LC oscillators employ passives resulting in a superior noise performance. Also the maximum frequency of a ring oscillator is limited by the minimum delay of a gain stage, while determined strictly by the inductor and the capacitor in an LC oscillator. The upper

frequency limit of an LC VCO is the self-resonance frequency of the inductor due to its parasitic capacitance to the substrate. It is also important to note that the power and noise performance trade-off in ring oscillators does not exist in LC oscillators, because higher Q corresponds to a less noisy output and lower power dissipation in LC VCOs. Ring oscillators, on the other hand, usually require a smaller die area, generate multiple phases at the output, and are easier to design in a standard CMOS process. Despite the limitations on frequency and noise in standard ring oscillators, there are various architectures and circuit design techniques to boost up their performance. For example, the saturated delay stages utilized in this work can provide a quality factor as high as 4.5 at 900 MHz.

Using the best known phase noise models, such as Leeson's [9], Razavi's [6] and Harjani's [7], together with published measurement results, Eken estimated limit curves for LC and ring VCOs as shown in Figure 86 for a logarithmic frequency axis [63]. These curves estimate that ring oscillators do not only exhibit 10 dB more phase noise at 5 GHz compared to the LC oscillators, but also do they dissipate 16 times more power.

Once defining the theoretical limits of the phase noise, a variety of published measurements and this work are next to be demonstrated in a comparative manner. For consistency, all offset frequencies for the plotted measurements are scaled to 1 MHz by assuming a 20 dB/decade drop. The scatter plots for the CMOS LC oscillators and the ring oscillators are shown in Figure 87 and 88, respectively [63].

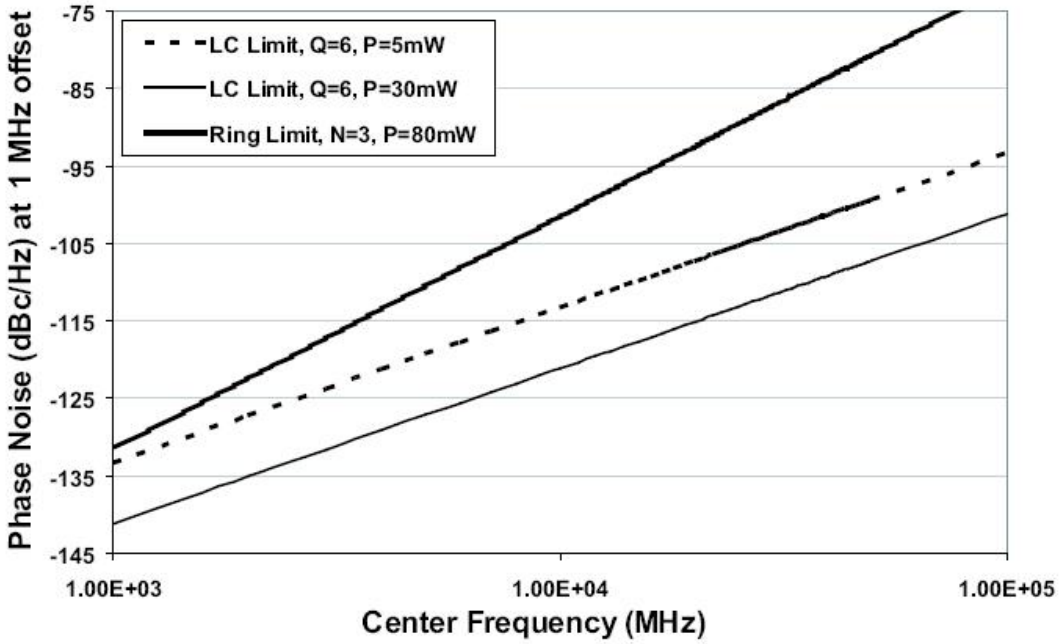


Figure 86: Phase noise limits of ring and LC oscillators

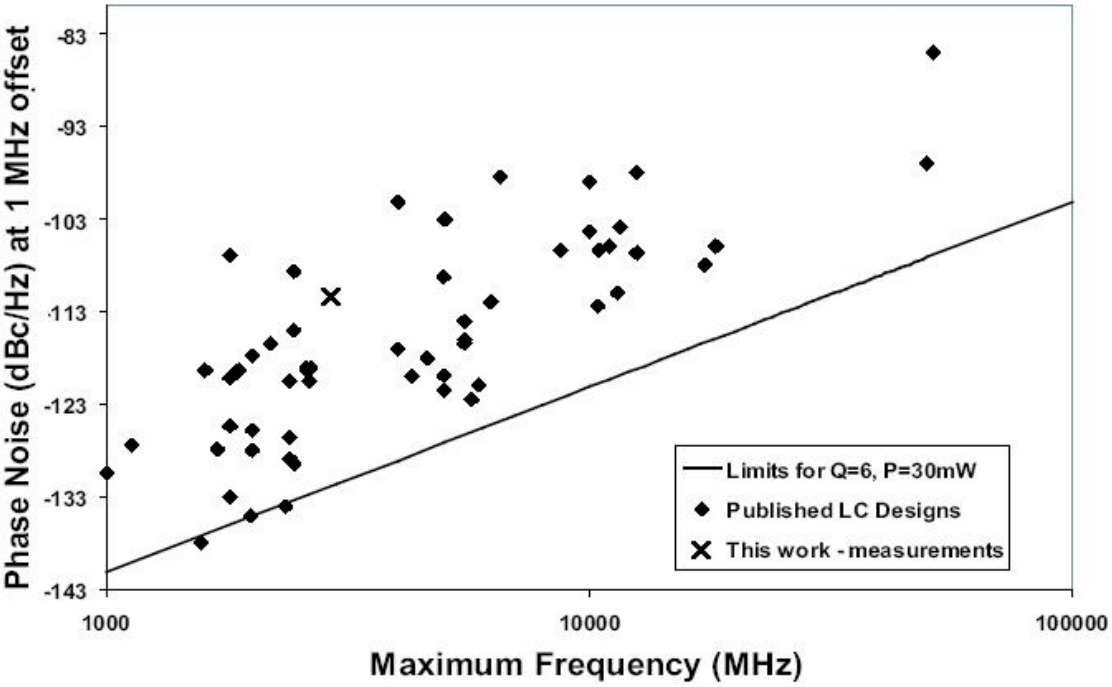


Figure 87: Phase noise versus frequency performance of LC VCOs

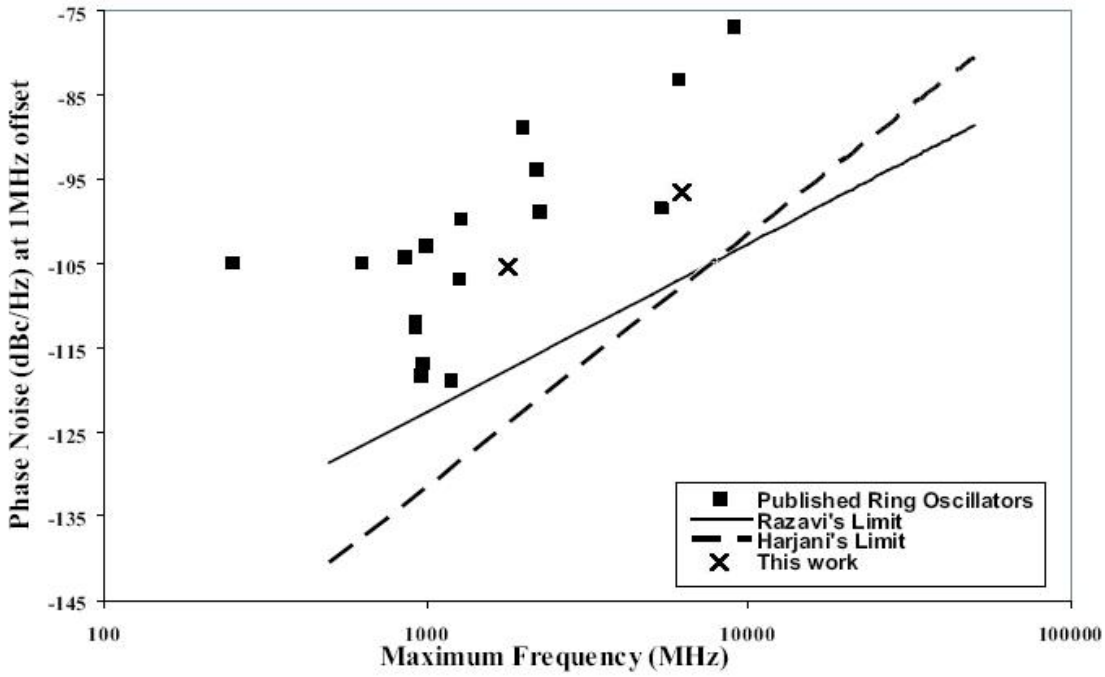


Figure 88: Phase noise vs frequency performance of ring VCOs

6.2 Single-ended versus Differential Oscillation Control

The advantages of a differential VCO, where differential outputs are generated, are already made clear in the context of oscillator design. Most important of these advantages were pointed out to be power supply noise and ground bounce immunity and 50% duty cycle generation. However most of the differential oscillators in literature utilize a single-ended control line. The advantage of a single-ended control line is the reduction in terms of area and power. It is, on the other hand, very critical to question the necessity of a differential control in high performance PLLs.

As the supply voltage scales down with the shrinking feature size, the gain of the oscillator needs to scale up to cover a certain frequency range. This is illustrated in

Figure 89 where supply scaling lowers the maximum control voltage from V2 to V2', the range (w1, w2) fixed, yielding a bigger VCO gain.

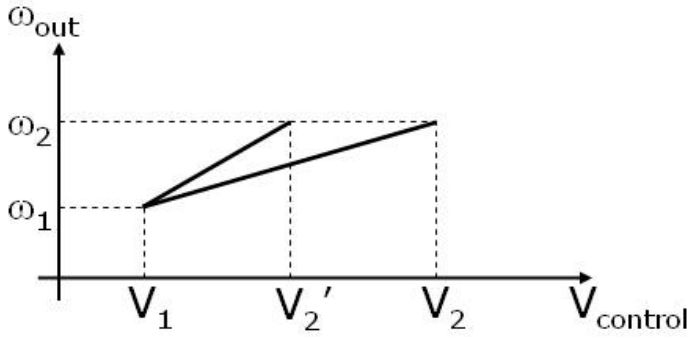


Figure 89: Increasing VCO gain due to supply scaling

The unavoidable increase in K_{VCO} causes a higher sensitivity to the noise that occurs at the control line. The noise on the control line is inevitable because of the parasitic leakage of the filter, parasitic leakage of the charge pump, current mismatch of the charge pump, and the periodic disturbance (even at the steady state) due to the PFD characteristic.

As an example, assume a sinusoidal control voltage $V_{ctrl} = V_m cos\omega_m t$ rather than a DC voltage. The VCO output is then expressed as

$$V_{out}(t) = A\cos(\omega_{FR}t + K_{VCO}\int_{-\infty}^{t} V_{ctrl}dt) = A\cos(\omega_{FR}t + K_{VCO}\frac{V_m}{\omega_m}\sin\omega_m t) \quad \textbf{(40)}$$

$$V_{out}(t) = A\cos\omega_{FR}t\cdot\cos(K_{VCO}\frac{V_m}{\omega_m}\sin\omega_m t) - A\sin\omega_{FR}t\cdot\sin(K_{VCO}\frac{V_m}{\omega_m}\sin\omega_m t) \quad \textbf{(41)}$$

$$V_{out}(t) \approx A\cos\omega_{FR}t - AK_{VCO}\frac{V_m}{\omega_m}\sin\omega_{FR}t\cdot\sin\omega_m t \quad \textbf{(42)}$$

$$= A\cos\omega_{FR}t - \frac{AK_{VCO}V_m}{2\omega_m}\left[\cos(\omega_{FR}-\omega_m)t - \cos(\omega_{FR}+\omega_m)t\right] \quad \textbf{(43)}$$

The output spectrum, which consists of three frequencies, is shown in Figure 90. The components at ($\omega_{FR} \pm \omega_m$) are identified as sidebands and appear as timing jitter in PLL applications.

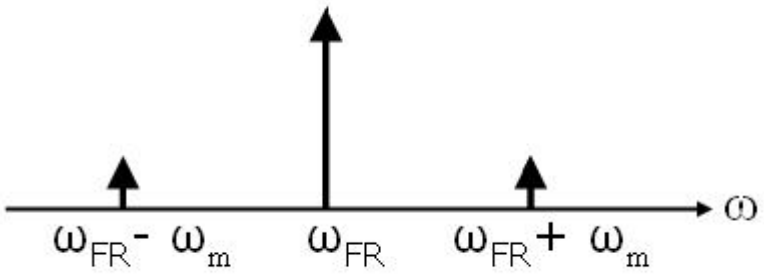


Figure 90: Sidebands at VCO output

This example shows that time variations of the control voltage may create unwanted components at the output. Therefore, the control voltage variation must be minimized at the steady state. This discussion can be expanded for the square wave VCO output since the square wave can be expressed as an infinite sum of sinusoidal signals (Fourier series).

The sideband magnitude in the above example is directly proportional to the VCO gain. Hence, the differential control in a PLL decreases the spur magnitude as it relaxes the gain constraint to cover a certain frequency range. Ideally, since the differential control doubles the dynamic range, the spur levels drop by 50%. Besides, the common-mode rejection of the differential control significantly lowers the output spur levels.

Differential oscillator control typically requires the use of a differential charge pump and an extra loop filter. The differential charge pump design, however, is not an easy task as it requires a common-mode feedback (CMFB) correction scheme. Most CMFB implementations in literature degrade the tuning range of the VCO due to the MOS threshold voltages. The common-mode sensing through a transconductance amplifier, explained in Section 5.1.1, solves this problem. The common-mode feedback also decreases the VCO spur levels by adjusting the control voltages for improved linearity.

6.3 PLL Comparison

In this section, after the performance characteristics for the measured PLLs are summarized, they will be compared to the published designs in the literature [13, 33, 37, 40, 42, 64-76]. The PLL measurement results are summarized in Table 9. Two of these PLLs utilize single-ended controlled ring oscillators, and the third PLL incorporates a differentially controlled LC oscillator.

After summarizing the test results, the PLL performance is plotted together with published designs for comparison. Figure 91 shows the maximum phase locking frequencies extracted from most significant papers together with the presented measurement results.

It is commonly known that ring oscillators have limited maximum frequency due to the stage delay. This work proves that a 3-stage multi-feed VCO can achieve high frequency operation meeting the requirements of the RF and optical transceiver applications.

Table 9: Summary of the PLL measurements

	PLL at 1.8 GHz	PLL at 5.8 GHz	PLL at 2.5 GHz
Control path	single-ended	single-ended	differential
VCO type	9-stage multi-pass ring	3-stage multi-pass ring	LC
VCO range (MHz)	1120-1860	5160-5930	2392-2525
Output lock-in range (MHz)	1180-1840	5310-5840	2402-2518
Input lock-in range (MHz)	74-115	166-182.5	150.1-157.4
VCO gain (MHz/V)	770	793	68
Division ratio	16	32	16
Charge-pump gain (μA/rad)	11.14	11.14	11.14
C_1 (nF)	10	10	10
C_2 (pF)	50	50	50
C_3 (pF)	50	50	50
R_1 (Ω)	680	680	680
R_2 (Ω)	1500	1500	1500
Phase margin	68.66	73.38	54.92
PLL bandwidth (kHz)	529.58	248.37	54.36
Output RMS jitter (ps)	1.7	2.6	3.5
Phase noise @ 1MHz offset (-dBc/Hz)	116	110	123
Power (mW)	112	50	5

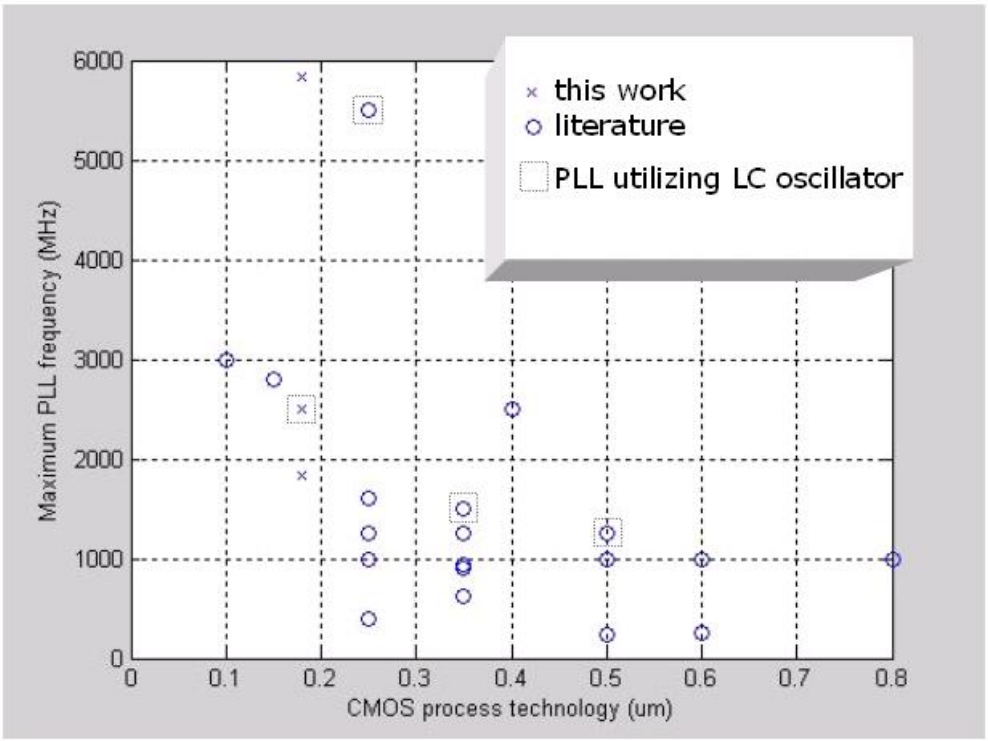


Figure 91: Maximum frequencies of published PLLs

Output phase noise at 1 MHz offset and center frequency of published PLLs with those of tested PLLs are illustrated in Figure 92. Very low phase noise at 2.5 GHz is achieved with a differentially controlled LC oscillator and a novel differential charge pump. The only PLL that performs better in terms of phase noise at multi-GHz frequencies is, interestingly, a single-ended loop, with single ended oscillator delay stages [64]. The reported PLL is built in 0.1 μm CMOS and the wafer is tested using a high-speed Picoprobe. There are no high-power digital blocks or dividers on the same chip to degenerate the power supply voltage. The results from [64] prove that single-ended PLLs can exhibit high performance with a clean supply and a clean ground. This fact, indeed, led to recent single-ended PLLs running from a regulated power supply for lower power applications.

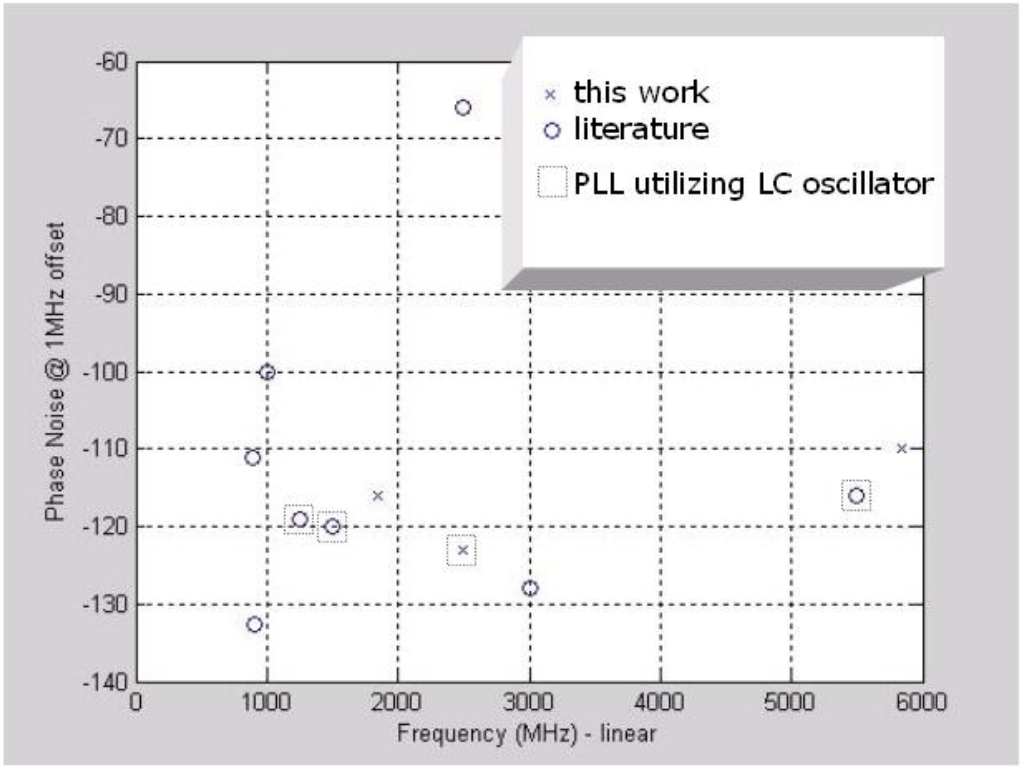


Figure 92: Phase noise versus maximum frequency

Figure 93 compares the rms jitter and Figure 94 compares the normalized rms jitter of the measured PLLs with those of recently reported PLLs. All PLLs designed within this research fit in with top-notch recent implementations by demonstrating rms jitter values lower than 5 ps. The normalized rms jitter for these designs is lower than 2% of the clock period.

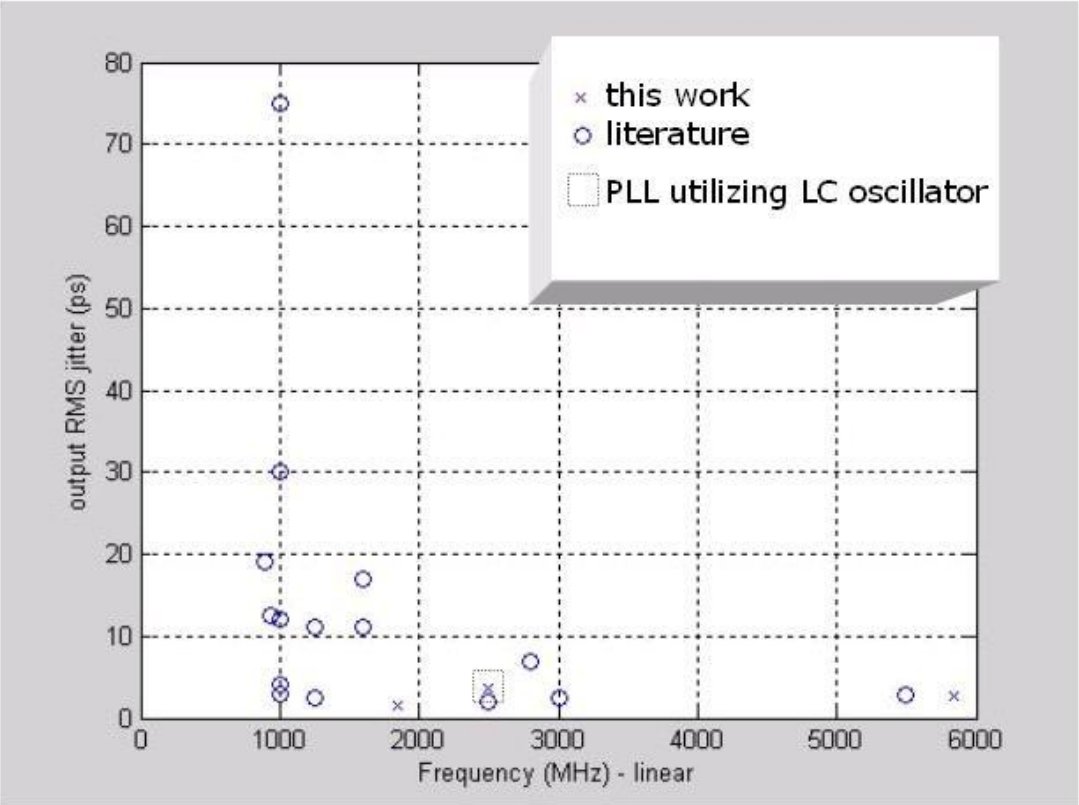


Figure 93: Reported output jitter and measurements

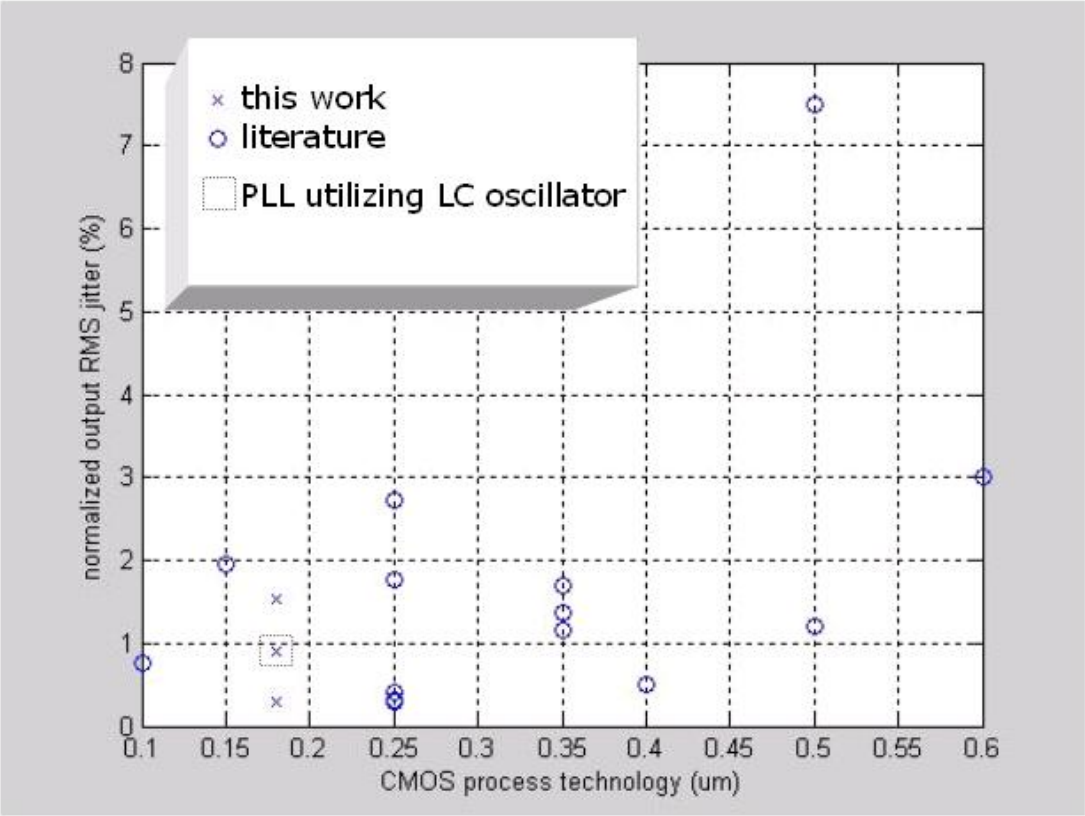


Figure 94: Reported normalized jitter and measurements

The above plots claim very similar jitter performance for single-ended control loops and the differential loop. It is crucial to note that these measurements are made after isolating oscillator blocks from each other by laser cuts. When all blocks on the same chip run simultaneously, degrading the power supply, an increase in jitter measurements is observed as shown in Table 10. The phase jitter increases by a factor of 20 to 35 for single-ended control architectures; whereas the ratio is lower than 6 for the differentially controlled oscillation. These results confirm the importance of fully differential structures for high performance applications where supply voltage

fluctuations may occur. Single-ended designs, however, can also find use in these applications when accompanied by a voltage regulator to filter out the supply voltage noise. This is obvious from the low jitter performance of these PLLs when run from a clean VDD.

Table 10: Phase jitter increase with noisy power supply

PLL Type	Oscillation control path	RMS phase jitter (ps)	
		clean supply voltage	noisy supply voltage
1.8 GHz	single-ended	1.7	60
5.8 GHz	single-ended	2.6	50
2.5 GHz	differential	3.5	20

Another key point is the fact that jitter increase is more significant at lower frequencies for the single-ended PLLs. This supports the theory developed for jitter contribution of a noisy control line (Section 6.2). Also the periodic cycle-to-cycle jitter characteristic –shown in Figure 95- confirms the significance of the control line noise by displaying frequency modulation of the VCO by a periodic signal.

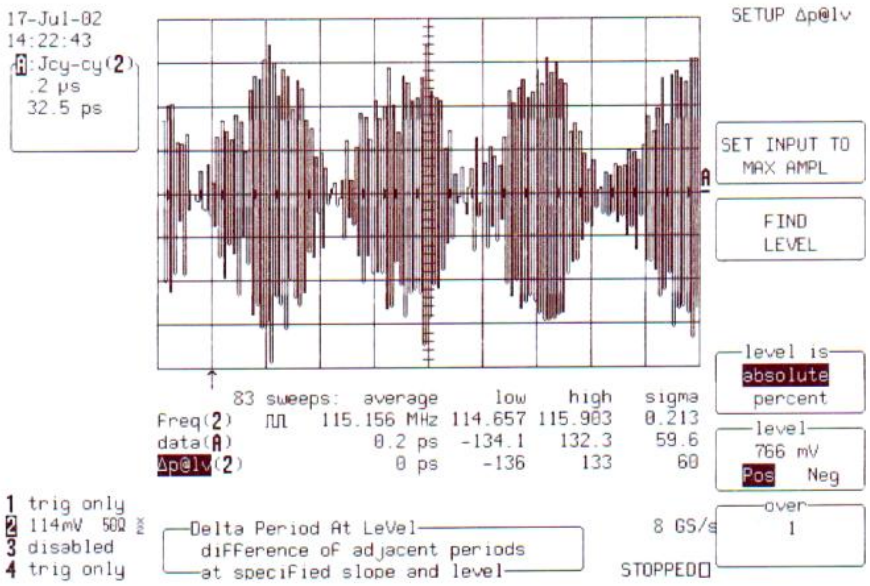


Figure 95: Periodic cycle-to-cycle jitter

Increasing jitter with decreasing frequency can be explained by leakage on the control node(s). With the development of faster CMOS processes, effective gate length becomes shorter and gate dielectric thickness becomes thinner. Hence, the level of leakage currents becomes comparable to the operation currents of transistors in weak inversion in these processes. When on-chip filter capacitors are implemented by using NMOS transistors, the maximum tunneling leakage current on the loop filter can be as high as 80% of the charge pump current [11]. If the filter capacitor leakage current is 10% of the charge pump current, for instance, a phase error of 36° would be generated to compensate for the leakage current. In the PLL's locked state, the supply current pulses, generated by the charge pump to compensate for the gate leakage, result in a noisy VCO control voltage. A common-mode feedback circuitry seems to solve this problem at the first glance. The common-mode control scheme discussed so far, however, fails to reduce the voltage drift due to leakage at low frequencies. This is because the common-mode correction takes place for duration of a reset pulse in one period. The significance of this correction decreases with a decreasing frequency of operation. Two possible modifications to solve this issue are briefly discussed next:

1. Multiple Reset Pulses in Lock: Multiple reset pulses can be generated at the lock condition instead of a single pulse. This can be realized by modifying the PFD to have a lock characteristic as depicted by *up'* and *dn'* in Figure 96. The modification can easily be implemented by using internal signals in the divider chain as shown in Figure 97. In the given implementation four reset pulses are generated in a period. The number of pulses can be increased to 16 or 32 by feeding a higher frequency internal signal from the divider chain.

2. Adaptive Multiple Pulses in Lock: Since the leakage problem becomes more significant at lower frequencies, an adaptive control that allows longer time for correction at lower frequencies could reduce jitter more significantly. This can be achieved by modifying the PFD to generate *up''* and *dn''* in lock as shown in Figure 96. A possible high-level implementation for this modification for frequency-adaptive common-mode control is demonstrated in Figure 98.

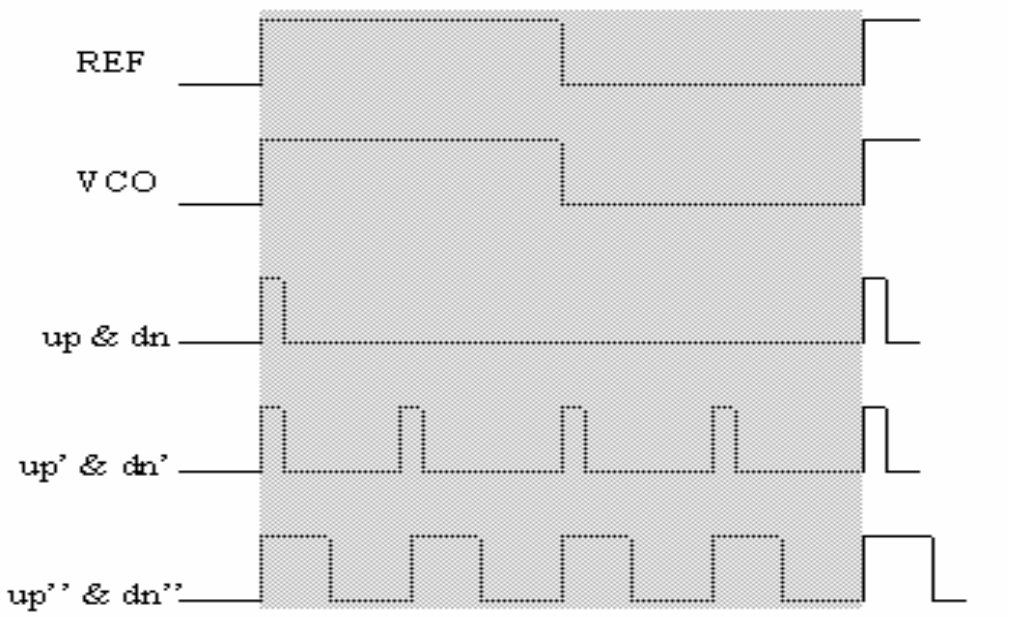


Figure 96: Conventional and modified PFD outputs in lock

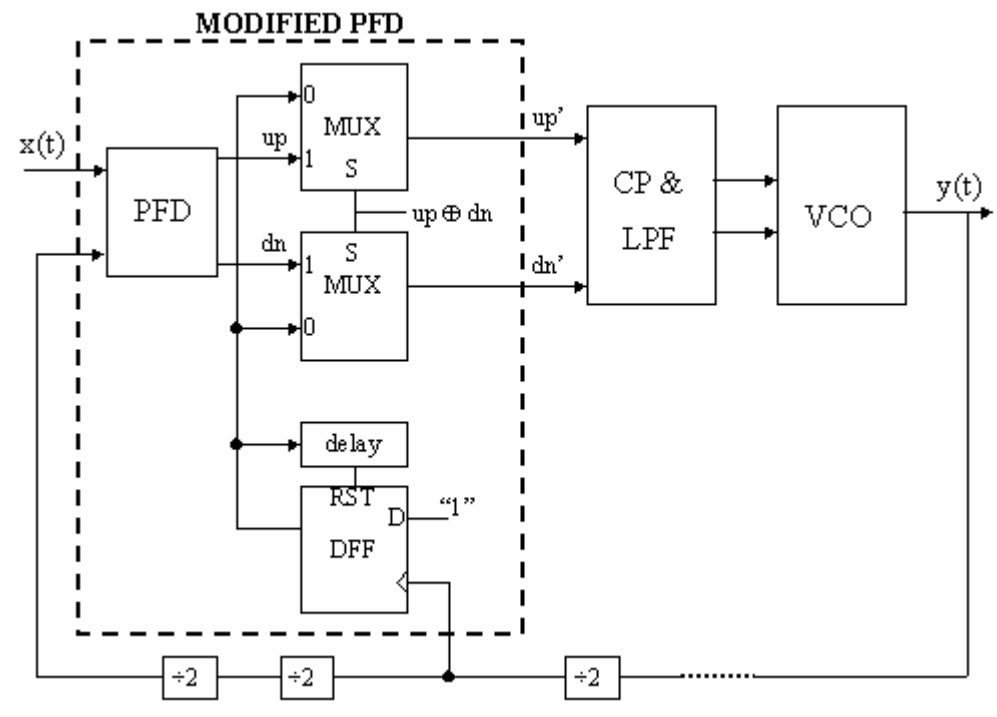


Figure 97: Generation of multiple reset pulses in lock

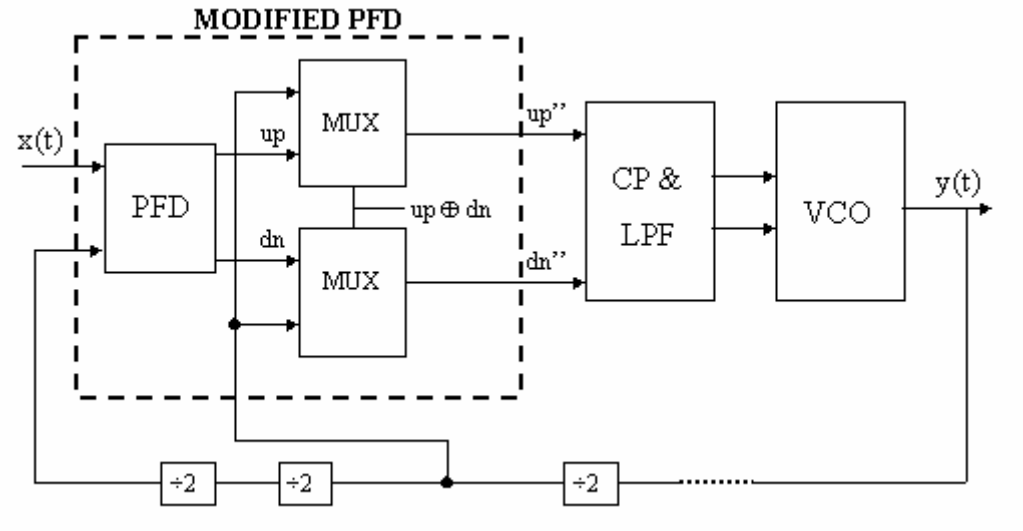


Figure 98: Generation of adaptive multiple pulses in lock

The best-case analysis for the phase skew is summarized in Table 11 for the conventional loop versus the two modified loops. A charge pump current of 70 μA, a leakage current of 7 μA (10%), a maximum charging current of 100 μA (charging current modulated by the CMFB), and a reference frequency of 25 MHz are assumed.

Table 11: Static phase error estimations

Type of the Loop	Minimum Phase Error
Conventional Loop	33.4°
Modification 1 (4 pulses)	25.7°
Modification 1 (8 pulses)	15.4°
Modification 2	0° *

*Circuit mismatches and nonlinearities cause nonzero phase error in practice.

For the proposed charge pump with sampled-data common-mode feedback, both longer reset pulses and increased number of pulses can improve the static phase error by a factor of

$$\frac{\Delta\Phi_{offset}}{\Phi_{offset}} = M\,\frac{t_{reset}}{T}\,\frac{\Delta I_{CMFB}}{I_{leak}} \qquad \textbf{(44)}$$

where $\Delta\Phi_{offset}$ is the improvement in the output phase offset Φ_{offset}, t_{reset} is the reset pulse width of the PFD, T is the period of the PFD inputs, ΔI_{CMFB} is the difference between charging and discharging currents driven by the CMFB, M is the number of pulses, and I_{leak} is the leakage current in a charge pump output node.

Equation 44 suggests that retaining low phase offset gets harder with increasing clock period. Therefore, M needs to be increased for remarkable improvements in phase skew at very low frequencies. For example, as shown in Table 11, more than 50%

improvement is achieved by inserting 8 short pulses (Modification 1), where the phase skew is reduced as low as 4.3% of the clock period.

In addition to the enhancement in static phase error, the insertion of extra pulses also lowers the magnitude of the ripple on the control line. This is demonstrated by HSpice simulation results for various leakage levels in Figure 99 and 100.

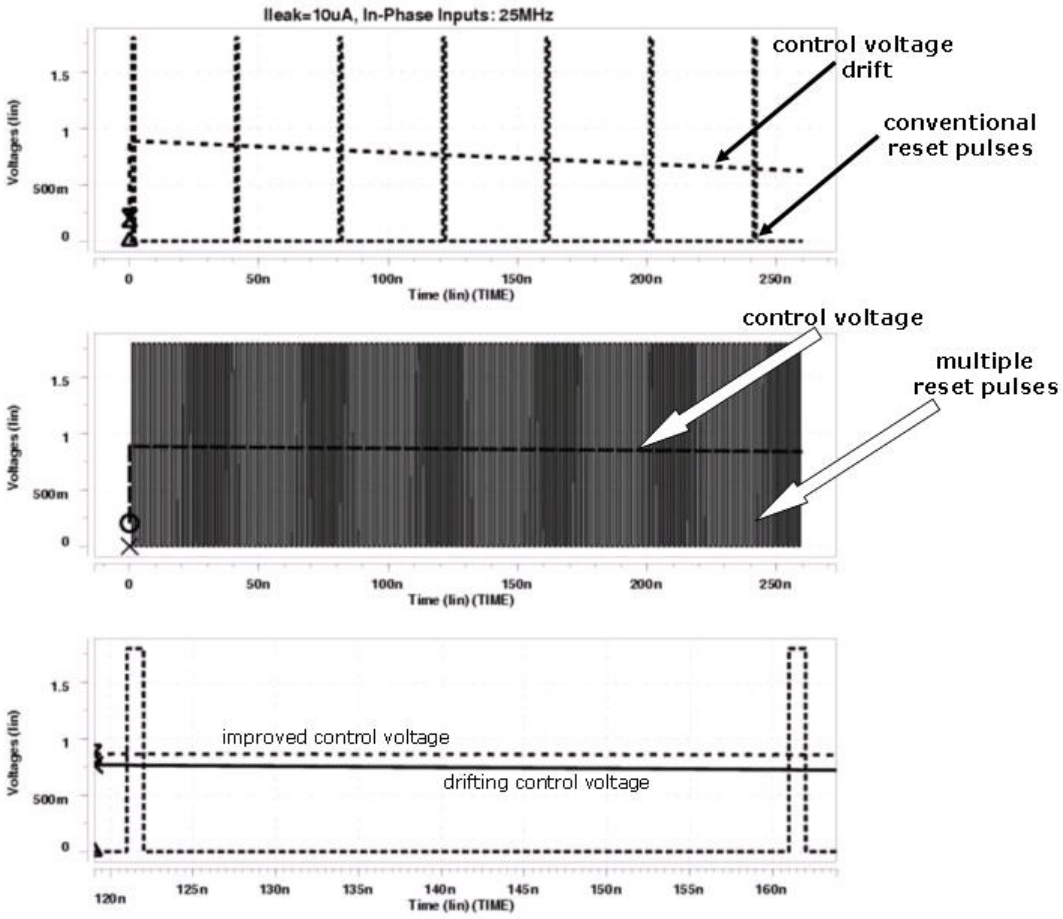


Figure 99: Control voltage drift and improvement for I_{leak} = 10μA

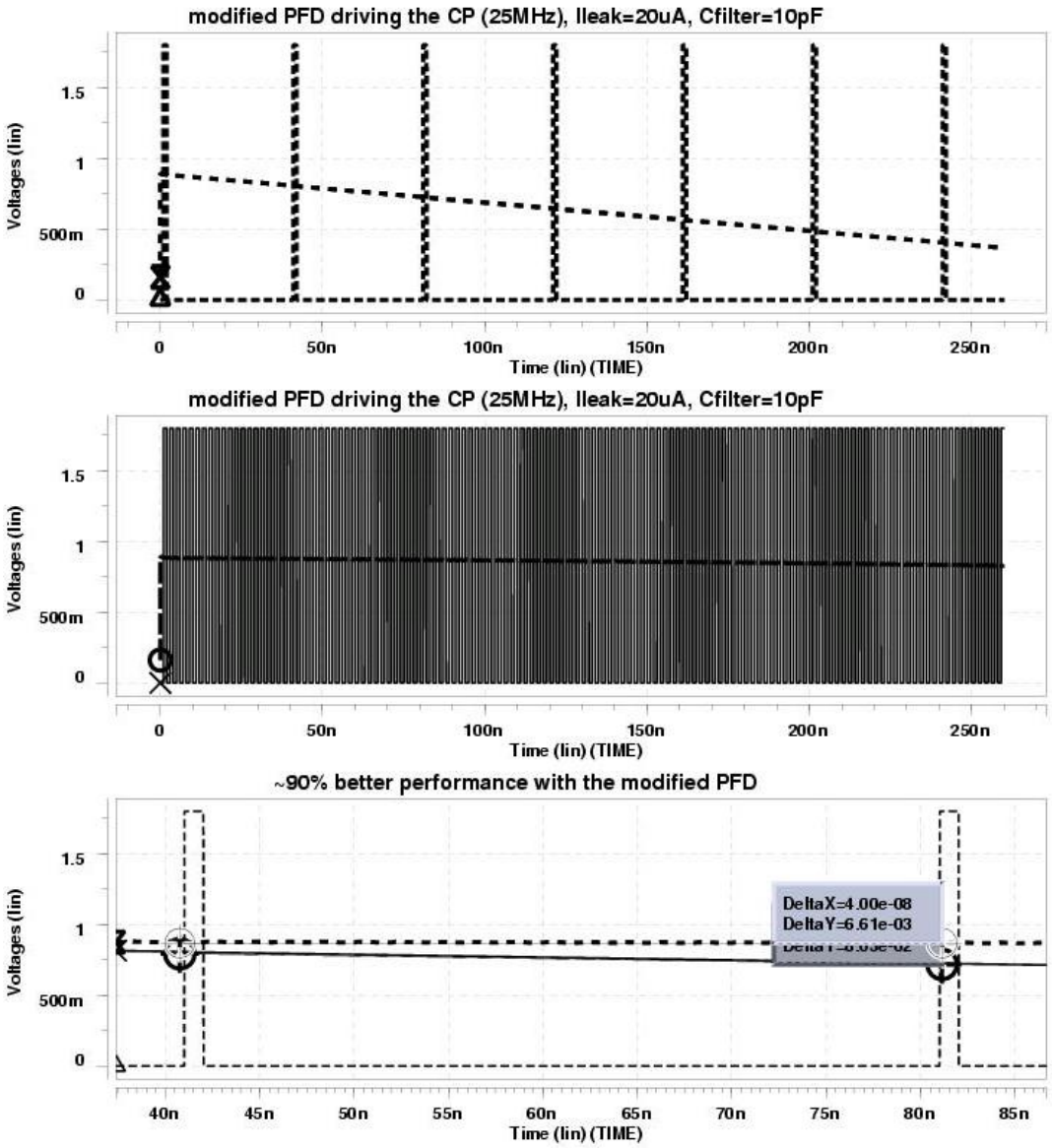


Figure 100: Control voltage fluctuation and improvement for I_{leak} = 20μA

In Figure 100, the ripple magnitude is reduced by 90%. At first, this improvement may not seem necessary since the differential control, ideally, would reduce the effect of common-mode drift. Even if this were the case, the loop dynamics would change as both control voltages drift from their original values without a differential change, causing the PLL to lose lock.

The analysis for an architecture using Modification 2 is also similar. The improvement for the drifting control voltage, in this case, is demonstrated in Figure 101.

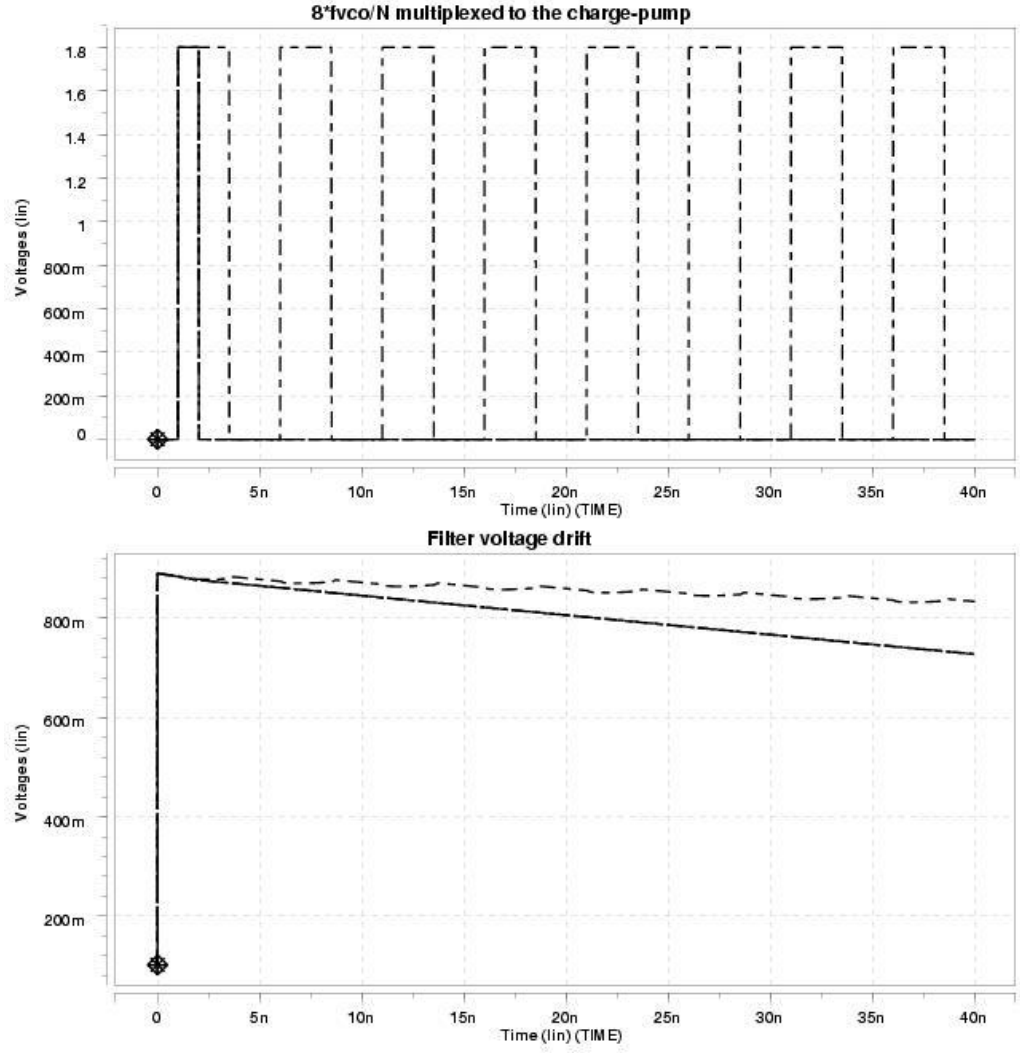


Figure 101: Control voltage drift and improvement by second modification

CHAPTER VII

PULSE STREAM CODED PHASE-LOCKED LOOPS

Recently designed high-performance systems have shown that submicron CMOS devices can be used to achieve multi-GHz operating frequencies. Reducing the channel length and the gate dielectric thickness to achieve faster operation requires a drop in the power supply voltage to avoid gate breakdown and punch through. Analog circuit design in a low-voltage submicron process is complicated by the fact that the linear operation range of the circuits is reduced and the leakage currents in weak inversion become comparable to the bias currents. Furthermore, switching noise from digital blocks on the same silicon die may couple through the power supply and the substrate into noise-sensitive analog circuits [11, 77]. All of these nonlinearities become significant in a basic charge-pump PLL (CPPLL) since it is designed using mostly analog blocks. As already discussed, a digital input block (PFD) measures the phase difference between the reference (REF) and the oscillator (VCO) signals to generate UP/DN pulses in a charge-pump PLL. These digital signals, in turn, produce current pulses to create an analog control voltage on the filter capacitor (V_{ctrl}). This whole operation can be redrawn as shown in Figure 102 to fit in the PLL structure generalized in Section 2.1, Figure 2.

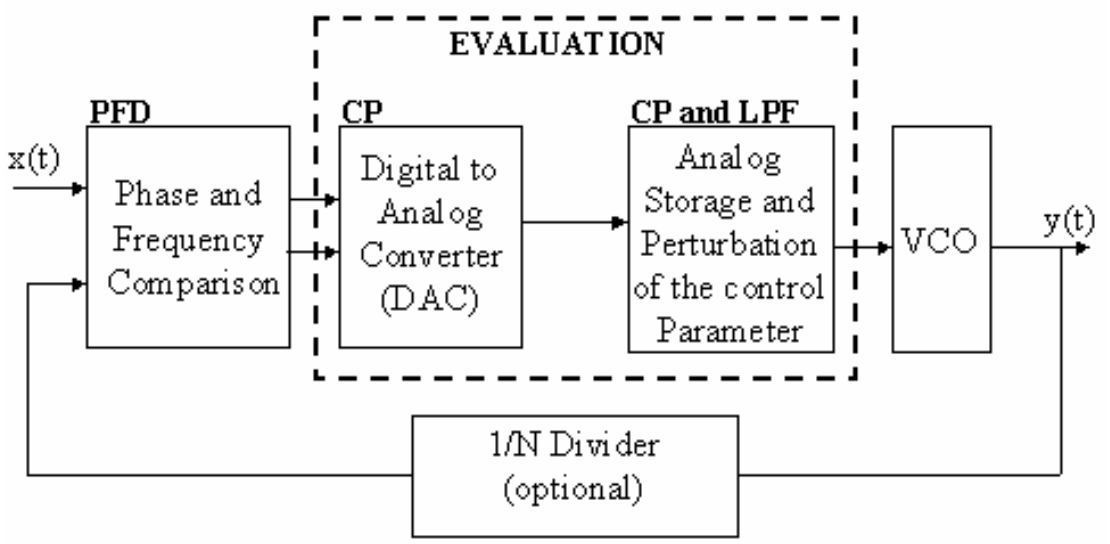


Figure 102: The charge-pump PLL

The subthreshold leakage current and the leakage current caused by tunneling charges between the gate and the inversion channel do not affect the functionality of digital circuits. They do, however, affect the operation of analog circuits. The control variable V_{ctrl} is an analog voltage that is updated at the input frequency rate in the CPPLL. The nonlinearities and noise sensitivity of the analog circuits are the main issues for the CPPLL design in future CMOS technologies.

One of the other limitations is the limited acquisition time due to the evaluation of the frequency difference by means of the phase difference in a conventional CPPLL. Fast acquisition is gaining importance in some specific applications such as low-power microprocessors employing various power management techniques. The acquisition time is inversely proportional to the loop bandwidth (BW). However, an enhancement of the acquisition time through wide loop bandwidth results in increased input phase noise.

Another limitation of charge-pump PLLs comes from resistors and capacitors used in the loop filter. A charge-pump PLL often employs a series RC loop filter to store the control voltage of the VCO. The leakage problem in submicron processes has already been discussed. Yet, another important issue is the series resistor (R) that is used to give a left-half plane zero to stabilize the loop. The effectiveness of the technique is limited by process, voltage, and temperature (PVT) variations of the resistance. The values of resistors and capacitors in the loop filters are unalterable, once implemented. Process variations alone may give 30% variation in the resistance of an ion-implanted resistor in a digital CMOS process [14]. Since the damping factor is proportional to R, the loop stability changes dramatically with PVT variations. Moreover, these passive loop components consume a large amount of precious silicon area, and their values are unalterable once implemented.

Several problems with performance enhancement and precise oscillator control using analog circuits in low-voltage submicron CMOS processes, coupled with the fact that analog (or semi-digital) oscillators having various advantages over their digitally controlled counterparts, prompted the proposal of the digitally-controlled phase-locked loop. The proposed architecture is given in Figure 103 at its highest level. The blocks other than the digital-to-analog converter (DAC) and the VCO/CCO are designed by using digital techniques. First of all, digital design of the control provides possibilities for enhanced performance in current low-voltage submicron CMOS processes with a tolerance to process variations. Secondly, loop design becomes flexible (semi-custom) and the digital data allows the implementation of modified feedforward algorithms easily and precisely (i.e. adaptive loop bandwidth). Besides these advantages, internal loop

states and digital control words can be monitored without any significant effect on the loop operation.

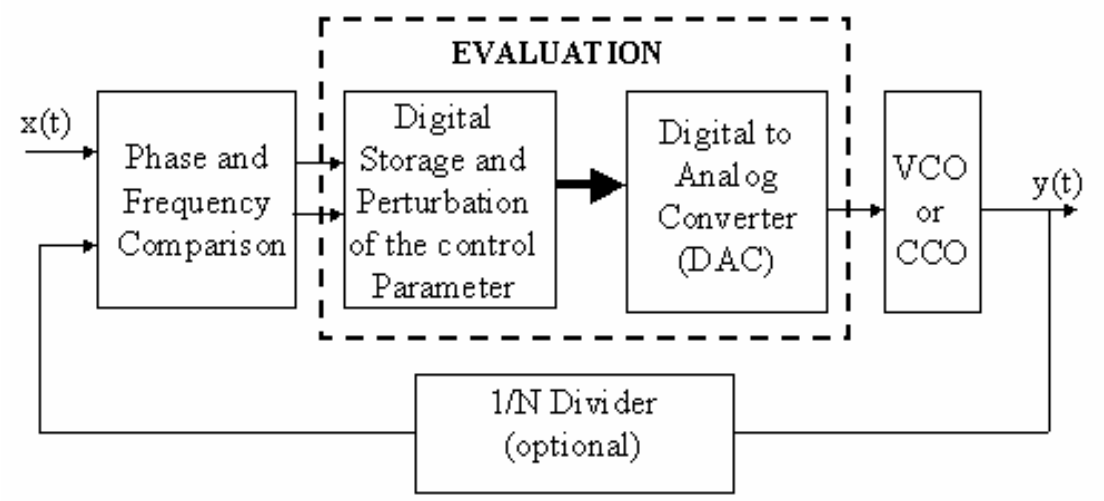


Figure 103: Proposed PLL architecture

Fundamentally, this chapter focuses on producing a control signal (a digital word in this case) that is less sensitive to variations in a submicron process. Particular emphasis is on merging the advantages of digital circuits with those of analog circuits for a more stable control voltage/current generation to achieve higher precision in oscillator control. A novel method for digitization is proposed where trains of pulses code the phase/frequency comparison information rather than the duration of the pulses. This aspect of the design also releases the constraint on the requirement of a loop filter for stability. The digital control word is then used to drive a differential analog oscillator. The proposed research examines problems at both the circuit level and the architecture level based on digitized control of the VCO/CCO to gain precision.

7.1 Digitization of the Oscillation Control

The proposed PLL architecture consists of a digital PFD, digital processing and storage, a digital-to-analog converter, and an analog VCO/CCO. It is important to notice that the design is based on the conventional charge-pump PLL, and the proposed modifications aim to still have the advantages of a PFD/CP combination in the CPPLL in that it will null the static phase error and have a wide frequency capture range.

The modified phase-frequency detectors proposed in this research generate trains of short pulses to enable fast acquisition and to render a digital design of the control loop. Thus, providing many advantages to the designers. There are almost infinite options to process the PFD data before the digital-to-analog conversion. Two different PFDs are designed as each can find valuable usage in a different loop implementation. The pulse generation network acts as a type of low-pass filter in both designs. This is an important advantage of the proposed designs, since the left half-plane zero assignment of the traditional CPPLL by using resistors is automatically eliminated. These designs operate independent from the input duty cycle, and they allow an unlimited capture range.

7.1.1 Dual Pulse-Train PFD

In the dual pulse-train PFD (dpt-PFD), the number of pulses determines how much the VCO must speed up or slow down to achieve the lock. The direction of the change is determined by which of the two outputs is carrying the pulses. The outputs of the dpt-PFD are shown in Figure 104 together with the gate-level schematics. When the VCO signal is leading, a train of pulses are generated at the DOWN (DN) output instead of a long pulse in the conventional counterpart. Similarly, the pulse train is generated at the

UP output if the VCO signal lags the reference signal (REF). The operation of this PFD is the same as the conventional PFD when both inputs are in phase.

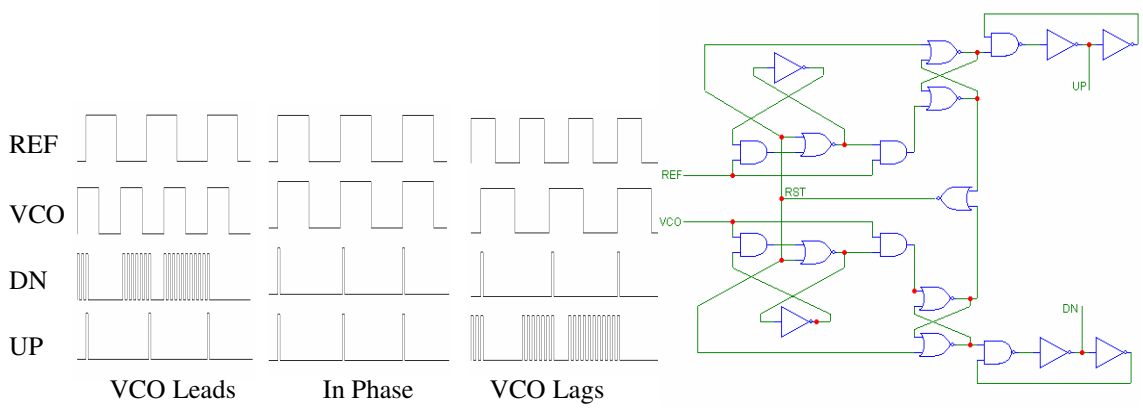


Figure 104: Dual pulse-train PFD operation and schematic

7.1.2 Single Pulse-Train Phase-frequency Detector

The operation and gate-level schematic of the single pulse-train PFD (spt-PFD) are slightly different, and are shown in Figure 105. The MODIFY (MOD) signal drives the VCO frequency adjustment whereas the DIRECTION (DIR) signal determines the direction of the modification. When there is a phase/frequency difference between the two input signals, VCO and REF, a pulse train is generated at the MOD output. This corresponds to the need for a VCO control voltage modification whose direction (speed up or slow down) is determined by the DIR output. The DIR signal is useful only when there's a pulse at the MOD output to trigger a change in the evaluation stage. However, these two signals need to be aligned since there is no symmetry issue at the generation of the two signals.

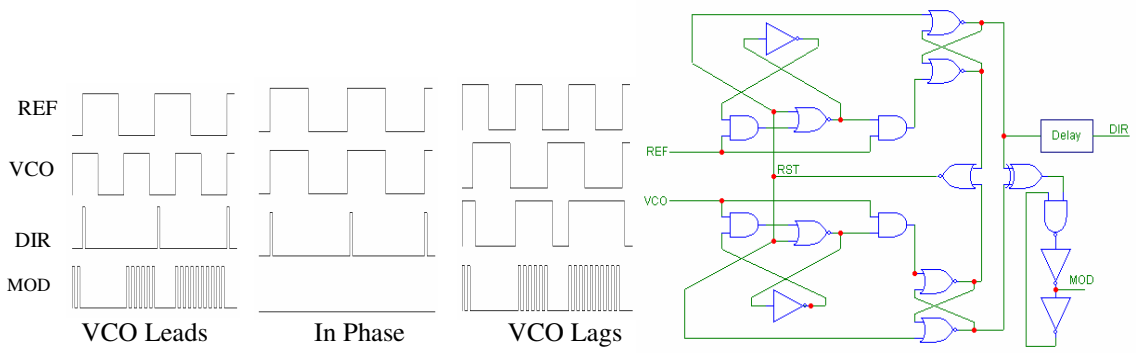


Figure 105: Single pulse-train PFD operation and schematic

7.2 A Simplified Pulse-Stream Coded PLL

A simplified version of the phase-locked loop that incorporates the modified sequential logic PFD with pulses (spt-PFD) is designed for testing the basic characteristics of the system. The goal of the design (Figure 106) is to develop a better insight into critical system parameters (the pulse width, the resolution, the power-up characteristic, and the digital word length) of this novel design. For this purpose, the initial work concentrates on low-frequency implementation.

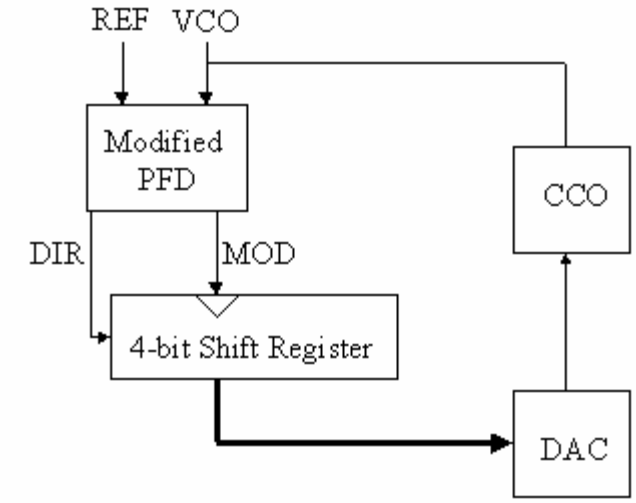


Figure 106: Functional block diagram of the prototype design

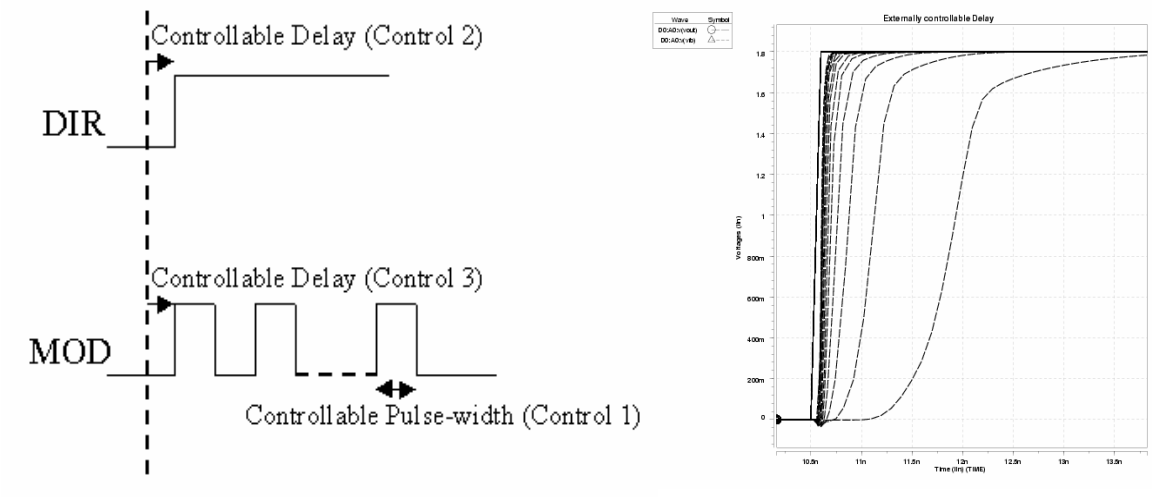
The operation of the proposed design in its simplest form is very similar to the charge-pump PLL operation. The phase-frequency difference between the reference signal REF and the oscillator signal VCO (this notation is used for consistency even if the oscillator in the design is a current-controlled oscillator) results in a train of pulses, the number of which is directly proportional to the phase difference. These pulses clock the 4-bit shift register whose serial input is

- a "1" if the reference signal is leading the oscillator signal
- a "0" if the reference signal is lagging the oscillator signal.

The digital word stored at the 4-bit shift register is converted to an analog current level by the monotonic digital-to-analog converter (DAC). Therefore, if the reference signal is leading the feedback signal, for example, a "1" is shifted into the register. Depending on the rightmost bit at the previous MOD edge, the overall number of "1"s is either increased or kept constant (the loop will keep feeding in a "1" into the shift register until DAC output is increased unless it is already saturated). The total number of high bits determines the oscillator control current.

In the prototype design, the spt-PFD is implemented such that, the pulse width can be changed by an external control pin if needed (Control 1). The outputs of the PFD have externally controllable delay elements for aligning the two output signals, MOD and DIR (Control 2 and Control 3). All these three controls are realized by using externally adjustable current mode logic gates. Current-mode inverters are used at the MOD output generation and simple differential amplifiers are employed as delay stages. The reason for choosing current input as an external control is to decrease the effect of any possible noise in control lines. The three control parameters discussed so far are demonstrated in

Figure 107(a). The pulse-width control, Control 1, can change the pulse-width from 1ns to 1.6 ns to alter the number of pulses generated for a given phase difference. The delay with respect to the control voltage (generated by replica biasing from Control 2 or Control 3 currents) is shown in Figure 107(b) where it can be set from 0.2ns to 1.5ns.



(a) (b)

Figure 107: (a) Parameterized modified-PFD outputs (b) external delay control

The 4-bit shift-register is composed of 4 D-flip-flops (DFF) with resets. The static DFFs are designed to operate above 0.5 GHz. The DAC is a simple current mirror based monotonic design that converts the digital word carrying the frequency information into an analog current value. All bits from the shift-register are equally weighted for simplicity. The output of the DAC has five levels:

$$I_{DAC} = n\, I_{STEP} \text{ and } n = 0, 1, 2, 3, \text{ or } 4 \qquad \textbf{(45)}$$

where I_{DAC} is the output current of the DAC and I_{STEP} is the step current corresponding to each active bit. The fourth parameter of the prototype, Control 4, alters I_{STEP}. Hence,

none of the shift register bits has significance over another. Only the number of high bits in the register counts to determine the DAC output level as is clear from the simplified schematic in Figure 108.

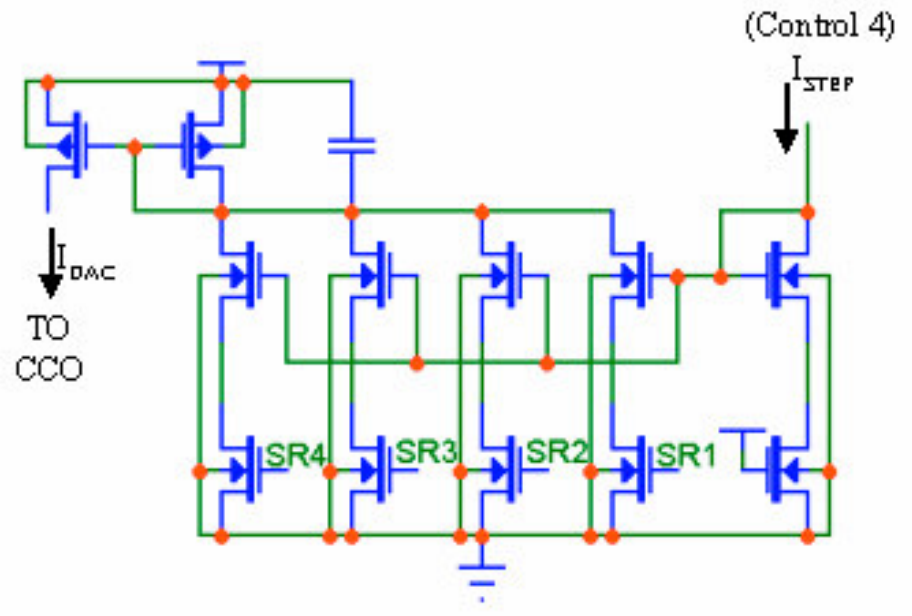


Figure 108: Simplified circuit schematic of the DAC

The current additive property and the linear frequency-to-current characteristic of a CCO simplify the system design. The operation principle of the CCO can be described with Figure 109 and the following simple equations:

$$I_{CCO} = I_{DAC} + I_{BIAS} \quad \textbf{(46)}$$

$$\text{Frequency } (I_{CCO}) = \text{Frequency } (I_{DAC} + I_{BIAS}) \quad \textbf{(47)}$$

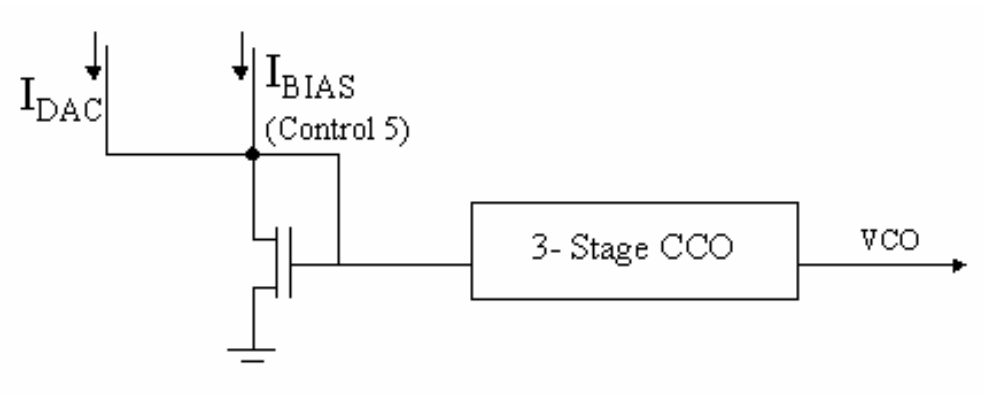


Figure 109: CCO control

Within the region that the CCO has a linear current-frequency (I-F) characteristic, Equation 47 can be rewritten as follows:

$$\text{Frequency } (I_{CCO}) = n\,[\text{Frequency } (I_{STEP})] + \text{Frequency } (I_{BIAS}) \qquad \textbf{(48)}$$

where I_{STEP} and I_{BIAS} can be externally controlled by the control input currents Control 4 and Control 5, respectively. I_{BIAS} can be set properly to allow the free-running CCO to operate at the left edge of its linear range and I_{STEP} can be set to allow the CCO to run still in the linear region for a total current of $I_{BIAS} + 4I_{STEP}$. The designed CCO is a 3-stage ring oscillator utilizing active load differential-pair delay stages as shown in Figure 110. The circuit is designed to perform linearly from 100 MHz to 200 MHz. A differential design is preferred for a better immunity to the supply noises.

The functional block diagram of this highly parameterized test unit is shown in Figure 111 together with its layout in TSMC's 0.18 μm technology.

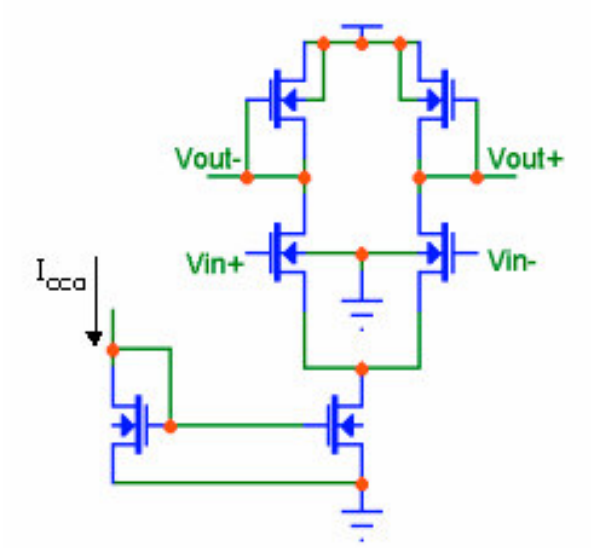


Figure 110: Differential oscillator delay stage

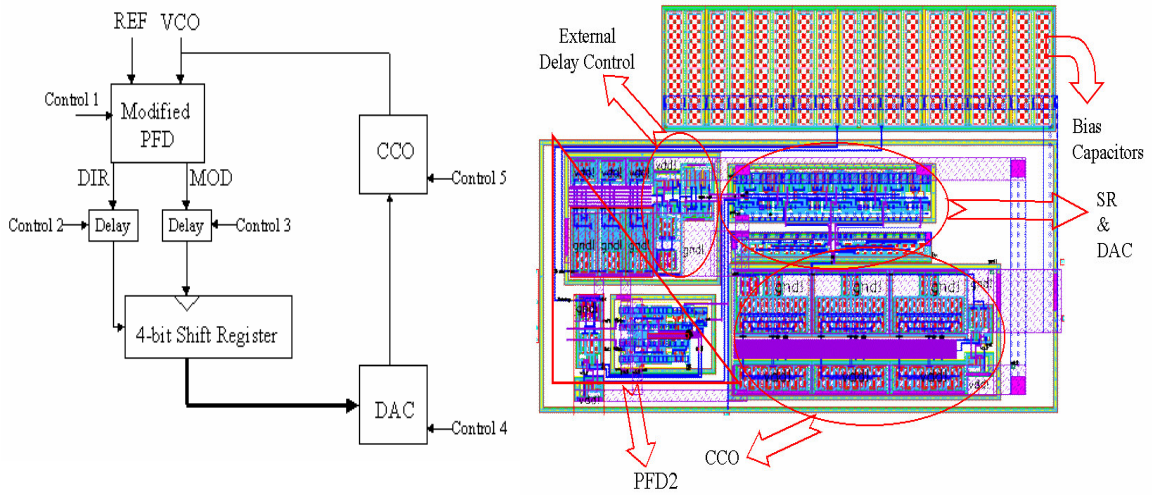


Figure 111: Parameterized block diagram and the layout

The open-loop operation is demonstrated next (Figure 112) after setting all the parameters properly. To allow the verification of the operation in the VCO leading and lagging cases, a frequency modulated reference signal is used as seen on the first row of the plots below. The second row shows the pulses generated by the modified PFD, whereas the next four rows show each register bit. The last row shows the five different levels of the DAC output, which increases or decreases with the VCO leading and lagging cases accordingly.

Even though it tracks the frequency successfully, the prototype PLL fails to phase-lock due to the very low resolution defined by the equally-weighted 4-bit shift register and the DAC. The DAC determines the resolution for a given oscillator gain. The linearity metrics of a DAC (integral and differential nonlinearities) which are critical in most applications are not as important due to continuous correction of the nonlinearity by the feedback. On the other hand, high resolution and monotonicity are required to enhance the proposed PLL's performance. In this aspect, using equally weighted bits causes a low efficiency usage of the bits such as, if binarily-weighted, 4-bits map to 2^4=16 analog levels rather than 5. However, a more sophisticated modification block than the simple shift register is needed to employ a binarily-weighted DAC while the monotonicity is satisfied.

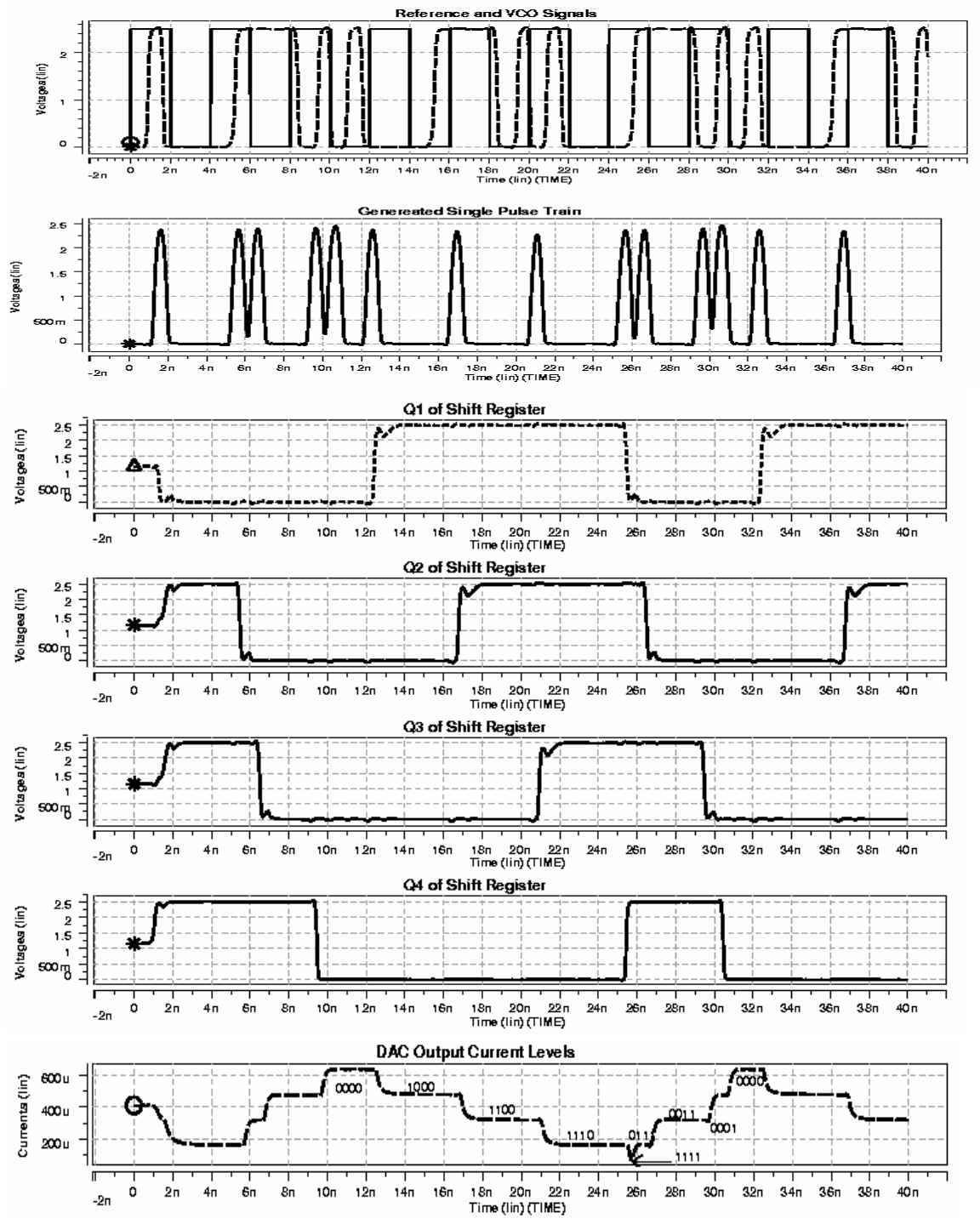


Figure 112: Open loop simulation of the prototype PLL

Another weakness of the design caused by the shift register can be best understood with an example shown in Figure 113. As demonstrated by the example, a change in the CCO control current by a single step can take as many as four MODIFY pulses instead of a single pulse. This shows how the fast acquisition property of the modified PFD cannot be taken advantage of by the prototype design.

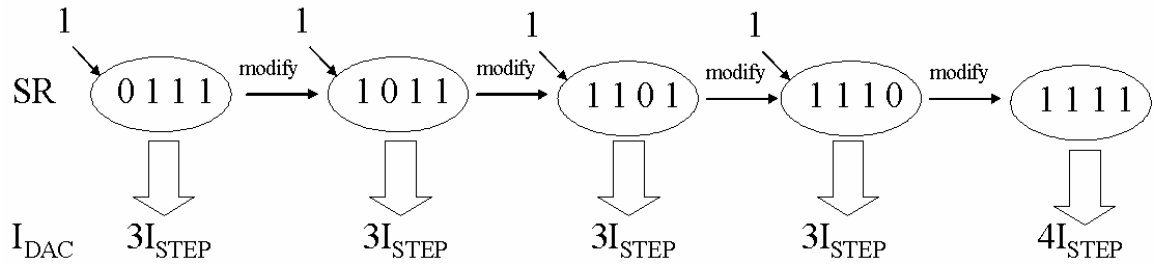


Figure 113: Shift register update example

7.3 Next Generation Pulse-stream Coded PLL

The problems with the shift register lead to the utilization of alternative blocks for the next generation design. The shift register in the proposed architecture can easily be replaced by an up/down (UP/DN) counter to solve these problems, shown in Figure 114. This modification also requires the design of a binarily-weighted digital to analog converter.

In the proposed architecture, extra phase noise is generated by the quantization noise of the DAC in addition to the input reference noise and the oscillator noise. The DAC related noise is a uniformly distributed noise that is uncorrelated with the rest of the contributors. A current-controlled oscillator with 100 KHz/μA gain and 100 MHz tuning range can be driven by an 8-bit binarily-weighted DAC to generate less than 40 ps of

quantization noise. The effect of number of bits on the quantization noise is shown in Figure 115, where quantization noise lower than 10 ps can be achieved by a 10-bit DAC for the given CCO. In order to obtain the same resolution, a 1023-bit shift register is required which would drastically slow down the acquisition (as many as 1023 cycles) for a single bit modification as demonstrated in Figure 113. Hence, the use of a counter does not only increase resolution with reasonable number of bits, but also does it satisfy the monotonicity with higher efficiency.

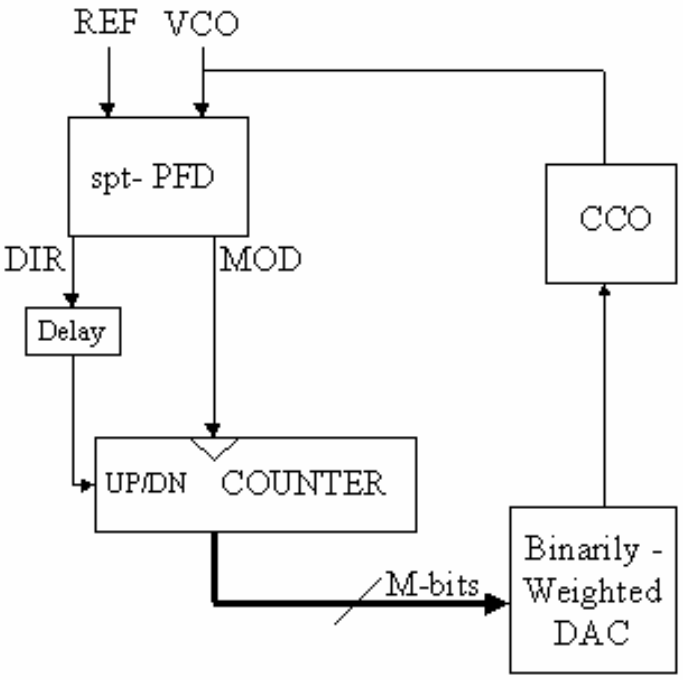


Figure 114: Proposed architecture utilizing an UP/DN counter

Next, critical control parameters are investigated in a bottom-up manner to explore the performance limits of the psc-PLL. Simulations are carried out in TSMC's 0.18 μm process, because earlier measurements of both digital and analog blocks were very close to the simulation results. Parasitics are included in all simulations.

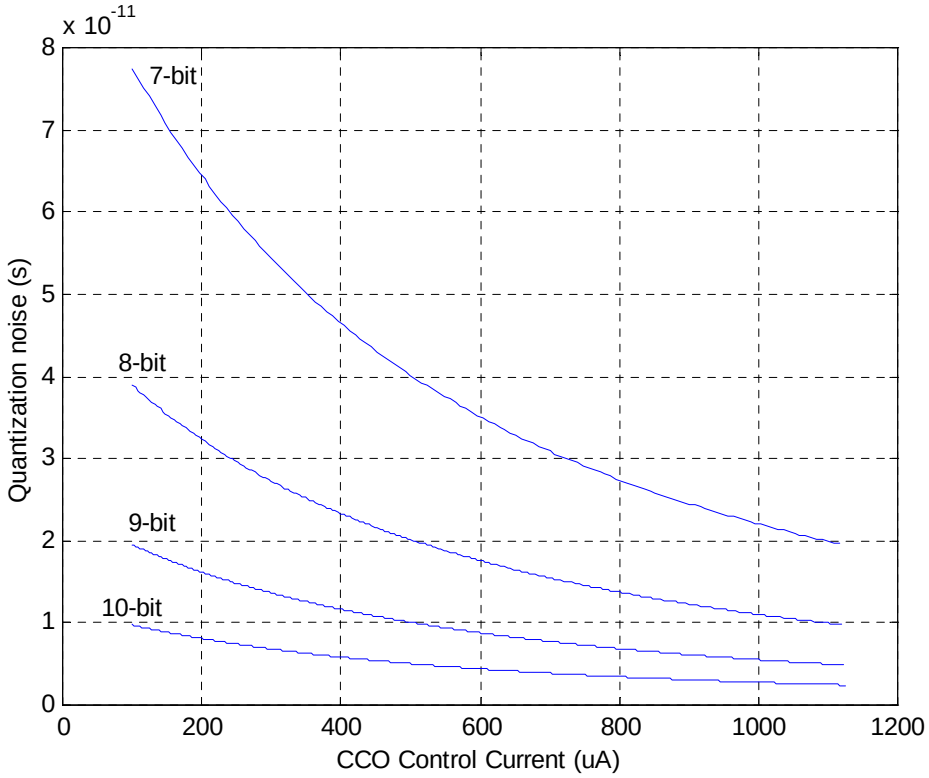


Figure 115: Oscillator output resolution with DAC quantization

7.3.1 Single Pulse-Train PFD Implementation

The pulse-stream coding is rendered by the novel block: single pulse-train PFD. The basics for the spt-PFD operation were summarized in Section 7.1.2. The characteristic for the *MODIFY* output of the spt-PFD is shown in Figure 116. The *DIRECTION* signal however spans the overall characteristic to match the conventional PFD characteristic, redrawn in Figure 117. Various implementations of this block are discussed here, since it is the key part to allow digital control without using complicated control units required in all-digital PLLs.

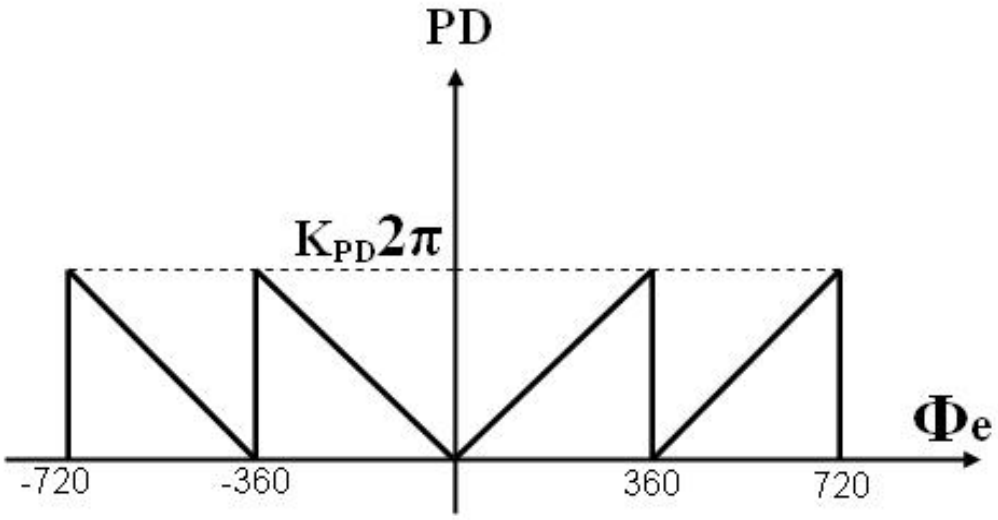


Figure 116: MODIFY output characteristic for the spt-PFD

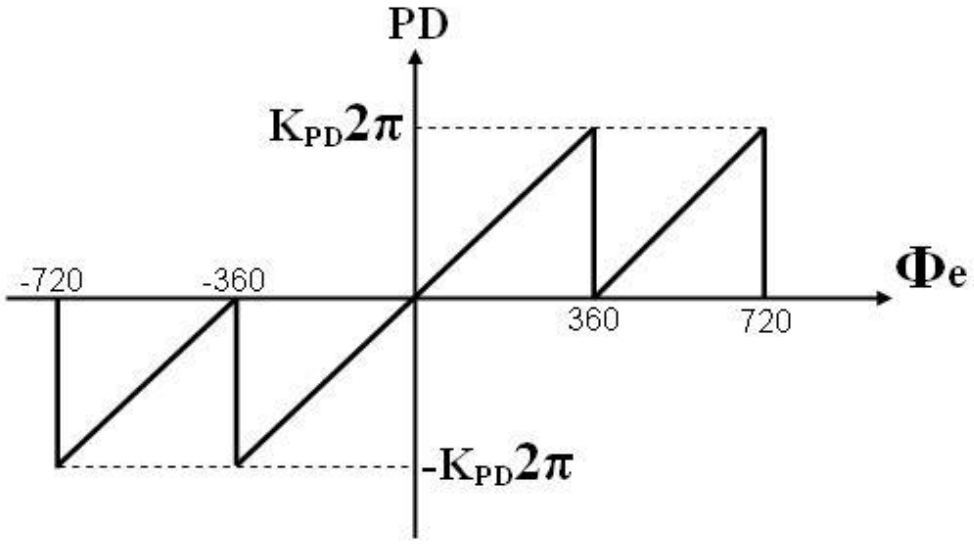


Figure 117: Overall spt-PFD output characteristic

spt-PFD with a pull-down transistor: spt-PFD1

Figure 118 illustrates the spt-PFD scheme with a strong pull-down transistor.

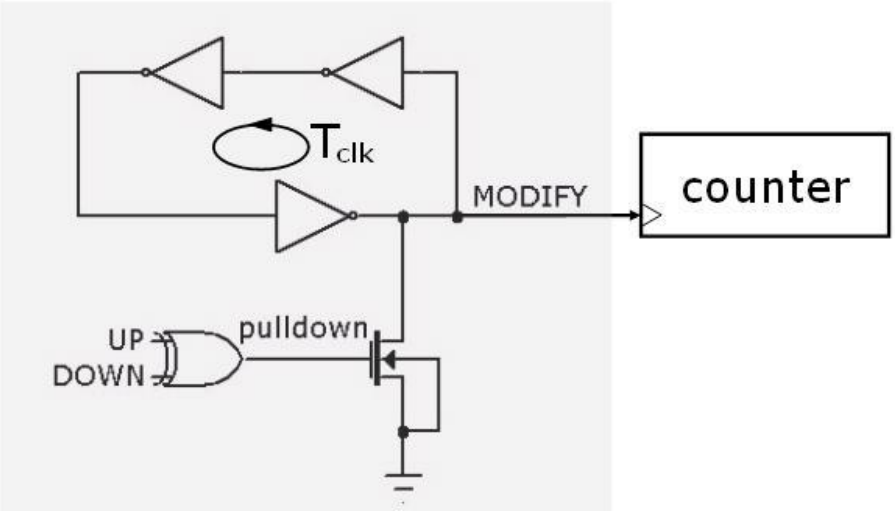


Figure 118: spt-PFD implementation with a pull-down switch

When the reference signal and the PLL output are not in phase, either one of *UP* or *DOWN* signals is high. The *pulldown* signal, in Figure 118, is pulled low to turn the pulldown transistor off. The modify signal, in this case, is a series of pulses for the duration of the input phase difference. Faster frequency tracking can obviously be achieved with a faster clock. The number of inverters in this scheme can be increased (while transistor sizing is another parameter) to rise the *modify* signal period T_{clk}. This adjustment is needed to increase the loop gain while keeping the frequency low enough for the proper counter operation. In other words, the upper bound for Tclk is determined by the PLL loop gain and the lower bound by maximum digital filter frequency.

Similarly, when *UP* and *DOWN* signals are equal, the *pulldown* signal goes high pulling the *modify* signal low. This case is depicted in Figure 119. It is important to note

that the output low voltage (V_{ol}) is determined by the relative strength of $Mn_{pulldown}$ and Mp_{inv}.

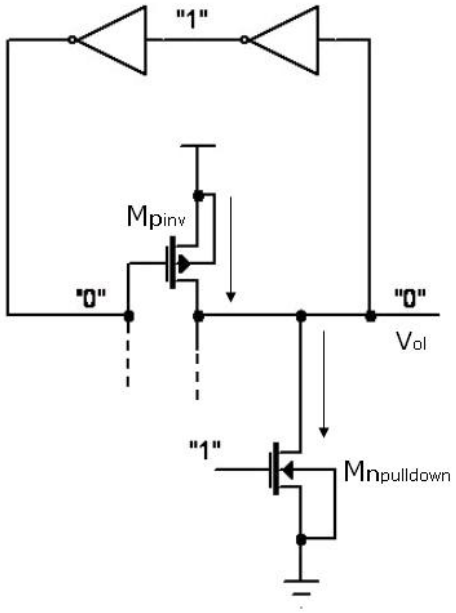


Figure 119: spt-PFD output pulled down

The implementation employing standard CMOS gates and a strong pulldown transistor is characterized as in Figure 120. The design is simulated over the process corners. The maximum and minimum values for the dead-zone are extracted as 155 ps on the slow-slow (SS) and 90 ps on the fast-fast corner (FF). HSpice simulation results at various corners are presented in Table 12.

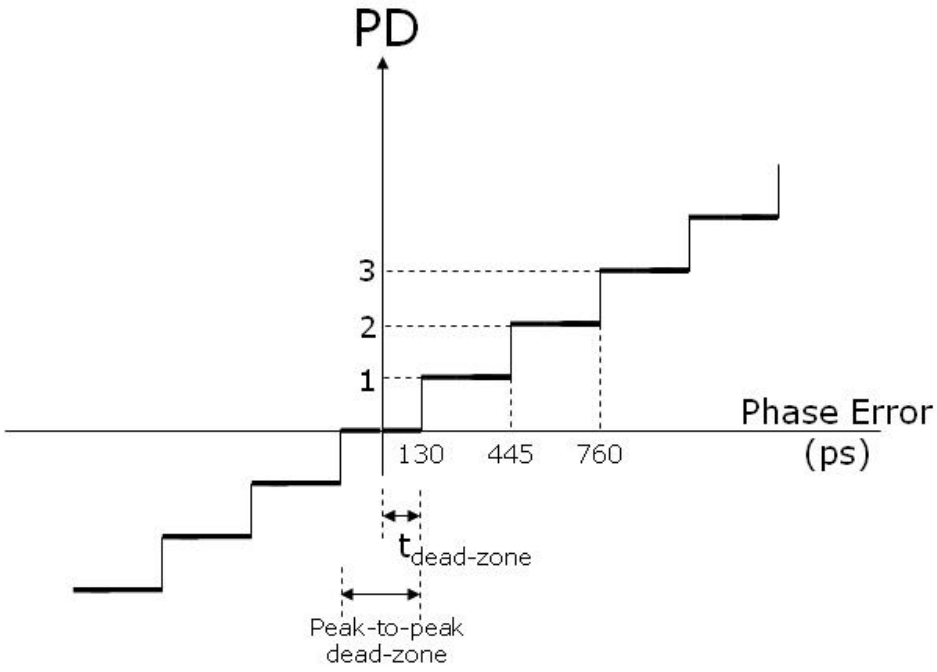


Figure 120: Dead-zone of the spt-PFD with a strong pull-down

Table 12: Dead-zone at various process corners for spt-PFD1

Model Name	Dead-zone (ps)	V_{ol} (V)	Power (mW)
Typical - Typical	130	0.22	0.6
Slow - Slow	155	0.21	0.5
Fast - Fast	90	0.24	0.75
Slow - Fast	120	0.28	0.66
Fast - Slow	140	0.18	0.56

The dead-zone can be improved by shortening the time delay to turn off the strong pulldown transistor. This improvement can be achieved in two ways:

- employing a faster XOR gate
- reducing the pulldown strength

The differential cascade voltage switch with pass-gate (DCVSPG), Figure 121, improves the pulldown release time by 70 ps. Therefore, the dead-zone is expected to fall down to 60 ps if this XOR gate is utilized. HSpice simulations show that the dead-zone is now 65 ps at the typical-typical corner without any change in power consumption or output-low voltage.

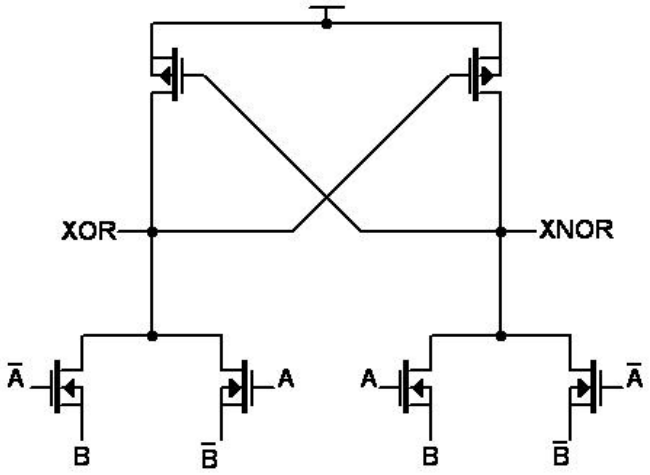


Figure 121: Differential cascade voltage switch with pass-gate XOR circuit

The modify output of the spt-PFD is pulled down to V_{ol} when both *UP* and *DOWN* signals are equal. When there is an input phase error, the pulldown transistor turns off and the *modify* signal gets pulled high. Therefore, increasing the aspect ratio for Mp_{inv} would reduce the dead-zone. Attention, however, needs to be paid since this would increase the output-low voltage which may no longer be input-low for the next inverter stage. The dead-zone and the output-low voltage variations with the relative strength of Mp_{inv} and $Mn_{pulldown}$ are summarized in Table 13.

Table 13: Relative pulldown strength variation

$Mn_{pulldown}$ (µm/µm)	Mp_{inv} (µm/µm)	$t_{dead\text{-}zone}$ (ps)	Power (mW)	V_{ol} (V)
2.6/0.2	1.6/0.2	80	0.61	0.08
2.6/0.2	2.6/0.2	70	0.99	0.15
2.6/0.2	3.6/0.2	60	1.40	0.235
1.6/0.2	3.6/0.2	50	1.40	0.514

As illustrated by the simulation results in Table 13, the output low voltage increases as the relative pulldown strength is reduced. An asymmetric inverter can be employed at the output node for proper logic generation as shown in Figure 122. For instance, V_{ol} (= V_1 when pulldown is active) must be smaller than V_{IL} of INV_n at all process corners to generate a logic "1" at the output. If V_{ol} is not lower than V_{IL}, the default output gets inverted as demonstrated in Figure 123.

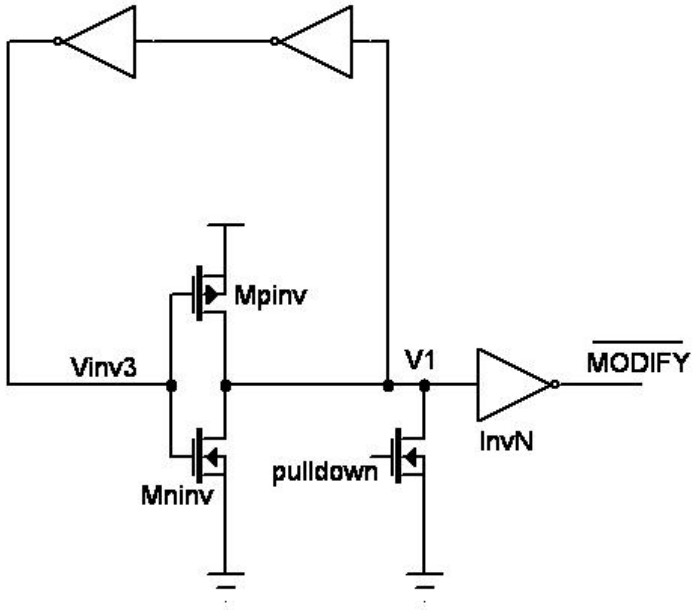


Figure 122: spt-PFD driving an asymmetric inverter

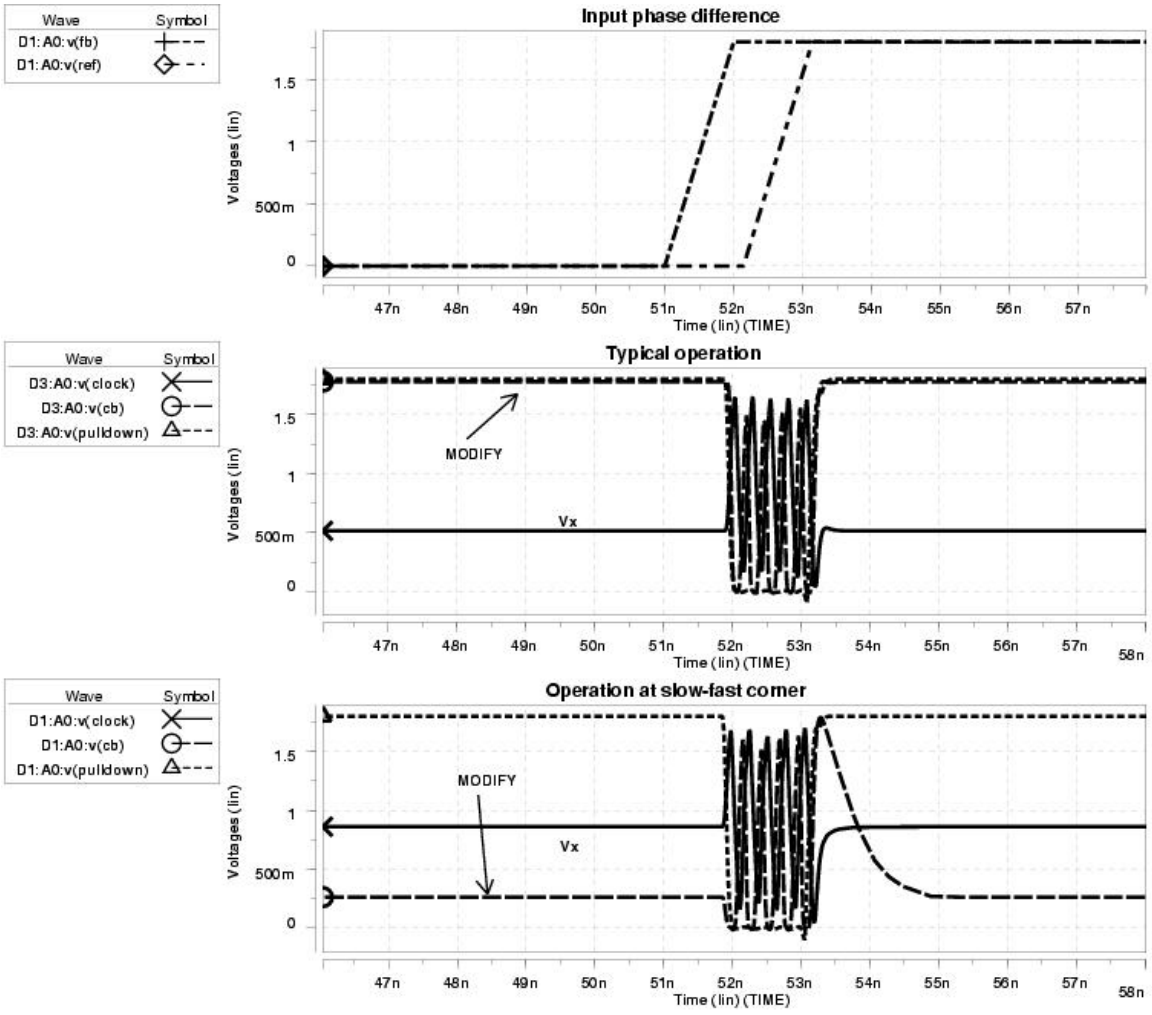


Figure 123: Default output inversion

Using the two methods described above, the dead-zone can be decreased down to 30 ps. The simulation results at the typical-typical corner are shown in Figure 124. Figure 125 exhibits operation for a larger input phase error.

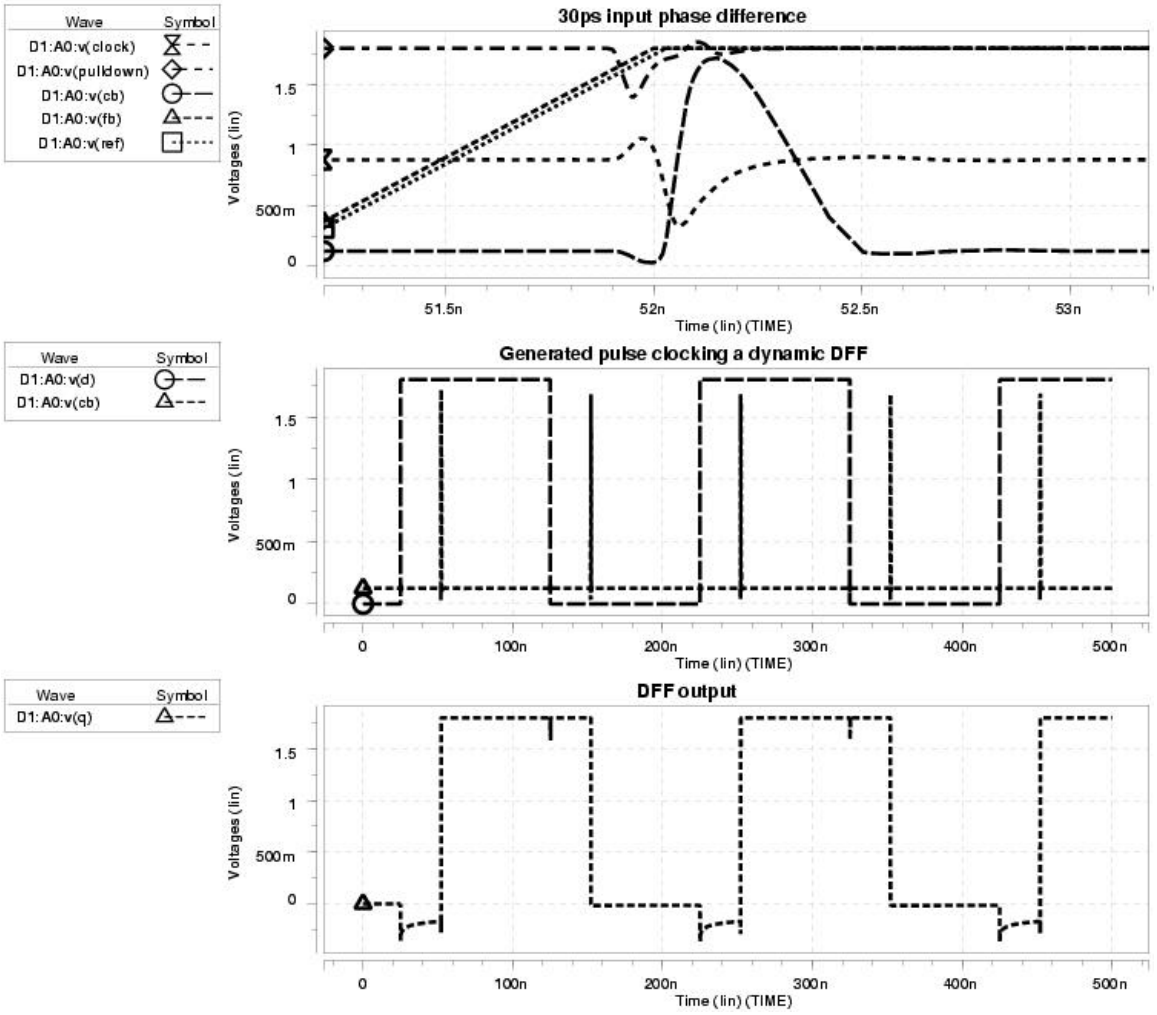


Figure 124: Improved dead-zone for spt-PFD with a weaker pulldown

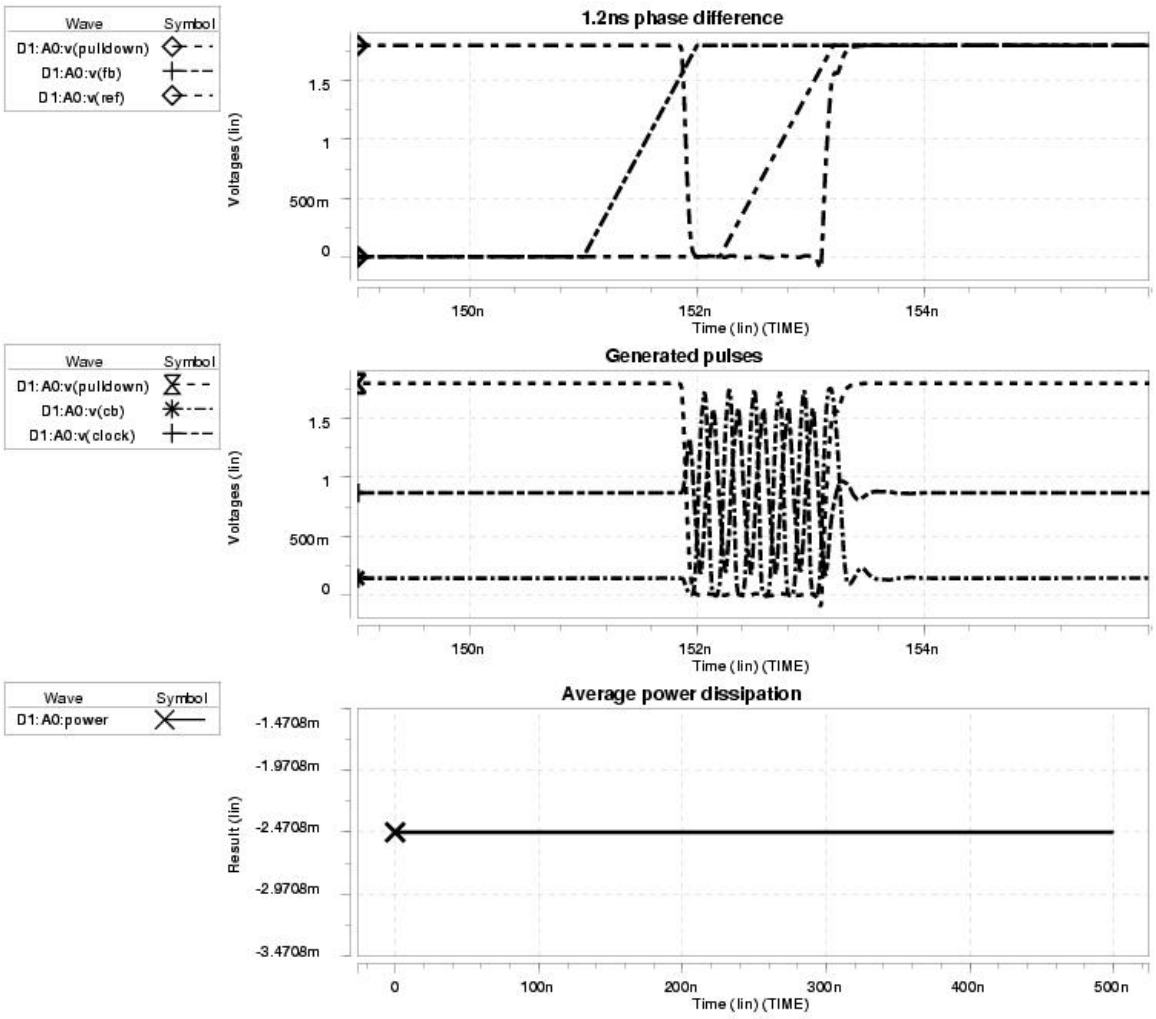


Figure 125: spt-PFD operation for a larger phase error

The drawback of the dead-zone improvement by reducing the pulldown strength is the increased power consumption (4 times larger) and noise sensitivity. The noise sensitivity is simulated with the setup shown in Figure 126, and the simulation result is shown in Figure 127.

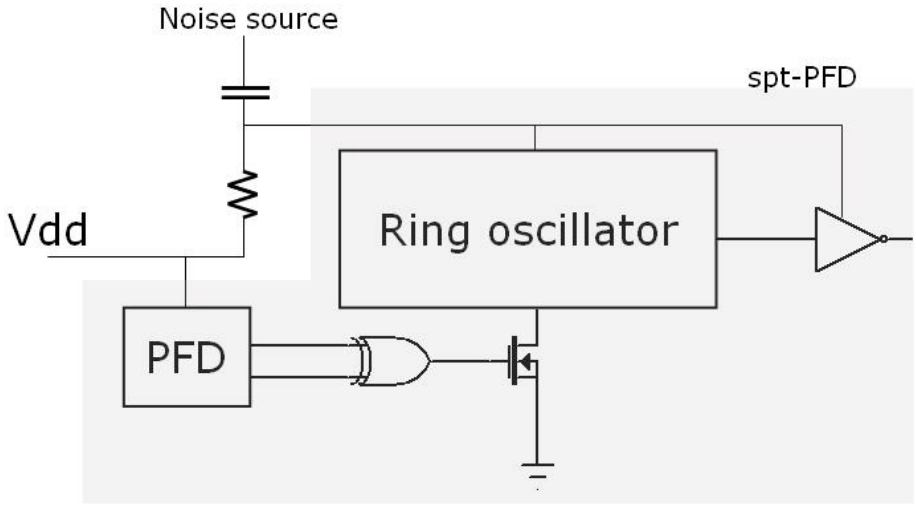


Figure 126: Noise sensitivity simulation setup

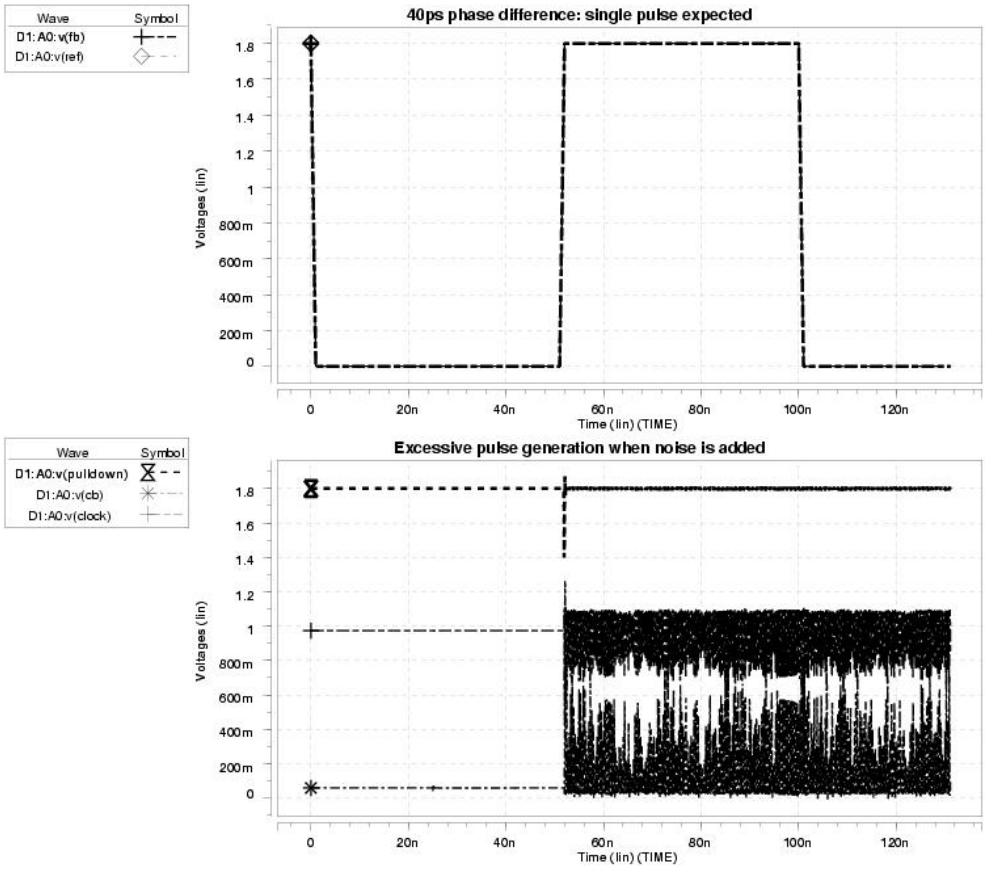


Figure 127: Noise sensitive spt-PFD output

spt-PFD with a multiplexer: spt-PFD2

Another method to implement an spt-PFD is using a multiplexer to select between pulses or GND according to the input phase difference (Figure 128).

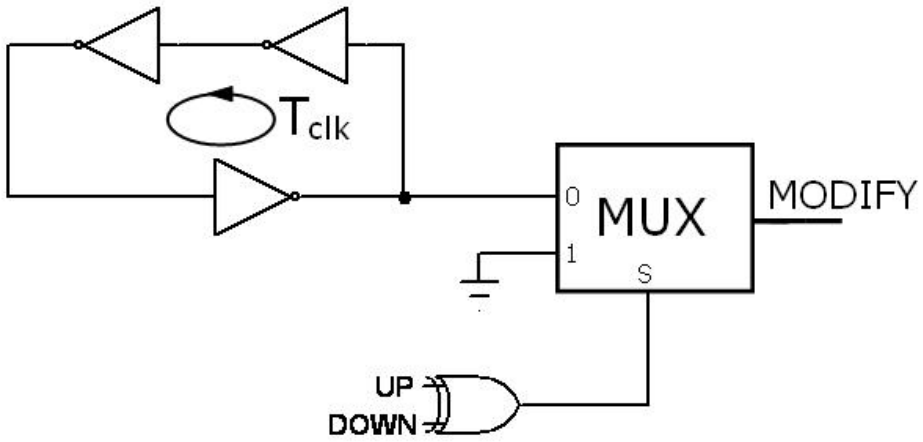


Figure 128: spt-PFD implementation with a multiplexer (spt-PFD2)

The operation principle for spt-PFD2 is similar to spt-PFD1's. The pulldown signal, in this case, is used to pass the oscillation or GND to the output via a multiplexer. This implementation doesn't create a VDD-GND path in case of lock. However, the architecture creates a random dead-zone due to the uncorrelated standing of the multiplexed clock and the select signal. The set of possible characteristic curves are shown in Figure 129. This curve is drawn based on a 600 ps clock period, assuming 50% duty cycle. In general, the dead-zone can be defined as a uniform random variable $\mathbf{t_{dz}}$, such that:

$$t_{\text{dead-zone,min}} < \mathbf{t_{dz}} < t_{\text{dead-zone,min}} + T_{\text{clk}}\,(1\text{-}\textit{duty cycle}) \qquad \textbf{(49)}$$

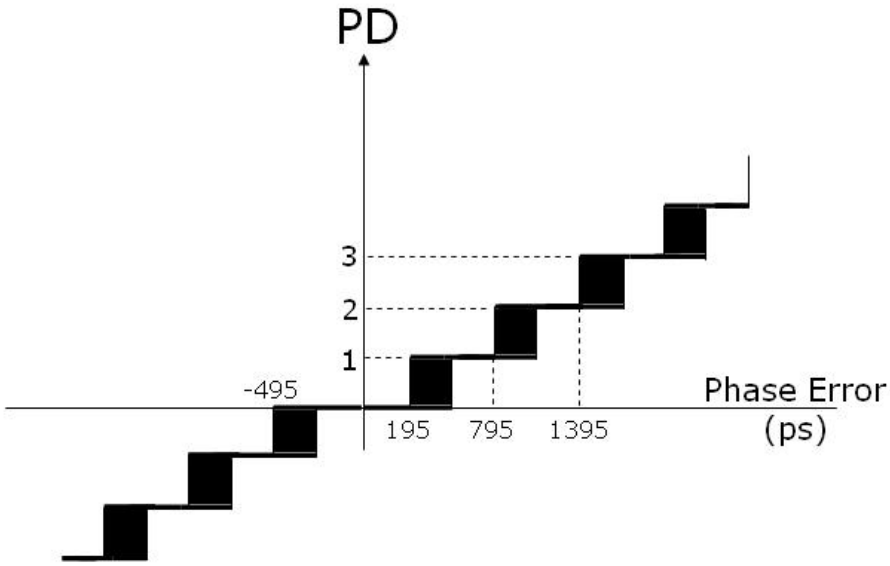


Figure 129: Random dead-zone of the spt-PFD2

spt-PFD with a gated oscillator: spt-PFD3

Single pulse-train generation can also be achieved by using a gated oscillator, illustrated in Figure 130.

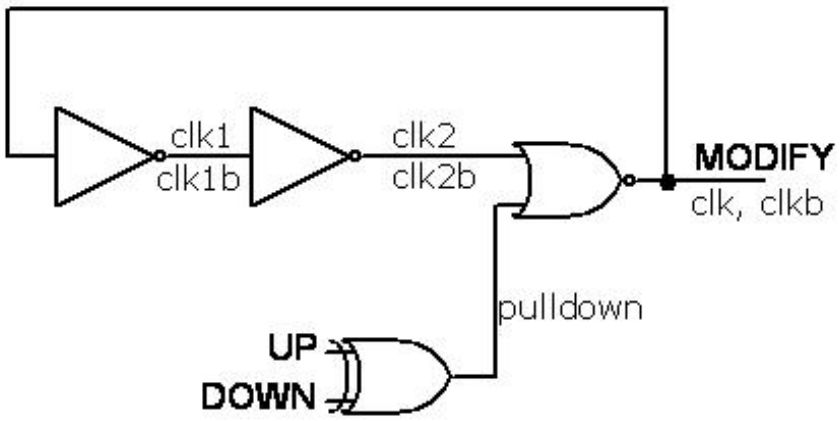


Figure 130: spt-PFD implementation with a gated oscillator (spt-PFD3)

When the two inputs are in phase, the *pulldown* signal is pulled high to drive the *modify* output low. On the other hand, when the two inputs are out of phase, the *pulldown* signal is pulled low. The 2-input NOR gate, with a "0" input, operates like an inverter to form an odd number of inverters for oscillation. The *modify* signal, in this case, is a series of pulses for the duration of the input phase difference. The inverters and the NOR gate are implemented as differential static logic circuits. The cascade voltage switch logic (CVSL) NOR gate is shown in Figure 131.

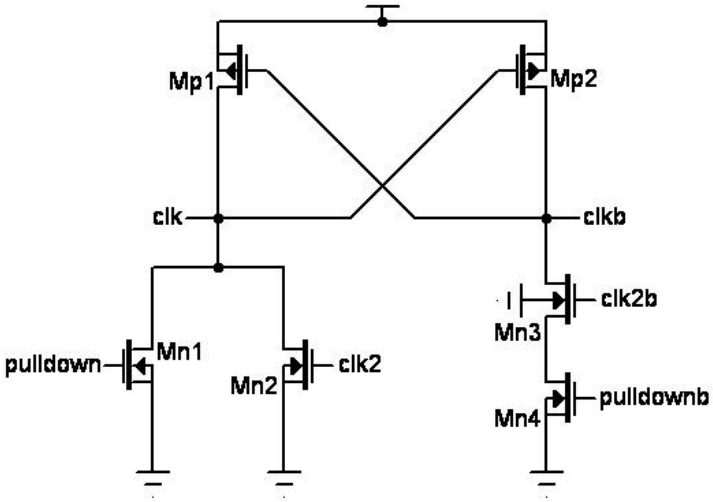


Figure 131: 2-input NOR gate schematics

When the *clk* output is used to trigger a flip-flop, 190 ps dead-zone is measured. The dead-zone is determined by how fast the *clk* output is pulled high when the *pulldown* signal turns low. Also shown in Figure 132, *clkb* signal is pulled down first, and then it pulls the *clk* signal high through Mp_1. If the *clkb* is used to clock the flip-flop, the dead-zone improves more than 50%, demonstrated in Figure 133.

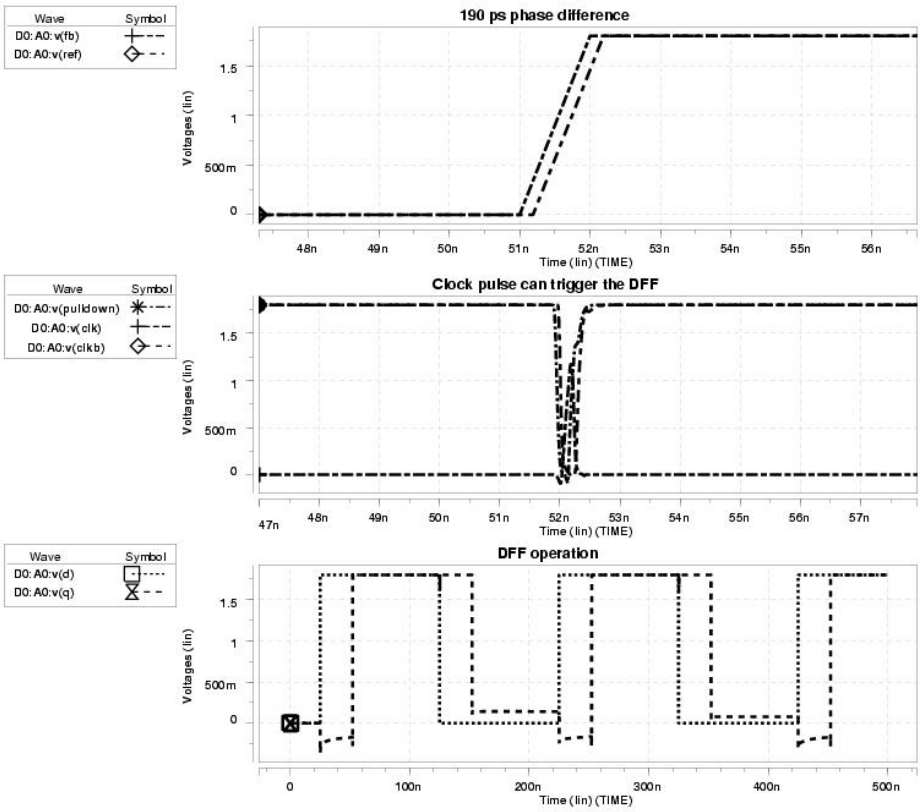


Figure 132: Dead-zone for spt-PFD3

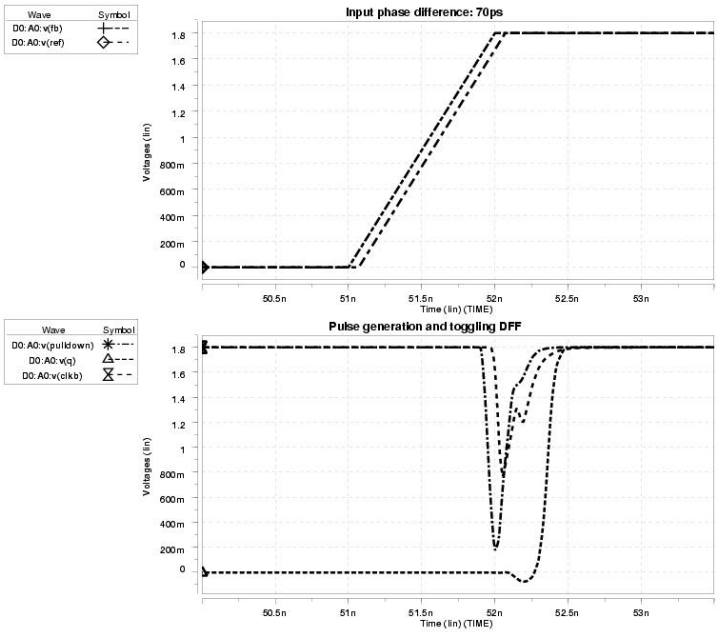


Figure 133: Improved dead-zone for spt-PFD3

The response delay of the flip-flop, the time from the *pulldown* switching to the output flipping, is measured as 536 ps in Figure 133. When pulldown goes low, clkb goes low. The positive edge of the clkb occurs after $T_{clk}/2$. The feedforward path response delay can be decreased by an amount of $T_{clk}/2$ by simply replacing the positive edge-triggered DFFs with negative edge-triggered DFFs. This issue is shown in Figure 134, where responses of positive edge versus negative edge triggered DFFs are drawn together. The measured delay improvement is 340 ps, which matches quite well with the 300 ps improvement in theory. The schematics for the high-speed differential flip-flop are shown in Figure 135, where a termination stage is used at the output for proper operation at the hold stage [78].

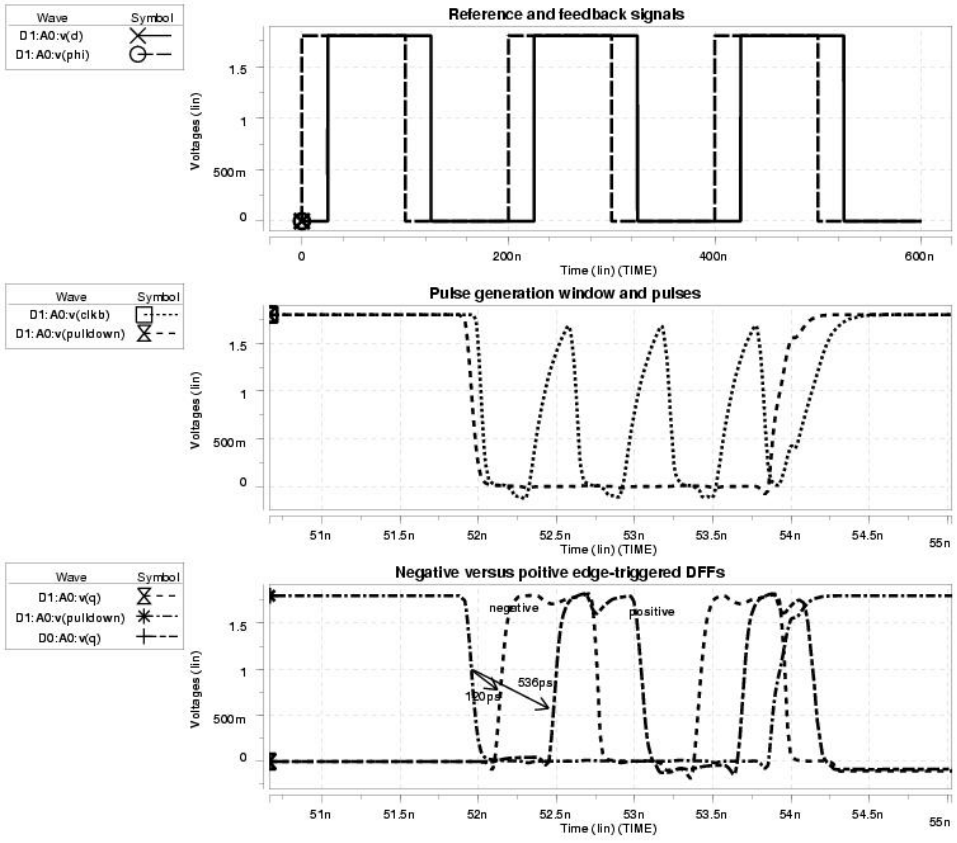


Figure 134: Forward path delay improvement by negative edge-triggered DFFs

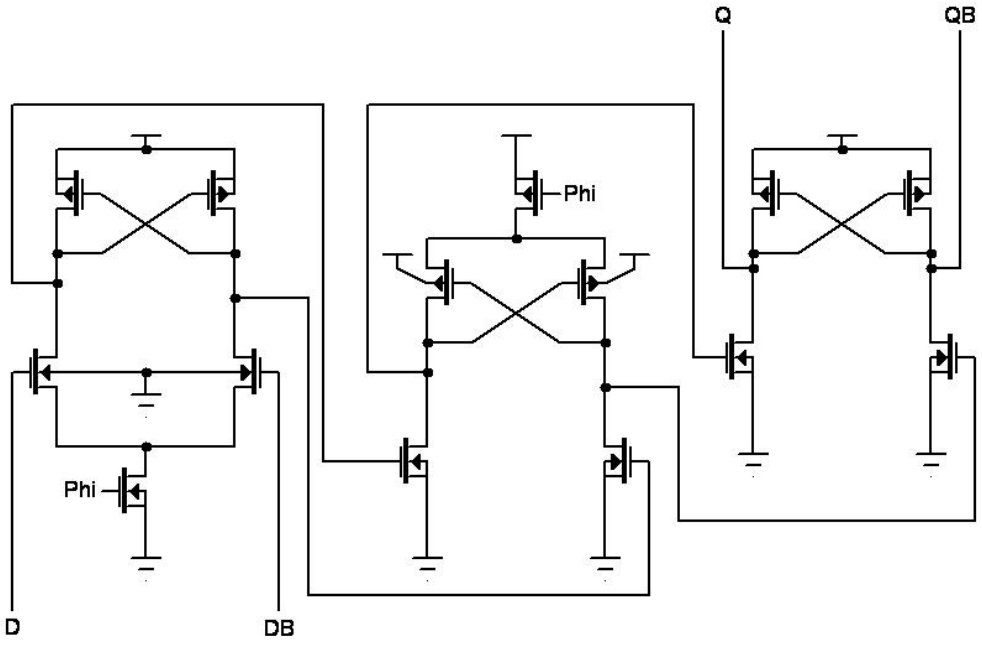


Figure 135: Negative edge-triggered DFF schematic

After all the analysis, the characteristic of the spt-PFD3 can be drawn as shown in Figure 136. The dead-zone measurements at various process corners are summarized in Table 14.

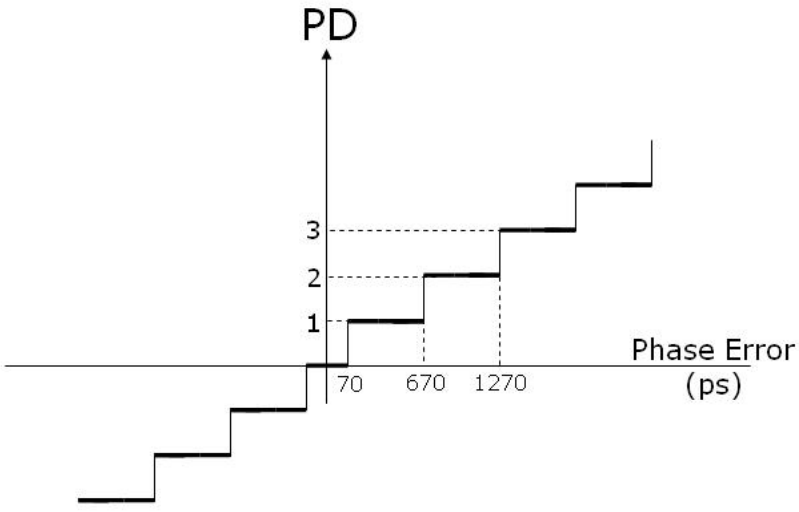


Figure 136: Dead-zone characteristic of the spt-PFD3

Table 14: Dead-zone measurements at various process corners

	TT	FF	FS	SF	SS
Dead-zone (ps)	70	60	70	90	90
Power at lock (µW)	17	23	20	18	15
Tclk (ps)	600	467	591	620	770

The power consumption data in Table 14 show that spt-PFD3 consumes 100 times less power than spt-PFD1. The low power consumption of spt-PFD3 is due to the clock gating. Hence, the dissipated power is a function of the input phase error. This fact is demonstrated by simulation results in Table 15.

Table 15: Power consumption variation with input phase error

Reference frequency	**ΔΦ**				
	0	**π/2**	**π**	**3π/2**	**2π**
10 MHz	17µW	196µW	350µW	513µW	660µW
100 MHz	180µW	420µW	515µW	699µW	770µW

7.3.2 Truncated UP/DOWN Counter

Figure 137 shows the block structure of the truncated UP/DOWN counter. The *MODIFY (MOD)* and *DIRECTION (DIR)* are the two input signals to the block, whereas the output is a binarily weighted *n*-bit word (reg(0) is the least significant bit). On each clock cycle, the counter is incremented if the *DOWN* signal is low and decremented if it is high. However, the clock is gated by the truncating circuitry to block any flipping when

- all bits are high and the counting direction is UP, or
- all bits are low and the counting direction is DOWN.

The gate level implementation of the truncating circuitry is given in Figure 138 for *n = 4*. Functional speed for this block is not critical for proper operation. Therefore, standard CMOS cells can be used to implement multiple-input gates.

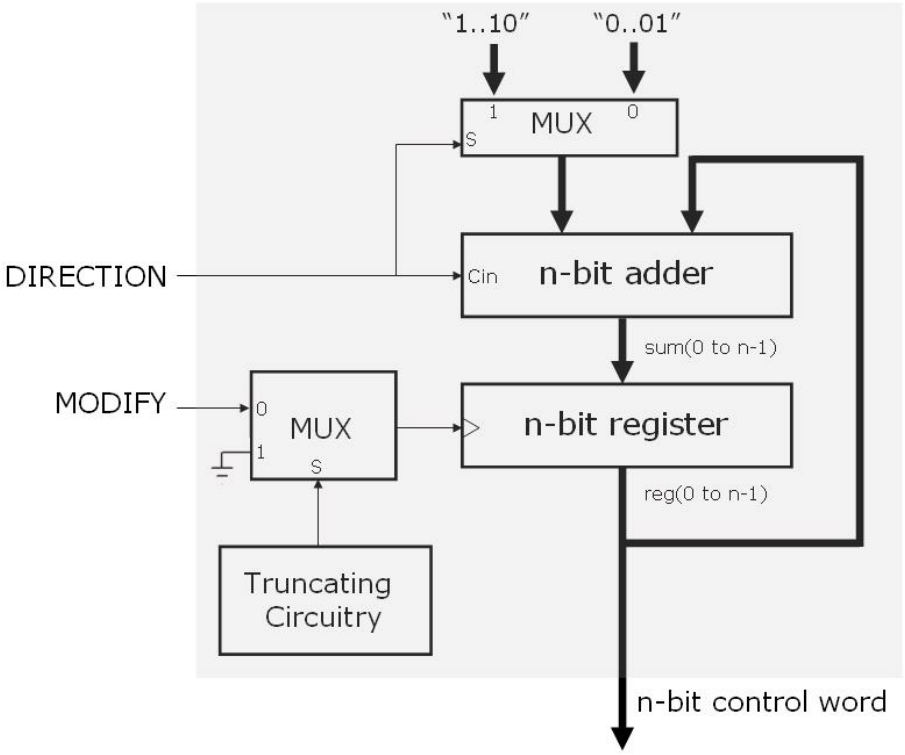


Figure 137: The truncated UP/DOWN counter block diagram

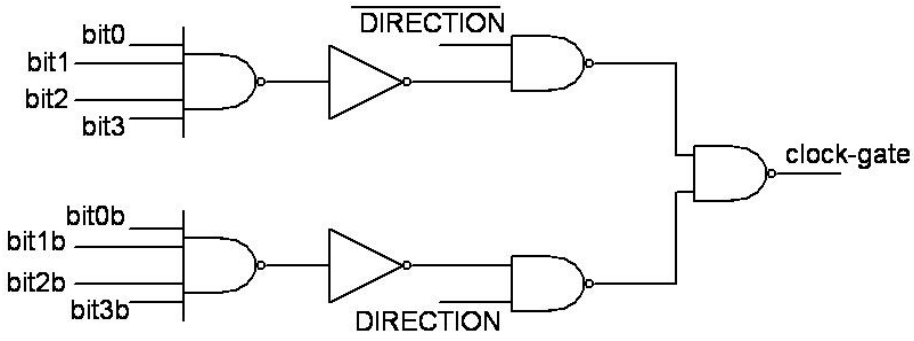


Figure 138: The truncating circuit

The frequency response of the counter block determines the oscillation frequency limits for the single pulse-train PFD. Even though the registers can respond to pulses as short as 180 ps, the minimum allowable period is determined by the data preparation time from register output to the register input. For instance, the worst case data preparation delay is the switching delay from *Reg0* to *Sum(n-1)*. Therefore, the minimum period for the clock has to be bigger than the sum of this worst case delay plus the register's setup time. The worst case adder delay occurs when the data goes from "01..10" to "01..11" at one clock edge, and the sum "10..00" gets prepared (after n-1 stages of carry propagation) at the register input, before the next clock edge arrives.

A 4-bit carry look-ahead (CLA) adder is designed next. A generic structure with AND and XOR gates is used to produce *generate/propagate* signals and the *Sum*. A Manchester-like CLA carry generator is adopted and modified as shown in Figure 139 [79]. The "*b3 b2 b1 b0*" input of the adder is "0001" for UP counting and "1110" for DOWN counting (along with *Cin=1*). The *DIRECTION* signal, hence, is fed to the input carry bit to determine the count direction. Figure 140 demonstrates the truncated counting, where register bits are denoted as "a3 a2 a1 a0".

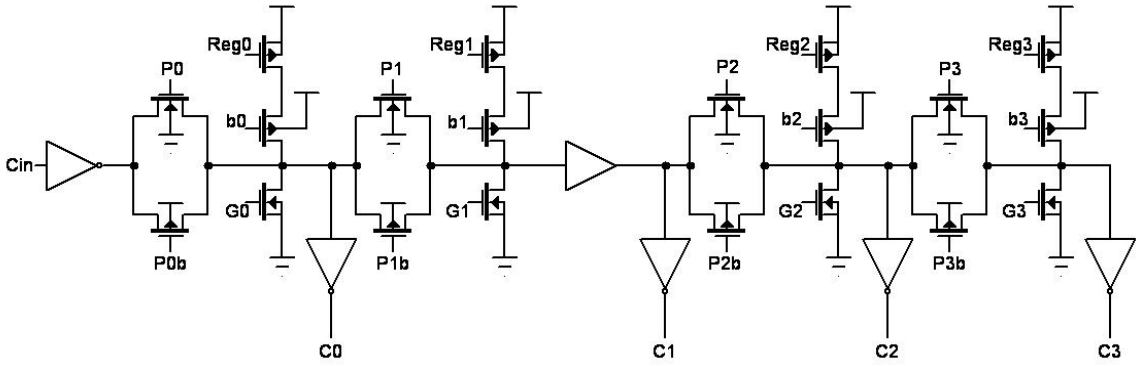


Figure 139: Manchester-like CLA circuit

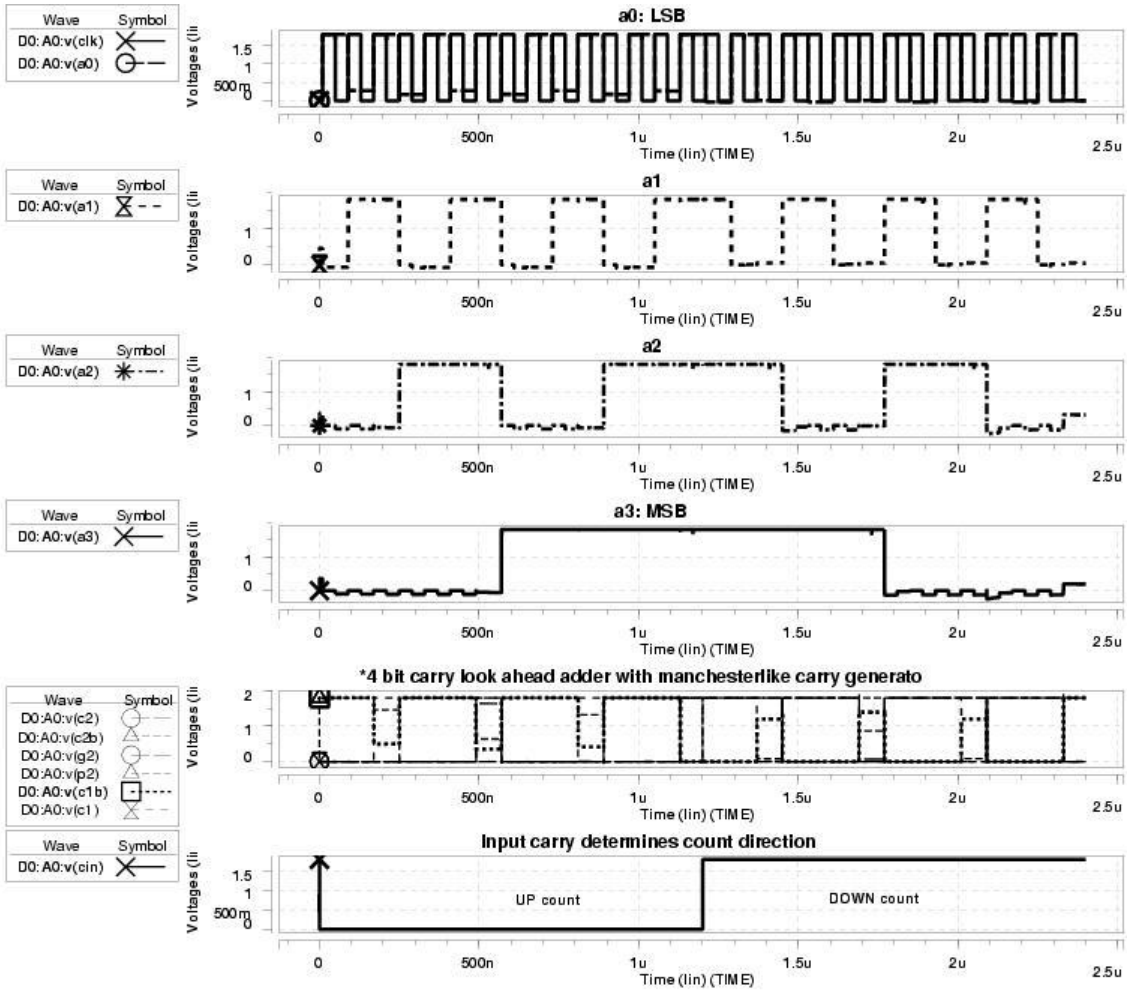


Figure 140: 4-bit truncated UP/DOWN counter operation

The design can be cascaded to build longer adders. Extra buffers are then needed in the carry generator after every two carry bit generation as in Figure 139. The truncating circuit also needs to be modified simply to NAND *n* inputs at the first stage. Increasing the number of bits, however, decreases the maximum operation frequency due to the rising carry propagation delay in the worst case. The minimum clock period for 4, 5, and 8 bit UP/DOWN counters are given in Table 16. The worst case is demonstrated

in Figure 141 for *n=8*. When cascading counter blocks, carry select adders can be employed to maintain a low delay variation as the counter gets longer.

Table 16: Minimum clock period for proper counter operation

Counter Length (bits)	Minimum T_{CLK} (ps)
4	570
5	700
8	1200

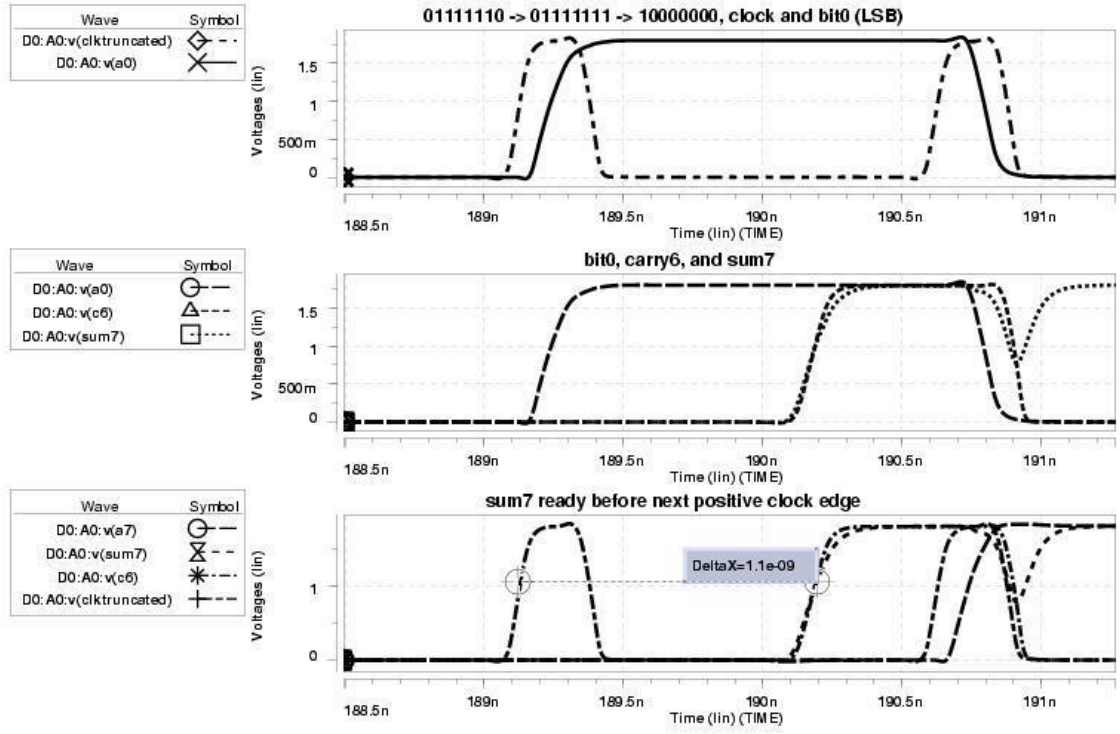


Figure 141: Worst case propagation delay for 8 bit UP/DOWN counter

7.3.3 DAC and CCO

The digital to analog converter designed for the prototype psc-PLL in Section 7.2 can be easily modified for binary weighting. Stacked implementation techniques make the design simpler while assuring monotonicity. The design criteria for the DAC were already discussed in the same section. Figure 142 shows the 4-bit DAC schematic.

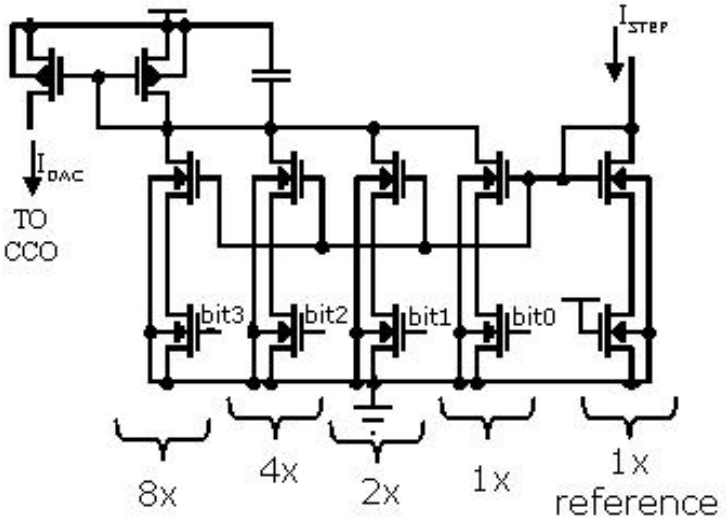


Figure 142: Digital to analog converter schematic

The CCO control current, I_{CCO}, in Equation 46 can now be rewritten as

$$I_{CCO} = I_{BIAS} + (bit_0 + 2\,bit_1 + 2^2\,bit_2 + 2^3\,bit_3)\,I_{STEP} \quad \textbf{(50)}$$

for a 4-bit binarily weighted DAC.

In order to demonstrate the DAC performance, it is utilized to drive a CCO whose characteristic is shown in Figure 143. The CCO is a 9-stage implementation employing the delay cell with a diode connected pMOS load as in Section 7.2.

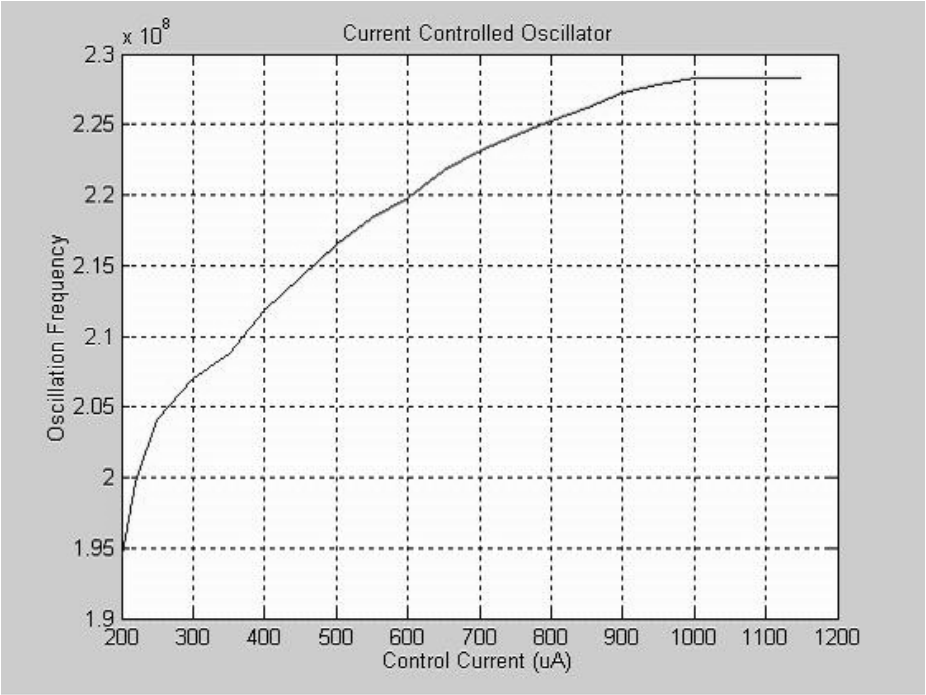


Figure 143: 9-stage CCO characteristic

If the fairly linear input range of 400 μA-900 μA of the CCO is picked to be controlled by the DAC, 5 bits would be enough to achieve around 10 ps resolution in average. The CCO bias current is set to be 400 μA. To span the given current range with 5 bits, the DAC supplies current from 0 μA to 496 μA in 16 μA steps. The HSpice simulation of the DAC driven CCO is given in Figure 144. The resolution of a bit varies between 6 ps and 16 ps within the control range due to the imperfections in linearity as demonstrated by a linear line in the same figure. However, as discussed in the prototype design, the nonlinearity in the characteristic does not affect proper operation as long as monotonic behavior is preserved.

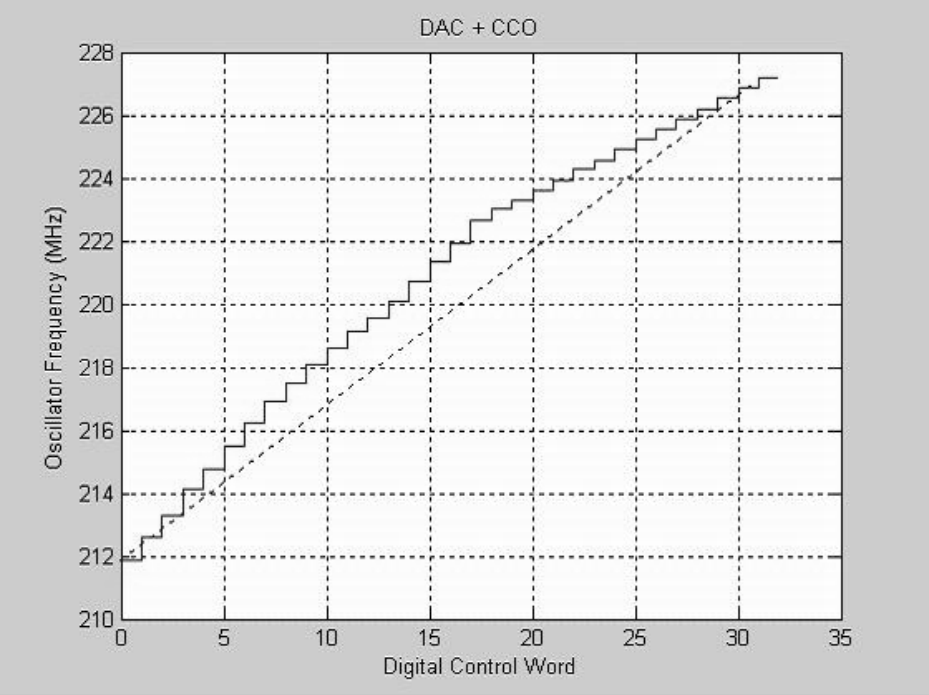


Figure 144: DAC driven CCO

7.3.4 Pulse-Stream Coded PLL Design Guidelines

The properties of each pulse-stream coded PLL block are analyzed so far. This section investigates the applications in which this design can be proven useful.

When designing PLLs, the allowable jitter range is the major design constraint. The jitter in psc-PLLs is mainly determined by the resolution of the generated feedback signal. For instance, in the above VCO driven by the 5 bit DAC, the oscillator resolution changes from 6 ps to 16 ps. In the best case, the control word at the DAC input fluctuates one least significant bit (LSB). Hence, the output jitter will vary between 48 ps to 128 ps for a feedback division ratio of N=8. The control word fluctuation may however be a few LSBs if the phase detector does not have a good resolution. This estimation does not

include either the jitter due to the power supply noise or the reference noise. The jitter of the feedback clock (deterministic part) is the dominant part of the overall jitter.

Operating frequency, together with the allowable jitter range, usually determine the kind of PLL to be utilized within an application. For low frequency operations, with high allowable clock jitter, all-digital PLLs can be synthesized from a generic code using standard cell components. However, digitally controlled oscillators fail to realize most design constraints in recent communication systems. It is, hence, imperative to design analog VCO/CCOs for high frequency applications. Next, an analog or a digital forward loop can be designed to control the oscillation. Several issues in the implementation of an analog loop were discussed in Chapters IV, V, and VI. On the other hand, a novel technique to digitally control the analog oscillator is described earlier in this chapter. If the jitter specification is not extremely tight, the pulse-stream PLLs can offer fast application-specific solutions.

Initial effort during the PLL design is required to roughly decide the division ratio and the VCO range. The VCO characterization is straightforward when Spice or Spectre tools are used. Once the VCO is characterized, the number of bits required for the target jitter can be determined using Equation 51. Considering that an offset is also needed, since this jitter estimation includes only the deterministic jitter, if the specifications are not realizable, an analog loop can be established for attaining low jitter. At this point in the design, a short analysis on applicability of the digital control can be carried out based on the VCO characteristic, whereas the jitter analysis for the analog loop requires complicated simulation tools and methods. This discussion is illustrated in Figure 145 to

show that extra time to investigate a possible psc-PLL implementation could save T_2-T_1 amount of time.

$$n = \left\lceil \log_2 \left(\left(\frac{1}{f_{\min}} - \frac{1}{f_{\max}} \right) \frac{N}{Jitter_{peak-to-peal}} \right) \right\rceil \quad \textbf{(51)}$$

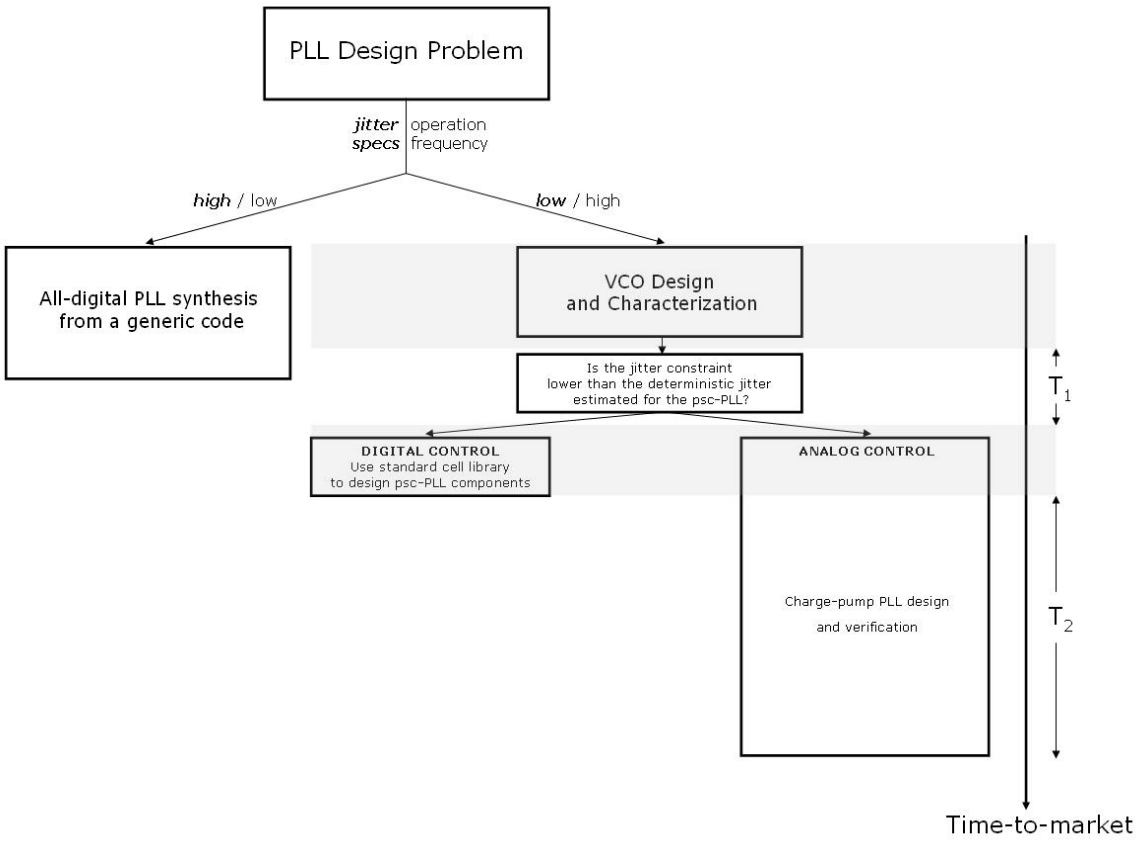


Figure 145: PLL design procedure for a short time-to-market

As will shortly emerge, fundamental reasons dictate that the parameters of the pulse-stream coded PLL need to be analyzed for stability. The transfer function of the PFD and the DAC with the CCO are given in Equations 52 and 53, respectively.

$$H_{sptPFD}(z) = \frac{m}{T} z^{-1} \quad \textbf{(52)}$$

$$H_{DAC,CCO}(z) = \frac{\Delta T}{1 - z^{-1}} \quad \textbf{(53)}$$

where m is the number of short pulses that would fit within a reference period T. ΔT stands for the oscillator resolution. In analogy with the single capacitor as an integrator in CPPLLs, employing a simple digital integrator (Equation 54) filter in the loop results in a root-locus plot as in Figure 146. The open loop transfer function and the loop gain that is swept for the root-locus plot are given in Equations 55 and 56.

$$F(z) = \frac{1}{1 - z^{-1}} \quad \textbf{(54)}$$

$$H_{open-loop}(z) = Kz^{-1}F(z)\frac{1}{1 - z^{-1}} \quad \textbf{(55)}$$

$$K = mN\frac{\Delta T}{T} \quad \textbf{(56)}$$

Figure 145 indicates that the second-order PLL is unstable since the poles will never be inside the unit circle. Just as in the CPPLL theory, a zero at z=0.5 can be inserted to the integrating digital recursive filter:

$$F(z) = \frac{1 - 0.5z^{-1}}{1 - z^{-1}} \quad \textbf{(57)}$$

The new root-locus plot is given in Figure 147, suggesting K < 2.8 for stability. Hence the relation of the loop parameters is derived, Equation 58, for stability. This equation states that the number of short pulses within a period is not only limited by the operation time of the digital blocks but also by the stability constraint.

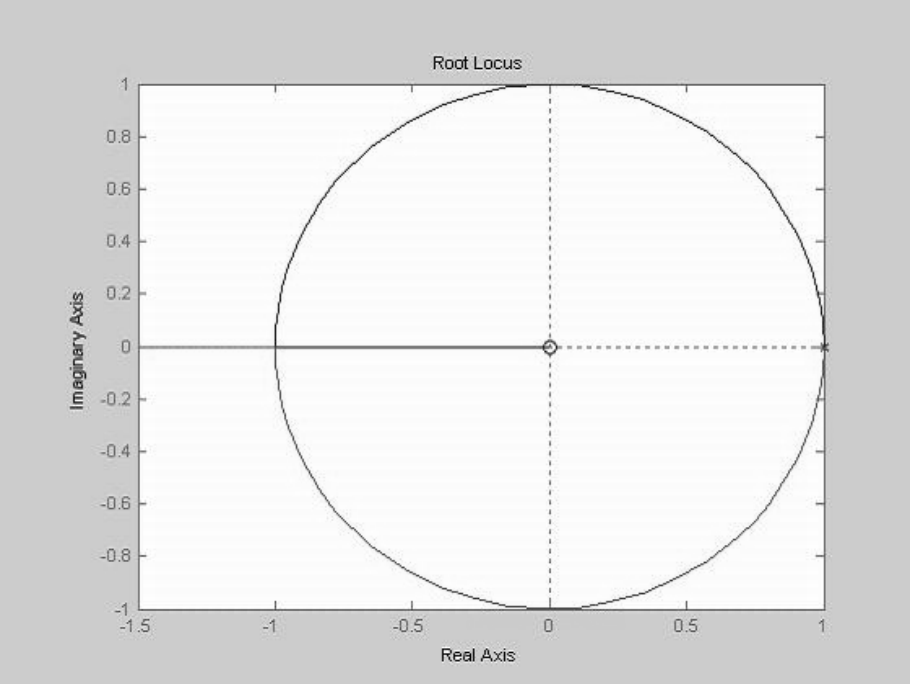


Figure 146: Root-locus plot for $F(z) = 1/ (1 - z^{-1})$

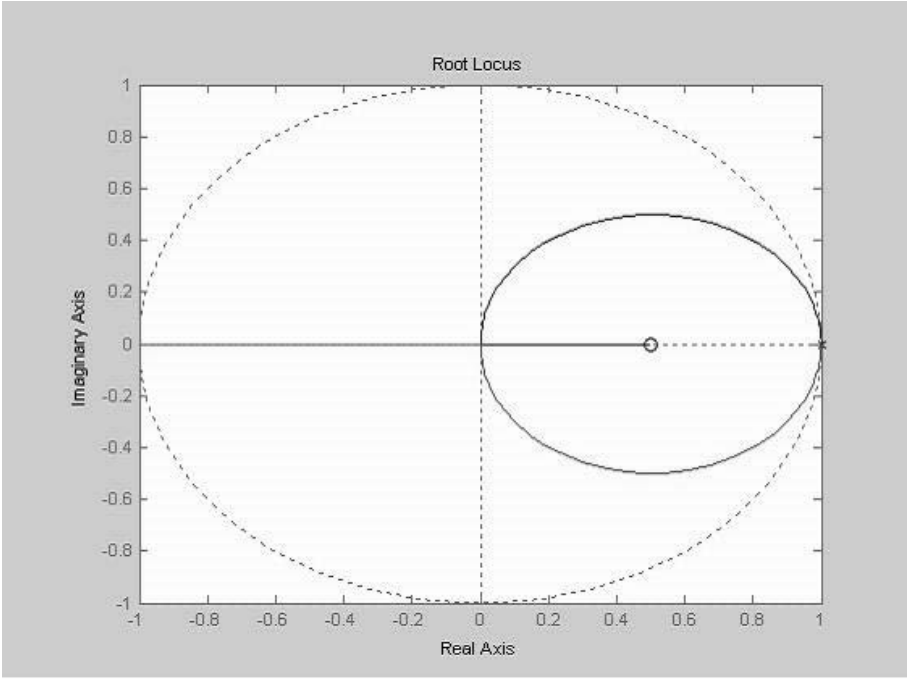


Figure 147: Root-locus plot for $F(z) = (1 - 0.5 z^{-1})/ (1 - z^{-1})$

$$mN\frac{\Delta T}{T} \; < \; 2.8 \qquad \textbf{(58)}$$

Figure 148 shows the ripple in the digital control word during the lock. One LSB, the peak fluctuation in this case, will cause an output jitter equal to the resolution of the DAC driven CCO.

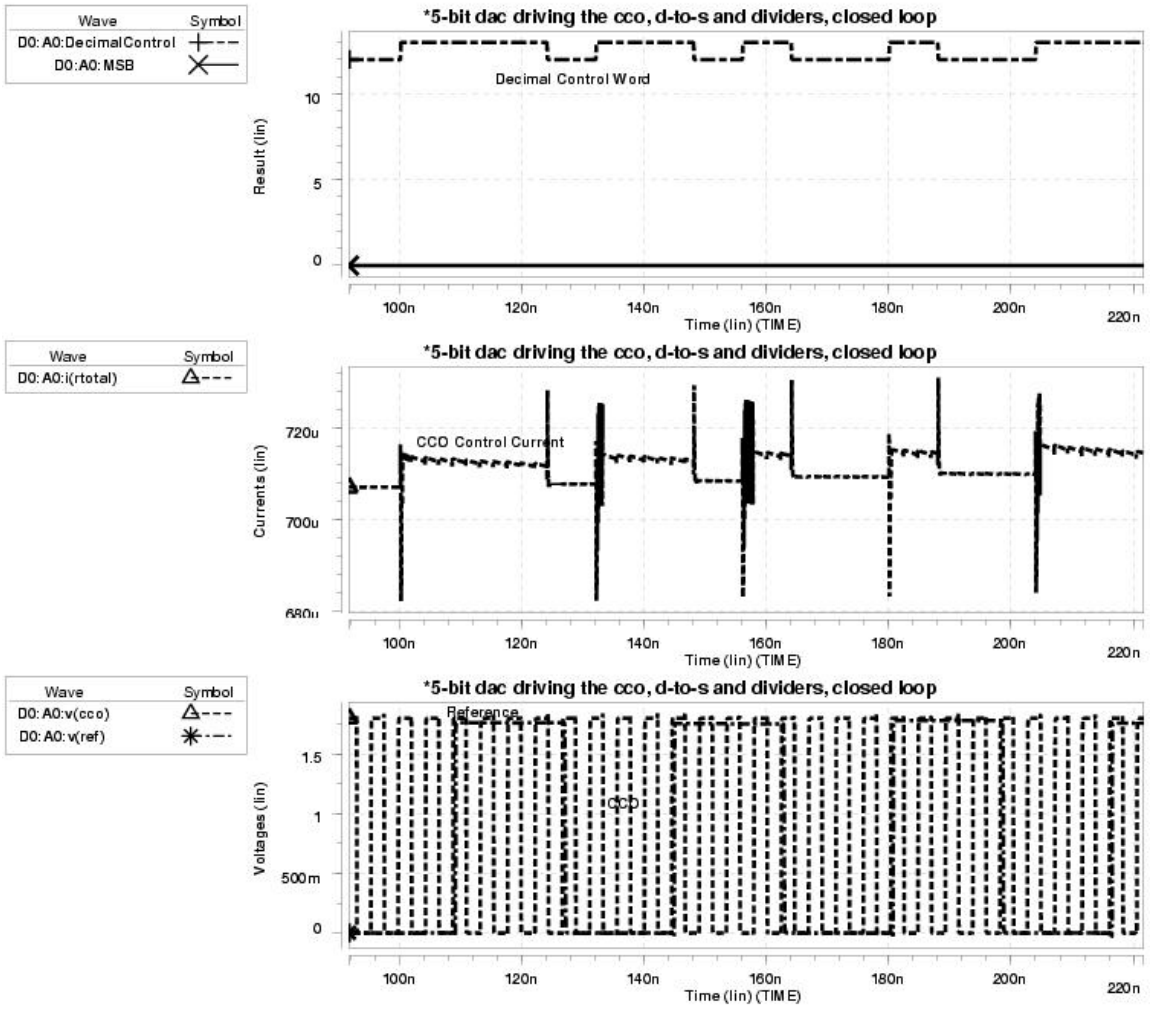


Figure 148: One LSB ripple at lock

CHAPTER VIII

CONCLUSIONS AND FUTURE RESEARCH

In the closing chapter of this thesis, the major contributions of the work are summarized along with the inquiry of some prospective directions in which this research can proceed.

8.1 Conclusions

This work has presented a study of oscillation control for high-performance CMOS phase-locked loops. The research first focused on the limits and design issues of the control path in high-performance charge-pump PLLs, based on the comparative study of various architectures. The attention, then, was turned to a novel class of otherwise analog PLLs that use a digital control path (less sensitive to variations in a submicron process) for driving an analog oscillator. The contributions of this research can be summarized as follows:

- The basics of PLL operation were shown in a unique control centric flow. Existing PLL types are classified within this framework. The comparative study of various PLL architectures led to the detailed analysis of the low-jitter charge-pump PLLs with a focus on control blocks.
- This research has shown the possibility of expanding the applications of CPPLLs with ring VCOs into low-noise multi-GHz communications that previously required CPPLLs with LC VCOs. Effective control blocks to implement a single

ended low-jitter CMOS charge-pump PLLs were extensively explained. These blocks were used to build a PLL operating at 1.8 GHz with a 1.7 ps RMS cycle-to-cycle jitter measured with a clean power supply.

- Next, the maximum lock-in frequency was investigated using the same single-ended control scheme and a 3-stage ring oscillator for maximum speed in TSMC's 0.18 μm CMOS process. The 3-stage ring oscillator incorporated saturated-type delay cells within a multiple-pass loop to achieve the highest frequency in a given technology. The single-ended PLL locked with a 2.6 ps RMS cycle-to-cycle jitter at 5.8 GHz.
- The poor performance of single-ended CPPLLs with a noisy power supply was experimentally demonstrated. An exceptionally performing differential CPPLL was implemented and verified at 2.5 GHz with -124 dBc/Hz phase noise at 1 MHz offset, which is a noteworthy result in the literature. The differential CPPLL utilized a unique charge pump and a unique common-mode feedback scheme that allowed low-jitter operation at high frequencies. The LC oscillator built in the standard CMOS technology incorporated digital coarse-tuning by switched MiM capacitive loads as well as differential fine-tuning by accumulation-mode varactors.
- Physical design considerations were summarized for low-jitter PLLs from FET level to the pin level.
- The significance of the control line noise was shown by a periodic cycle-to-cycle jitter characteristic, confirming the frequency modulation of the VCO by a

periodic signal. The importance of differential control was emphasized by measurement results.

- Poor performance of submicron CMOS CPPLLs at low frequencies was addressed and theoretically modeled. Increasing jitter with decreasing frequency was explained by leakage from the control node(s), the significance of which has been amplified by technology trends. Arguments were also given in this research to decrease the leakage influenced jitter by an innovative method of inserting multiple reset pulses in lock. The expected improvement was mathematically derived in terms of phase error and verified by Spice simulations. These issues are demonstrated in Figure 149.

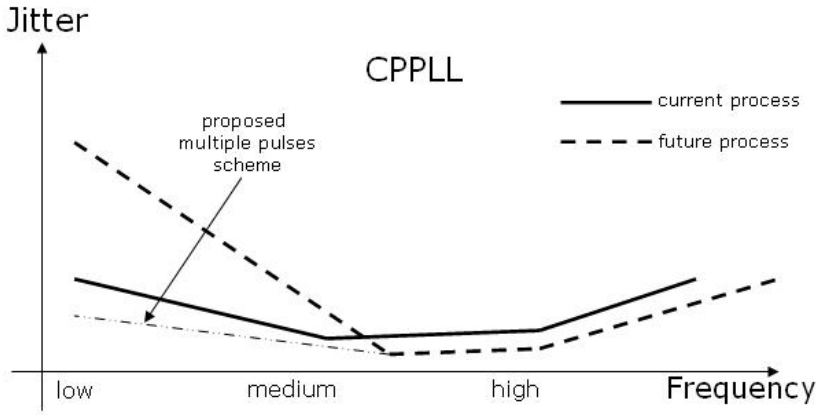


Figure 149: Poor performance of CPPLLs at low frequencies

- Several problems with performance enhancement and precise oscillator control using analog circuits in low-voltage submicron CMOS processes, coupled with the fact that analog (or semi-digital) oscillators having various advantages over their digitally controlled counterparts, prompted the proposal of the digitally-controlled phase-locked loop. A novel method for digitization was proposed in

which trains of pulses code the phase/frequency comparison information rather than the duration of the pulses. The result is the pulse-stream coded phase-locked loop (psc-PLL). A simplified prototype was implemented and tested to prove frequency tracking with failure in locking. After investigating the control resolution problem with the prototype, a next generation psc-PLL was developed. Each building block of the psc-PLL was designed and characterized in detail. The loop stability condition was derived for proper operation considering the delay introduced by each block.

- The dominant deterministic noise in psc-PLLs was quantified. Then, general design guidelines were extracted for constructing semi-custom PLLs and how to deciding whether the proposed architecture could show advantages over its analog counterpart for given specifications. The PLL type versus jitter is qualitatively shown in Figure 150. Quantitative analysis was established throughout Chapter VII; however, Figure 150 illustrates how the significance of psc-PLLs increases with the technology trends (improving digital circuit performance while analog design becomes more challenging).

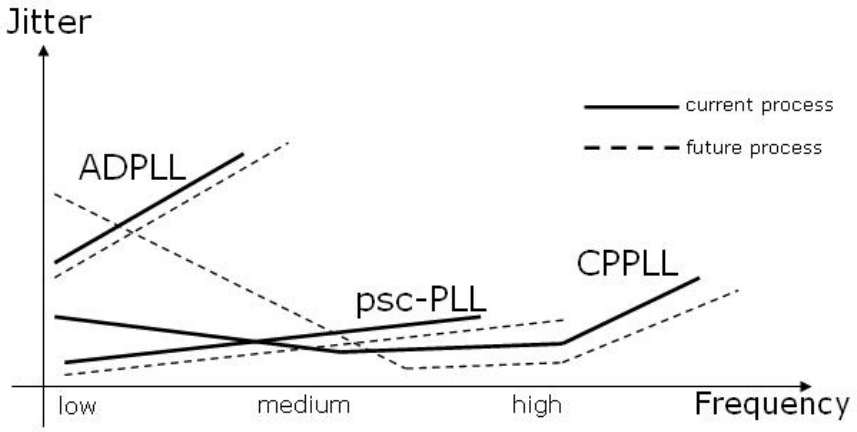


Figure 150: Jitter performance of various PLL types

8.2 Future Research

Several possible future research directions based on this work are summarized below:

- Charge-pump PLLs with single-ended control path have been successfully implemented to operate at high frequencies with low output jitter. The low jitter measurements, made with clean power-supplies, showed the possibility of expanding single-ended designs into low-noise multi-GHz applications. It was also shown in Chapter IV that the output jitter was still increased significantly when the chip was fed from a noisy power supply. A possible solution is to drive the analog PLL components from a regulated power source. In that case, to prevent improper start-up of the oscillator, the comparator output of a conventional regulator can be used to generate a digital reset pulse, which could reset the oscillator until the regulator output settles.
- An exceptionally performing differential CPPLL, which utilizes a unique charge-pump and a common-mode feedback scheme, is implemented and verified for low-jitter operation at 2.5 GHz. The LC oscillator used in that loop had a lower quality factor than expected, because the center of the hollow inductor was filled with 6 layers of metal and 2 layers of poly by MOSIS for meeting chemical-mechanical-polishing specifications. The control scheme, hence, can be shown to perform even better with a higher-Q oscillator. For this purpose, a new differentially controlled oscillator can be designed, or an extra layer of mask can be used to stop the dummy filling of the hollow region.

- A byproduct of the control line noise analysis was the introduction of the "multiple reset pulses" solution, presented in Chapter VI. The theory was studied along with some circuit level simulations. Further work involves fabrication of various test structures starting with simulated architectures. Further development of the system can include adaptively increasing the number of reset pulses with decreasing frequency through digital control.
- It is illustrated in Chapter VII that digitally controlling analog oscillators can serve as a significant timing solution in submicron CMOS processes. A novel system, the pulse-stream coded PLL, was described and simulated. Realization of various test structures in upcoming submicron processes can verify the significance of the design and can facilitate better modeling of the system. Some of the design considerations that need particular attention are the implementation of pulse-stream generation and the number of pulses within an input period. When tested at high temperature (increased leakage), the frequency range for which psc-PLLs over-perform CPPLLs can be quantified (quantification of intersection points in Figure 150).
- It is crucial to note that the psc-PLL operates similar to the CPPLL with a digitized storage and evaluation block. For instance, increasing the resolution corresponds to smaller charge pump current in the well-studied CPPLL which decreases the loop bandwidth to improve the noise characteristic while degrading the acquisition performance. This issue has been tackled by using adaptive loops [36, 70, 80, and 81] or dual loops [16, 69, 75, 82-84] for CPPLLs in the literature. These solutions can be modified to be used in the proposed architecture. Even for

the frequencies at which the psc-PLL cannot sustain low jitter, employing it in a dual-loop phase-locking scheme should be considered. The psc-PLL can prove useful as the coarse-tuning in such architectures because it is simpler to design and verify, it enables digital control in the feedforward path (for more complicated algorithms), it does not require big passive components for the filter, and it minimizes PVT variations.

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