Optical Gigabit Ethernet Design Project

Midterm Report

ECE 135 – Project GabE

March 25, 2005

Omar Al-Jadda
Patrick Crosby
Adam Durity
Rahmin Sarabi
# Table of Contents

Table of Contents ............................................................................................................. ii
Abstract ............................................................................................................................. 1
1. Introduction .............................................................................................................. 2
   1.1. Background ....................................................................................................... 2
   1.2. Gigabit Ethernet Design .................................................................................. 2
   1.3. Board Components ......................................................................................... 3
   1.4. Project Overview .............................................................................................. 5
2. Project Information ................................................................................................... 6
   2.1. Group Management Plan .................................................................................. 6
   2.2. Time Management ............................................................................................ 6
   2.3. Optical Link Budget ........................................................................................ 7
   2.4. Part Selection ................................................................................................... 9
   2.5. Financial Budget .............................................................................................. 12
   2.6. Bill of Materials ............................................................................................... 12
3. Test Board .............................................................................................................. 14
   3.1. Test Setup ....................................................................................................... 14
4. Design and Layout ................................................................................................. 15
   4.1. Schematic Design ........................................................................................... 16
   4.2. Board Design .................................................................................................. 19
5. First Non-Aggressive Board Run ........................................................................... 21
6. Conclusion – The Future of Project GaBE ............................................................. 27
References ....................................................................................................................... 28
Abstract

The need in industry for simply a fast connection between computers has all but vanished. In its place is a new demand for a low-cost, reliable high speed link that serves as the backbone for large network infrastructures. Until now, optical Ethernet could not provide this reliability and speed for low costs that compared to their electrical counterparts. Now, however, Project GaBE is developing an opto-electric Gigabit Ethernet solution that excels in speed and reliability and competes with its high end electrical counterparts for price. Using the latest Optical Link Budgeting techniques and selecting from only the best VCSEL and ROSA manufacturers and parts vendors, Project GaBE confidently designed and constructed their new opto-electrical link.
1. **Introduction**

1.1. **Background**

Ethernet, the most dominate networking protocol today, was one of the pioneering projects to come out of Xerox Corporation’s Palo Alto Research Center (PARC) [1]. It is widely believed that Robert Metcalfe wrote a memo to his bosses at PARC about Ethernet’s potential that in turn lead to its development in the 1970s. Metcalfe left Xerox in 1979 to promote the use of personal computers and local area networks (LANs), forming 3Com. He then successfully convinced DEC, Intel, and Xerox to work together to promote Ethernet as a standard which was first published on September 30, 1980. Competing with them at the time were two largely proprietary systems, token ring and ARCNET, but both would soon be squashed under an explosion of Ethernet products.

Since its inception, Ethernet has undergone over a thousand-fold increase in speed. Gigabit Ethernet (GbE) is an Ethernet technology that operates at a transmission speed of one gigabit per second, a ten-fold increase from the prior generation 100 Mbps Ethernet. The rapid increase in computing power, computing resources, and the need to interconnect these computing environments led to a demand for faster networks. Used mostly for backbones as a connection between switches, routers, and servers, Gigabit Ethernet is a solution to this demand that continues to grow.

1.2. **Gigabit Ethernet Design**

The increase in speed from 100 Mbps to 1 Gbps was accomplished by merging two technologies together - IEEE 802.3 Ethernet and ANSI X3T11 FiberChannel. For purposes of compatibility the Gigabit Ethernet architecture essentially looks identical to that of Ethernet from the data link layer upwards. The first standard for Gigabit Ethernet, IEEE 802.3z, was defined in June 1998 for use over multimode optical fiber [1]. The design of our optoelectronic link will follow the IEEE 802.3z standard. The basic architecture of this standard can be seen in Figure 1-1 below.
In order to build an optoelectronic link that could potentially be sold on the market, the device must be in compliance with the 802.3z standards. As a result, the laser may transmit at either 850 nm or 1300 nm wavelengths for 100baseSX class. In addition, two types of fibers are supported in the standard: single-mode optical fiber (SMF) with 10µm core diameter or multimode optical fiber (MMF) with 50µm core diameter or 62.5µm core diameter [2]. Further, we will need to meet the eye safety specifications. In addition, our optoelectronic link will contain a single power supply in order to minimize the size of the final device. Our group will further attempt to meet spacing requirements for use of SC connectors.

1.3. Board Components

The optoelectronic board is the Physical Media Dependent (PMD) layer of the 802.3z architecture. The main active components of the board are the Vertical Cavity Surface Emitting Laser (VCSEL), used to transmit data with light, and the Photodiode (PD), used to receive the light data. Our VCSEL is driven by a Maxim MAX3287 laser driver that takes a differential input and converts the signal into a current. The current from the MAX3287 allows the VCSEL to produce high and low pulses of 850nm light. The light from the transmitter board is transmitted to a receiver via an optical fiber connection, and another optical cable connects a transmitter to the receiver. Typically, a photodiode on the receiver board detects the incoming light and generates small current signals in response. In our design, the photodiode is coupled to a Trans-
impedance Amplifier (TIA) in a combined device known as a Receiver Optical Sub-assembly (ROSA). The ROSA converts the incoming light to a current with its photodiode, and then to a differential voltage with the trans-impedance amplifier. The Limiting Amplifier, a MAX 3264, creates a digital signal from the incoming analog voltage signal from the ROSA then uses this as the output from the PMD layer.

1.3.1. VCSEL Background Considerations

The VCSEL has led to dramatic increases in the efficiency of fiber optic communications. It is composed of layers of mirrors that are a result of semiconductors sandwiched with varying composition. The mirrors are arranged in a way to reflect light back into a central cavity. Since the mirrors only reflect a narrow range of wavelengths, the combined mirrors ensure that only a small range of wavelengths of light is emitted from the VCSEL. The VCSEL has certain advantages over edge-emitting lasers: it is cheap to produce, easier to test, and more efficient [3]. Light leaves the VCSEL as a cone that is more circular than that of edge-emitters also.

VCSELs come in connectorized and unconnectorized form. Connectorized VCSELs are embedded in a casing that protects the laser and ensures proper alignment with an optical fiber. For this project VCSELs will be assessed by their divergence angle, threshold current, and slope efficiency. Slope Efficiency reveals the ratio of outgoing light power to incoming current (mW/mA). The threshold current is the minimum current necessary to make the laser lase. In general, VCSELs with high slope efficiencies and low threshold currents are most effective in an optoelectronic link application. If a VCSEL has these properties, then it will consume less power, as it will require less power to turn on and it will be more efficient in producing higher light outputs.

1.3.2. ROSA Background Considerations

As mentioned earlier, the photodiode component of the ROSA receives the incoming light generated from the VCSEL after transmission, and converts it to a current that is then converted to a differential voltage in the transimpedance amplifier. Since considerable light energy can be lost through the transmission fiber, it is essential for the ROSA to be able to yield a usable differential voltage after all of these conversions.
The measurement of how well the ROSA converts optical energy (watts) to electrical potential (volts) is the digital transimpedance. The higher the digital transimpedance value, the lower the amount of light energy that is required to convey a usable signal.

1.4. Project Overview

The purpose of this project is to design, fabricate and test an optoelectronic link that complies with the Optical Gigabit Ethernet standard IEEE 802.3z. Over the course of five months, a team of four students, named Project GaBE, will generate and follow a project management plan, subdividing tasks according to expertise and resource management. Gantt charts will be used for time management purposes and weekly presentations will keep the group up to date and on schedule. The design and fabrication must be completed on a $350 budget provided by the Duke Electrical and Computer Engineering department (ECE) in conjunction with the ECE 135 design course. The team will formulate a Bill of Materials (BOM) that lists the price per unit if 100,000 units were to be produced. These methods emulate the processes used to manage design projects in industry.

In order to familiarize the Project GaBE team with the techniques of design, fabrication, and testing, a test transceiver board that did not utilize optical technology was constructed. Using this as a basis, the group was able to gain the knowledge necessary to integrate optics into the system. The optoelectronic link was then initially designed and laid out using PCB Express software. After a series of design reviews, the board was ordered through PCB Express. After soldering the components to the board and testing, a second design is scheduled with the goal of eliminating design errors found in the initial design.

Project GaBE will use a high frequency oscilloscope for visual inspection of the eye diagram, with and without attenuation. The oscilloscope will also be used in conjunction with a probe to troubleshoot the transceiver. A Tektronix GTS1250 pattern generator and Tektronix gigaBERT 1400 will be used to check the Bit Error Rate with the PRBS7 data pattern. The group should have a working optoelectronic transceiver that complies with 802.3z standards by April 26, 2005.
2. Project Information

2.1. Group Management Plan

In order to better organize our group, we divided the work that was to be done during the course of the semester into six categories: Research on the 802.3 standard, Testing, Soldering, Board Design and Layout, Group Management and Organization, and Parts Selection and Ordering. Each of these categories was assigned a lead person who was to be in charge of all tasks relevant to that category. In addition, we assigned a secondary person to each category (except soldering) so that if the lead person could not complete the task for whatever reason (illness, incapacity, etc.) then there was already a backup in place. Furthermore, this secondary person was to work alongside the lead, assisting him as much as possible. Table 2-1 lists the division of labor between the members of the group into the six categories.

<table>
<thead>
<tr>
<th>Category</th>
<th>Lead</th>
<th>Secondary</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standards Research</td>
<td>Rahmin</td>
<td>Patrick</td>
</tr>
<tr>
<td>Testing</td>
<td>Patrick</td>
<td>Adam</td>
</tr>
<tr>
<td>Soldering</td>
<td>Omar</td>
<td></td>
</tr>
<tr>
<td>Board Layout and Design</td>
<td>Adam</td>
<td>Patrick</td>
</tr>
<tr>
<td>Management and Organization</td>
<td>Adam</td>
<td>Rahmin</td>
</tr>
<tr>
<td>Parts Selection and Ordering</td>
<td>Omar</td>
<td>Adam, Rahmin,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Patrick</td>
</tr>
</tbody>
</table>

Table 2-1: Division of Labor

2.2. Time Management

Due to the nature of the project being confined to the length of the semester, much consideration and planning had to go into creating a project schedule and tracking the progress of the project as the semester continues. We accomplished this by dividing the project into tasks and creating a Gantt chart that allocates time for the tasks to be completed as well as showing relationships between tasks, such as dependencies or concurrencies. Furthermore, we are using the Gantt chart to track the progress of each task, ensuring that it gets completed on time, or shifted appropriately if it needs to be delayed. Figure 2-1 shows the current Gantt chart with our progress as of the time of publishing this report.
### 2.3. Optical Link Budget

Arguably the most important element in the planning of an optical Gigabit Ethernet link, the Optical Link Budget is a method of determining what the best optical parts are based on the requirements of the project and the specifications of the parts in question. First, it is necessary to determine the light power ranges defined in the standard. These are, at the high end, for eye safety, 1mW and, at the low end, $(1\text{mW}) \times (\text{Extinction Ratio}) = 0.1259\text{mW}$, where the extinction ratio is $10^{-\left(\frac{9\text{dB}}{10}\right)}$. Once we know what our target output power for the VCSELs is, then a four corners analysis is done for each part where the lowest and highest extremes on both the power requirements and the part specifications are analyzed to verify that reasonable values
for minimum, maximum, bias, and modulation currents can be achieved. Using this
technique, the best-suited optical component combination can be selected.

2.3.1. VCSEL Budget

When analyzing VCSELs, we considered three main components: Advanced
Optical Components’ HFE4191-541 and HFE418x-521, and Roithner-Lasertechnik’s
TTR-D1. The HFE4191-541 differs from the other AOC component in that it is rated for
2.5 Gbps, not 1.25 Gbps, as well as having overall better statistics.

The HFE418x-521 is an 850nm, 1.25 Gbps VCSEL. Its four corners analysis is
listed in Table 2-2. Because of its extremely high and broad threshold current range,
this is a very poor choice in VCSEL. In fact, on one side of its limits, the maximum
required current exceeds the specifications of the Maxim laser driver chip. Thus, if a
unit is particularly bad, it won’t function no matter how the bias and modulation current
are set.

<table>
<thead>
<tr>
<th>I_{th}</th>
<th>\eta</th>
<th>I_{max}</th>
<th>I_{min}</th>
<th>I_{bias}</th>
<th>I_{mod}</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.50</td>
<td>0.02</td>
<td>53.50</td>
<td>9.79</td>
<td>31.65</td>
<td>43.71</td>
</tr>
<tr>
<td>3.50</td>
<td>0.10</td>
<td>13.50</td>
<td>4.76</td>
<td>9.13</td>
<td>8.74</td>
</tr>
<tr>
<td>6.00</td>
<td>0.02</td>
<td>56.00</td>
<td>12.29</td>
<td>34.15</td>
<td>43.71</td>
</tr>
<tr>
<td>6.00</td>
<td>0.10</td>
<td>16.00</td>
<td>7.26</td>
<td>11.63</td>
<td>8.74</td>
</tr>
</tbody>
</table>

Table 2-2: HFE438x-541 Four Corners Analysis (mA) [4]

The HFE4191-541 is an 850nm, 2.5 Gbps VCSEL. Its four corners analysis is
listed in Table 2-3. This VCSEL is significantly better than the previous component,
because its threshold current is significantly lower. However its slope efficiency is still
not completely desirable. What the slope efficiency determines is how much (in mW)
the output power increases with an increases in input current of 1mA. Obviously 0.04 is
a very small change.

<table>
<thead>
<tr>
<th>I_{th}</th>
<th>\eta</th>
<th>I_{max}</th>
<th>I_{min}</th>
<th>I_{bias}</th>
<th>I_{mod}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.50</td>
<td>0.04</td>
<td>25.50</td>
<td>3.65</td>
<td>14.57</td>
<td>21.85</td>
</tr>
<tr>
<td>0.05</td>
<td>0.16</td>
<td>6.75</td>
<td>1.29</td>
<td>4.02</td>
<td>5.46</td>
</tr>
<tr>
<td>2.50</td>
<td>0.04</td>
<td>27.50</td>
<td>5.65</td>
<td>16.57</td>
<td>21.85</td>
</tr>
<tr>
<td>2.50</td>
<td>0.16</td>
<td>8.75</td>
<td>3.29</td>
<td>6.02</td>
<td>5.46</td>
</tr>
</tbody>
</table>

Table 2-3: HFE4191-541 Four Corners Analysis (mA) [5]
Finally, the TTR-D1 is an 840nm, 1.25 Gbps VCSEL. Its four corners analysis is listed in Table 2-4. This is by far the best component with regards to specifications. It has a slope efficiency that is practically unheard of in the industry.

| TTR-D1 |
|---------|---------|---------|---------|---------|---------|
| $I_{\text{th}}$ | $\eta$ | $I_{\text{max}}$ | $I_{\text{min}}$ | $I_{\text{bias}}$ | $I_{\text{mod}}$ |
| 1.50 | 0.15 | 8.17 | 2.34 | 5.25 | 5.83 |
| 1.50 | 0.35 | 4.36 | 1.86 | 3.11 | 2.50 |
| 3.00 | 0.15 | 9.67 | 3.84 | 6.75 | 5.83 |
| 3.00 | 0.35 | 5.86 | 3.36 | 4.61 | 2.50 |

Table 2-4: TTR-D1 Four Corners Analysis (mA) [6]

Our first choice in VCSEL was the TTR-D1 by far; however, due to limited availability, price, and the fact that the supplier was located in Austria, we could not choose this laser. We went, instead, with the HFE4191-541 from Advanced Optical Components. Despite the fact that it is rated for a speed greater than our needs, its specifications are much tighter and better tuned than the 1.25 Gbps VCSEL. Thus we have chosen the VCSEL for our transmitter: the AOC HFE4191-541.

2.3.2. ROSA Selection

Selecting the ROSA is not nearly as involved as choosing the VCSEL. In fact, once we selected the VCSEL, our choice was pretty much made for us, since we decided ahead of time that we would purchase the VCSEL and ROSA from the same vendor for compatibility reasons.

For the ROSA, we chose the Advanced Optical Components HFD3180-102 LC connectorized ROSA package [7]. Like the VCSEL, it is rated up to 2.5 Gbps, though we will not be using it at that speed. The ROSA has a typical responsivity of 1400 ($\mu$V/$\mu$W). Responsivity is a measure of optical input power to differential voltage output. This responsivity is fine for our purposes.

2.4. Part Selection

With a VCSEL and ROSA selected, the next step was to select our passive components. These components included capacitors, inductors, resistors, and potentiometers. The capacitors and inductors were used at various points throughout the circuit to keep power supply noise from interfering with sensitive parts of the circuit. The values chosen for these passives were 0.01uF and 10nH respectively. These
values were recommended in the project specification and are based on the bandwidth requirements for the circuit.

The potentiometers and two of the resistors are used to control the current entering the VCSEL. These current values are very important to circuit function. If the current to the VCSEL is too low, the VCSEL will not lase. If the current is too high we risk damaging the part. From the four corner analysis, the minimum and maximum bias current ($I_{bias}$) and modulation current ($I_{mod}$) are known. In order to find values for the potentiometer and limiting resistors, it was necessary to find relationships between these currents and their corresponding resistances ($R_{bias}$ and $R_{mod}$).

For $I_{bias}$, Ohm’s Law was used to derive the following equation based on the transmitter schematic (Figure 4-2).

$$R_{bias} = \frac{(V_{CC}-V_{V})}{(I_{bias})}$$

$V_{CC}$ is the power supply voltage and $V_{V}$ is the estimated voltage drop across the VCSEL which was taken to be 2.2V. Using this equation and the known values for $I_{bias}$ the minimum and maximum values for $R_{bias}$ were found to be 169Ohms and 696Ohms. Therefore, a 169Ohm limiting resistor and a 1kOhm potentiometer were used to control $I_{bias}$.

The relationship between $I_{mod}$ and $R_{mod}$ was determined from the MAX3287 data sheet [8]. The data sheet includes a listing of $R_{mod}$ values for several modulation currents (Table 2-5).

<table>
<thead>
<tr>
<th>TEMPCO (ppm/°C)</th>
<th>$I_{MOD} = 30mA$</th>
<th>$I_{MOD} = 15mA$</th>
<th>$I_{MOD} = 5mA$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R_{MOD}$ (kΩ)</td>
<td>$R_{TC}$ (kΩ)</td>
<td>$R_{MOD}$ (kΩ)</td>
</tr>
<tr>
<td>3500</td>
<td>26.7</td>
<td>1.69</td>
<td>53.6</td>
</tr>
<tr>
<td>3000</td>
<td>9.53</td>
<td>2.0</td>
<td>18.7</td>
</tr>
<tr>
<td>2500</td>
<td>5.76</td>
<td>2.49</td>
<td>11.3</td>
</tr>
<tr>
<td>2000</td>
<td>4.12</td>
<td>3.16</td>
<td>8.06</td>
</tr>
<tr>
<td>1500</td>
<td>3.24</td>
<td>4.32</td>
<td>6.19</td>
</tr>
<tr>
<td>1000</td>
<td>2.67</td>
<td>6.49</td>
<td>5.11</td>
</tr>
<tr>
<td>500</td>
<td>2.26</td>
<td>13.3</td>
<td>4.22</td>
</tr>
</tbody>
</table>

Table 2-5: Portion of Maxim Data Sheet [8]
The relationship is nonlinear so a graph of the given values was created in Excel (Figure 2-2). From this graph, an equation relating $R_{mod}$ and $I_{mod}$ was found. This equation was used to calculate $R_{mod}$. The minimum and maximum values were found to be 12.0kOhms and 3.02kOhms. A limiting resistor of 2.7kOhms and a 25kOhm potentiometer were used in the circuit. This calculation has been redone since the original part selection which is why there is a discrepancy in the value of the limiting resistor and the minimum $R_{mod}$. The limiting resistor still provides a significant measure of protection only allowing slightly more than the maximum $I_{mod}$ current when the potentiometer is set to zero.

![Extrapolation of Modulation Resistance](image)

**Figure 2-2: Extrapolation of Modulation Resistance**

The remaining components including the SMA connectors and the power connectors were given in the project specification so no selection was necessary. Part 901-143-6RFX from Jameco Electronics was used for the SMA connector and part CP-002AHPJ-CT from DigiKey Electronics was used for the power connector.

In order to simply ordering, all components that were available were ordered from DigiKey Electronics. Only the SMA connectors and ferrite bead inductors were ordered from other vendors.
2.5. **Financial Budget**

Each group was given $350 to successfully build and test the transmitter and receiver boards. Purchasing costs include VCSELs, ROSAs, passives, board fabrication and shipping costs. As this stage $238.7 has been spent. This puts the project well under budget, but if problems are encountered with parts or design in the coming weeks, further purchases may be necessary. An itemized list of our expenses to date is included in Table 2-6.

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Description</th>
<th>Quantity</th>
<th>Item Number</th>
<th>Unit Price</th>
<th>Amount</th>
</tr>
</thead>
<tbody>
<tr>
<td>DigiKey</td>
<td>Power Connector</td>
<td>1</td>
<td>CP-002AHPJ-CT</td>
<td>$0.900</td>
<td>$0.90</td>
</tr>
<tr>
<td>DigiKey</td>
<td>CAP 10000PF</td>
<td>100</td>
<td>PCC103BNCT-ND</td>
<td>$0.054</td>
<td>$5.40</td>
</tr>
<tr>
<td>DigiKey</td>
<td>RES 100 OHM 1/8W</td>
<td>10</td>
<td>311-100CCT-ND</td>
<td>$0.080</td>
<td>$0.80</td>
</tr>
<tr>
<td>DigiKey</td>
<td>RES 169 OHM 1/8W</td>
<td>10</td>
<td>311-169CCT-ND</td>
<td>$0.080</td>
<td>$0.80</td>
</tr>
<tr>
<td>DigiKey</td>
<td>RES 24 OHM 1/10W</td>
<td>10</td>
<td>RR12Q24DCT-ND</td>
<td>$0.140</td>
<td>$1.40</td>
</tr>
<tr>
<td>DigiKey</td>
<td>RES 2.7K OHM 1/8W</td>
<td>10</td>
<td>311-2.70KCCT-ND</td>
<td>$0.080</td>
<td>$0.80</td>
</tr>
<tr>
<td>DigiKey</td>
<td>POT 1.0K OHM 3/8&quot;</td>
<td>5</td>
<td>3296W-102-ND</td>
<td>$2.500</td>
<td>$12.50</td>
</tr>
<tr>
<td>DigiKey</td>
<td>POT 25K OHM 3/8&quot;</td>
<td>5</td>
<td>3296W-253-ND</td>
<td>$2.500</td>
<td>$12.50</td>
</tr>
<tr>
<td>AOC</td>
<td>VCSEL</td>
<td>4</td>
<td>HFE4191-541</td>
<td>$14.500</td>
<td>$58.00</td>
</tr>
<tr>
<td>AOC</td>
<td>ROSA</td>
<td>4</td>
<td>HFD3180-102</td>
<td>$10.000</td>
<td>$40.00</td>
</tr>
<tr>
<td>Jameco</td>
<td>SMA Connectors</td>
<td>10</td>
<td>901-143-6RFX</td>
<td>$3.450</td>
<td>$34.50</td>
</tr>
<tr>
<td>Express PCB</td>
<td>PCB</td>
<td>3</td>
<td>Custom</td>
<td>$17.00</td>
<td>$51.00</td>
</tr>
<tr>
<td>Mouser</td>
<td>Murata Inductors</td>
<td>10</td>
<td>81-BLM11HA102SG</td>
<td>$0.130</td>
<td>$1.30</td>
</tr>
<tr>
<td></td>
<td>Shipping</td>
<td></td>
<td></td>
<td></td>
<td>$18.83</td>
</tr>
</tbody>
</table>

**Table 2-6: Financial Budget**

**TOTAL** $238.73

2.6. **Bill of Materials**

The bill of materials outlines the costs needed to create a single optoelectronic link as well as the estimated price of producing the link in large quantities. An itemized description of these costs is included in Table 2-7.
<table>
<thead>
<tr>
<th>Vendor</th>
<th>Description</th>
<th>Quantity</th>
<th>Item Number</th>
<th>Unit Price</th>
<th>100k Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>DigiKey</td>
<td>Power Connector</td>
<td>1</td>
<td>CP-002AHJPJ-CT</td>
<td>$0.900</td>
<td>$0.900</td>
</tr>
<tr>
<td>DigiKey</td>
<td>CAP 10000PF</td>
<td>17</td>
<td>PCC103BNCT-ND</td>
<td>$0.054</td>
<td>$0.016</td>
</tr>
<tr>
<td>DigiKey</td>
<td>RES 100 OHM 1/8W</td>
<td>3</td>
<td>311-100CCT-ND</td>
<td>$0.080</td>
<td>$0.017</td>
</tr>
<tr>
<td>DigiKey</td>
<td>RES 169 OHM 1/8W</td>
<td>1</td>
<td>311-169CCT-ND</td>
<td>$0.080</td>
<td>$0.017</td>
</tr>
<tr>
<td>DigiKey</td>
<td>RES 24 OHM 1/10W</td>
<td>10</td>
<td>RR12Q24DCT-ND</td>
<td>$0.140</td>
<td>$0.030</td>
</tr>
<tr>
<td>DigiKey</td>
<td>RES 2.7K OHM 1/8W</td>
<td>1</td>
<td>311-2.70KCCT-ND</td>
<td>$0.080</td>
<td>$0.017</td>
</tr>
<tr>
<td>DigiKey</td>
<td>POT 1.0K OHM 3/8&quot;</td>
<td>1</td>
<td>3296W-102-ND</td>
<td>$2.500</td>
<td>$1.092</td>
</tr>
<tr>
<td>DigiKey</td>
<td>POT 25K OHM 3/8&quot;</td>
<td>1</td>
<td>3296W-253-ND</td>
<td>$2.500</td>
<td>$1.092</td>
</tr>
<tr>
<td>Maxim</td>
<td>Laser Driver</td>
<td>1</td>
<td>MAX3287</td>
<td>$4.430</td>
<td>$4.000</td>
</tr>
<tr>
<td>Maxim</td>
<td>Limiting Amplifier</td>
<td>1</td>
<td>MAX3264</td>
<td>$4.430</td>
<td>$4.000</td>
</tr>
<tr>
<td>AOC</td>
<td>VCSEL</td>
<td>1</td>
<td>HFE4191-541</td>
<td>$14.500</td>
<td>$5.800</td>
</tr>
<tr>
<td>AOC</td>
<td>ROSA</td>
<td>1</td>
<td>HFD3180-102</td>
<td>$10.000</td>
<td>$4.000</td>
</tr>
<tr>
<td>Express PCB</td>
<td>PCB</td>
<td>1</td>
<td>Custom</td>
<td>$17.000</td>
<td>$3.060</td>
</tr>
<tr>
<td>Mouser</td>
<td>Murata Inductors</td>
<td>7</td>
<td>81-BLM11HA102SG</td>
<td>$0.130</td>
<td>$0.042</td>
</tr>
<tr>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td><strong>$59.89</strong></td>
<td><strong>$24.63</strong></td>
</tr>
</tbody>
</table>

Table 2-7: Bill of Materials

As noted in the table, our large quantity per unit price is $24.63. This price competes very well with corresponding electrical Gigabit Ethernet links. One Linksys card retails for $25.99 [9]. Our product is very competitive with this price even when an appropriate profit margin is included. Furthermore, using some methods of manufacturing and board size reduction, the production price could be reduced even further in order that optical Gigabit Ethernet can finally be on the same level as electrical.
3. Test Board

![Eye Diagram from Test Board](image)

We constructed the transmitter portion of a test board for several reasons. First, building this test board gave us our first experience with soldering small surface mount components such as the 0805 size capacitors and the 0603 size inductors. Second, we gained valuable experience in testing and debugging the board as well as collecting data from the oscilloscope and bit error rate tester. We learned the various functions of the oscilloscope such as the triggering menu and capturing waveforms from the screen.

3.1. Test Setup

![Test Setup](image)

Figure 3-2 shows our test setup. The input to our test board came from a pattern generator; a PRBS7 test pattern was used. One of the differential outputs was connected to an attenuator; the other was connected directly to the input of the board. We observed that the oscilloscope at 0dB attenuation produced an undistinguishable eye pattern. Every other setting produced an eye pattern such as that seen in Figure 3-1; a bit
error rate of $10^{-9}$ errors per second. In Figure 3-1 we noticed a signal passing right through the middle of the eye. One explanation for this noise is an error in oscilloscope’s triggering function; we could not resolve this problem.

4. **Design and Layout**

![Figure 4-1: MAX3287 Evaluation Board Schematic [10]](image)
4.1. **Schematic Design**

Our next task after building and testing the evaluation board was to create a schematic for the transmitter and receiver of our optical transceiver. This process was straightforward; for the transmitter we began by studying Maxim’s datasheet for MAX3287 evaluation board. This schematic can be found in Figure 4-1.

From this schematic we derived the wiring for our transmitter (Figure 4-2). The transmitter schematic consists of three basic elements. First, the MAX3287 laser driver is used to supply enough current to the laser driver in order to send an optical (digital) signal to the photodiode. The MAX3287 works by using a differential input which is then converted into a laser bias current of up to 15mA. This bias current is required by the laser in order to “lase” or emit photons of 850nm infrared light to the photodiode. One of the key features of the MAX3287 chip is its ability to regulate the VCSEL bias current such that the VCSEL operates with very low probability of error [8]. Digital optical communication works when a transmitter sends optical power to a receiver; high power (optical) indicates a binary 1 and low power indicates a binary 0. At one gigabit per second it is essential for virtually all of the optical power emitted by the transmitter to be at the correct level—either high or low—in order for the communication to be viable. Therefore, the VCSEL bias current must also perform perfectly to drive the VCSEL. A perfect system would mean that all decisions at the receiver about whether a 1 or 0 was transmitted matches exactly with the original digital signal. However, in practice, an error rate of $10^{-9}$ errors per second or less is observed and is acceptable.

In optical transmitters optical power is converted from electrical power and sent to a receiver at which electrical power is converted back from optical power. The ratio of an electrical binary 1 to electrical binary 0 is equal to the corresponding optical power ratio. This is known as the extinction ratio: $r_0 = I_1/I_0 = P_1/P_0$. Ideally $P_0$ would equal 0 and the extinction ratio would be infinite, however, in practice it is a finite value since $P_0$ must be in the vicinity of the laser threshold (the cutoff point between 1 and 0). The MAX3287 operates with an extinction ratio of about 7 which allows for a low constant bit error rate and minimal power consumption.[8]
Our receiver schematic, seen in Figure 4-3, is shown with the chip MAX3266, a trans-impedance amplifier (TIA). The purpose of the TIA is to amplify the weak voltage signal from the photodiode into a current of about 25mA to the limiting amplifier. This is done by using impedance and the direct application of ohms law $V=IR$. The limiting amplifier (MAX3264) then uses this bias current to output into a differential output—an electrical digital signal. In our transceiver we did not use the MAX3266 because we have opted to use a receiver optical sub assembly (ROSA) which packages this component with the photo diode.
In addition to the MAXIM chips, each schematic includes several passive components. There are capacitors near every power and ground connection. The capacitors help decouple the power connections and ensure that high frequency noise on the power lines does not interfere with sensitive parts of the circuit. In the top left of both the transmitter and receiver schematics there is three element filter that includes two capacitors and a ferrite bead inductor. These filters provide additional protection from the Vcc noise by band-limiting the power signal. The potentiometers in the transmitter circuit (POT1 and POT2) are used to control the modulation current (I_{mod}) and the bias current (I_{bias}). In series with each potentiometer is a 'limiting resistor' which sets a maximum threshold for I_{mod} and I_{bias} is the potentiometer is set to zero.
4.2. Board Design

After designing our transceiver schematic, we proceed to the board design. Our board design required several revisions before submitting the final design to Express PCB for fabrication. For layout of the board we used the Express PCB software which allows for simple and streamlined design of circuits. On the MiniBoard, a 3.8" X 2.5" board, we fit two transceivers. We designed both a non-aggressive and aggressive design in order to test two different design philosophies. On the non-aggressive design, seen on the left half of Figure 4-4, we adhered strictly to symmetric layout of any differential input and output high speed lines. We made sure that no lines exceeded 4 cm; this value was calculated by knowing that since would be operating and 1Gbs, we would need at least 500 MHz signal. However, in order to minimize eye closure, we would require frequencies in the fifth harmonic, or about 2.5 GHz. This would therefore require line lengths of less than 4 cm as given by the equation: \[ \lambda = \frac{c}{f \epsilon} \], where \( \epsilon = 3 \).
We also assured that any angles were kept at approximately 45 degrees and all supply lines were kept away from high speed lines even if they were running under the board. This design decision prevents minimizing any noise from the supply line to the data lines.

In the aggressive design, seen in Figure 4-5, we relaxed these design decisions and allowed right angles and asymmetry to exist. Also, we wanted to position the TOSA and ROSA close together such that they would comply with standards for the SC connector (despite the fact that the VCSEL and ROSA are LC connectorized).

Our design experience led us to several difficulties worth mentioning. First, we had to determine the proper size, shape and pin spacing of the power jack, SMA connector, TOSA, and ROSA. This required finding the component’s datasheet and transferring the mechanical drawing to a PCB component. Next, we had to massage the design several times such that power lines were as far away as possible from data lines and all data lines were symmetrical. We had to assure that power and ground was
supplied correctly to all components. In our third board design, we noticed that our supply lines were daisy chained; this presented a perfect entry for noise into system so we redrew all power traces to prevent noise. Finally, before submitting the board for fabrication, we each individually checked the board against the schematic to assure that all proper connections were made. After five board redesigns, approval by Dr. Brooke and a final board review we submitted the board design to Express PCB for fabrication.

5. First Non-Aggressive Board Run

Our basic build procedure for non-aggressive transceiver is as follows; first, build the transmitter, test it and if it works, continue to the receiver. If it does not work, check the board for errors and make any modifications, if that still does not work then rebuild the board. The process is summarized by the flow diagram in Figure 5-1.

Our first iteration of this procedure for the transmitter yielded a non-working circuit. Voltage measurements showed that the Maxim chip was not receiving any power. A continuity test showed that a short existed from Vcc to ground. We desoldered several components in order to find the short, but were unsuccessful. Eventually we gave up on the first board and started a new transmitter build.

On the second transmitter board, great care was taken when soldering components. In particular connections were checked after each component was soldered and continuity from Vcc to the ground plane was also checked. After this build was completed, the Vcc/ground short problem no longer existed; however, the Vcc trace was still registering 0V. By going back to PCB Express and taking a second look at the transmitter board design layout it was evident that the ground pins from the power
supply were not traced to ground. We were able to fix this problem easily using alligator clips and continue testing.

On further testing of the transmitter we were able to power the maxim chip and trace the signal throughout the board all the way to the VCSEL; however, the VCSEL was still not lasing. This led us to believe that our problem lies in modifying the potentiometers in order to create proper bias current and modulation current as suggested in the four corners analysis. This issue has yet to be resolved, however, we believe that since the threshold and slope efficiency of the VCSEL is unknown, we must try various combinations of bias and modulation currents in order to get the VCSEL to operate.

The following figures show how the input signal was traced throughout the circuit. Figure 5-2 shows the input to the Maxim chip, and Figure 5-3 shows the output of the Maxim chip. 

![Figure 5-2: Input to Maxim Chip](image)
We were able to measure the bias current by adjusting the MODSET potentiometer, measuring its resistance, voltage drop and applying Ohm’s law. The next two figures illustrate how the output of the Maxim chip is affected by adjusting the potentiometer.
As is evident in these figures, increasing the resistance on the POT closes the eye (decreases peak-to-peak voltage) and decreasing resistance opens the eye
(increases peak-to-peak voltage). In order to meet the required modulation current, we plan on making minor adjustments to the potentiometer, measuring its exact resistance and then powering on the circuit and measuring the peak-to-peak voltage.

Another important test issue that we encountered was trying to determine whether or not the VCSEL was lasing. The easiest way was to connect the VCSEL to the pattern generators optical receiver and checking the status of the “Rx LOS” indicator LED (on indicates loss of service, see Figure 5-6). However, in the event that the receiver is faulty, we checked the VCSEL using a cell phone digital camera. Figure 5-6 and Figure 5-7 show the output from the pattern generator’s VCSEL when powered on.

![Figure 5-6: Pattern Generator Transceiver](image)
After our initial failure with the transmitter we moved on to the receiver testing with much more success. In fact, we were able to get a very good eye pattern after the first try. Figure 5-8 shows this result.
6. Conclusion – The Future of Project GaBE

Thus far, Project GaBE has tested both the Maxim Evaluation Board and the test board without issue. The completion of the Optical Link Budget helped us to determine which VCSEL and ROSA we wanted to order for our transceiver. Then we completed a schematic of both our receiver and transmitter, and, using the schematics, designed a board layout that would be both feasible and meet our goals for both the conservative and aggressive designs. Finally, with all parts ordered and received, we built the first prototype of our transceiver and began testing it.

Having begun our first testing cycle, we can confidently say that, despite some issues with the transmitter, our design is feasible and will be successful. Furthermore, with the way we are keeping to our schedule and tracking on our Gantt chart, we can promise that we will have a working product by our promised delivery date of April 26, 2005. Our next steps will be to complete the testing cycle and determine what the issues are. Then we will address these issues in the schematics and board design, making the necessary alterations in preparation for our second board run and prototype. This second board will be designed to not only correct the issues in the first board but also to address the issue of crosstalk prevalent when the transmitter and receiver are in use at the same time. This second board will be then enter a final test cycle with the hopes that it will be flawless. Success will mean that the final milestone of Project GaBE has been reached.
References

http://standards.ieee.org/  
http://searchsmb.techtarget.com/sDefinition/0,,sid44_gci803517,00.html  
http://www.roithner-laser.com/All_Datasheets/VCSELs/TTR-D1_.PDF  
http://www.maxim-ic.com/quick_view2.cfm/qv_pk2146  