Dr. Martin A. Brooke

Associate Professor

School of Electrical and Computer Engineering

April, 2007

1 EDUCATIONAL BACKGROUND

Degree	Year	University	Field
Ph.D.	1988	University of Southern California	Electrical Engineering
M.S.E.E.	1982	University of Southern California	Electrical Engineering
B.E.	1981	University of Auckland	Electrical Engineering

2 EMPLOYMENT HISTORY

Associate Professor with Tenure	Duke University	2003-Present
Associate Professor with Tenure	Georgia Institute of Technology	1994-2003
Assistant Professor	Georgia Institute of Technology	1988-1994
Research Assistant	The University of Southern California	1983-1988
Instructor	The University of Southern California	1981-1983
Research Assistant	University of Auckland, New Zealand	1980-1981
Engineering Cadet	New Zealand Electricity	1976-1980

3 TEACHING

1 Individual Student Guidance

2 Postdoctoral Fellows Supervised

1. Axel Thomsen, from Fall 1992 to Fall 1993, research into Thermally Stable Reference Design and Dynamic Range Enhancement of Laser Driver Amplifier Circuits. Now at Crystal Data Acquisition Division, Cirrus Logic Inc., Austin, TX.

2.Youngjoong Joo, from Spring 1999 to Spring 2000, research area: Sigma Delta Converters for Image Processing Focal Planes. Now an Assistant Professor at Arizona State University.

3.Daeik Kim, from Fall 2003 to Spring 2005, research area: Sigma Delta Converters for Sensors. Now at IBM.

4.Seokhun Hyun, from Spring 2004 to Fall 2006, research area: Integrated Circuits for Sensors. Now at Samsung.

3 Ph.D. Students Supervised

Ph.D. Students Graduated

1. Stephen Goodman, graduated Spring 1992, "Temporal Pattern Recognition Using Neural Networks with Application to Data Compression." Now a Full Professor of Electrical Engineering at the West Virginia University, Institute of Technology, Montgomery, West Virginia. GT Council of Outstanding Young Engineering Alumni inductee 1995.

2. Terry Sculley (co-advised with Phillip Allen), graduated Summer 1992, "High-Speed Analog to Digital Converters Using Neural Networks." Now at ESS Technology, Inc., Austin, TX, and an Adjunct Associate Professor at The University of Texas at Austin.

3. Axel Thomsen, graduated Fall 1992, "High-Speed High-Precision Signal Processing Using Parallel Analog Circuitry." Now at Crystal Data Acquisition Division, Cirrus Logic Inc., Austin, TX, and an Adjunct Assistant Professor at The University of Texas at Austin

4. Kenichi Hirotsu, graduated Summer 1993, "Neural Network Hardware with a Random Weight Change Learning Algorithm." Now at Sumitomo Electric Industries, Osaka, Japan.

5. Myunghee Lee, graduated Spring 1996, “A Quasi-Monolithic Optical Receiver Using a Standard Digital CMOS Technology.” Now at Agilent Technologies, Inc., San Jose, CA.

6. Lamar West, graduated Summer 1997, "Analysis of Laser Clipping in the Reverse Path of Cable Television Transmission Systems." Now at Scientific Atlanta, Atlanta GA.

7. Wei Zhou, graduated Summer 1997, "Neural Network Prediction and Modeling of Turbulence." Now at Bell South, Atlanta, GA.

8. John Tabler, graduated Fall 1997, "Trainable ADC Applications in Telecommunications." Now at Cadence Design Systems, Dallas TX.

9. Ravi Poddar, graduated Winter 1998, "Parasitics Extraction for High Speed Passives." Now at Transmeta Inc, San Jose, CA.

10. Youngjoong Joo, graduated Spring 1999, “A High Speed Image Acquisition System for Focal Plane Arrays.” Now an Assistant Professor at Arizona State University.

11. Jin Liu, graduated Spring 1999, "Real Time Control Using Hardware Neural Networks." Now an Assistant Professor at the University of Texas at Dallas, Dallas, TX.

12. Jae Joon Chang, graduated Summer 2000, "CMOS Differential Analog Optical Receivers with Hybrid Integrated I-MSM Detectors." Now at Agilent Technologies, Inc., San Jose, CA.

13. Liang Chu, graduated Fall 2001, “ADSL System Enhancement with Multi-User Detection.” Now at IBM T.J. Watson Research Labs, NY.

14. Brent Buchanan, Graduated Summer 2001, “Spatial Oversampling for Mixed Signal Image Processing Hardware.” Now at Philips Semiconductor, Bolder, Co.

15. Larry Carastro, Graduated Spring 2002, “Predictive Statistical Analysis Of Embedded Meander Resistors Via Measurement of Canonical Building Blocks.” Now at Philips Semiconductor, Norcross, GA.

16. Sungyong Jung, Graduated Spring 2002, “A High dI/dt CMOS Differential Optical Transmitter for a Laser Diode.” Now an Assistant Professor at the University of Texas at Arlington, Arlington, TX.

17. Indal Song, began advising Spring 2000, “10 Gbps CMOS Receiver with Thin Film Integrated Detector.” Now at Samsung.

18. Cheolung Cha, began advising Spring 2000, “Predictive, Scalable, Broad Band Modeling of I-MSM phtotodetectors for co-optimization of PD-TIA designs.” Now at ETRI.

19. Daeik Kim, graduated Spring 2003, “Fully Integrated Delta-Sigma Analog to Digital Converter and Optoelectronic Interface Circuits for Optoelectronic Biological Sensor.” Now at IBM.

20. Borte Terlemez “VCO design for 2.4 GHz RF integrated circuit,” Now at Maxim (Turkey) (Borte was John Uymera's Student)

21. Seokhun Hyun, graduated Spring 2004, “40 Gbps Thin-Film InP HBT – CMOS Hybrid Receiver with Thin Film Integrated I-MSM Detector.” Now at Samsung in Korea.

22. Jaehong Kim, graduated Spring 2004, “Predictive, Scalable, Broad Band Modeling of Thin Film laser diodes.” Now at Teradyne Corp.

23. Jaemin Shen, graduated Spring 2004, “Circuits for System on a Package Integrated Optoelectronic Interfaces and Interconnections.” Now at Intel.

Ph.D. Students in Process

1.Xin Cai, began advising Summer 2004, “Compact CPU for sensors.”

2.Arnak Aleksanyani, began advising Spring 2006, “Compact ADC for sensors.”

3.Heather Wake, began advising Spring 2004, passed qualifying exam Fall 2005, “Integrated Circuit Electrophoresis.”

4 M.S. Thesis Students Supervised

M.S. Thesis Students Graduated

1. Curt Karnstedt, began advising Winter 97, completion date Winter 99, “Optoelectronic Transimpedance Amplifier Design.”

2. Olivier Geradier, began advising Fall 1996, completion date Fall 98, “Laser Driver design.”

3. Kamran Assadian, began advising Fall 1993, completion date Fall 95, “Analog Computation Engine.”

4. Guang Ping Shen, began advising Winter 1993, completion date Spring 95, “Design of Low Power Amplifiers.”

5. Zhuang Hou, began advising Fall 1993, completion date Fall 95, “Laser Driver Design.”

6. Jay Bolton, began advising Fall 1993, completion date Fall 95, “10 Msps 14-bit Nonlinearity Correcting Analog to Digital Converter.”

7. Bruce Adams, began advising Fall 1990, completion date Fall 92, “Communications Applications of Neural Networks.”

8. Teng Sin Pong, began advising Fall 1988, completion date Fall 90, “Analog Integrated Circuit Model Reduction to User Specified Accuracy.”

9. P. Erik Pace, completion date Winter 2003, “1394 Optoelectronic Data Link Prototype.” (TI Analog Fellow)

10. Norman W. Chin See, completion date Winter 2003, “Passive Free CMOS PLL Design.” (TI Analog Fellow)

11. Tracy Yeh, completion date Winter 2003, “1 Gbps optoelectronic data links.”

M.S. Project Students in Process

1. Gary Pan, began advising Fall 2006, completion date Fall 2007, “.”

2. Qun Woo, began advising Fall 2006, completion date Fall 2007, “.”

3. Raymond Kryskowski, began advising Fall 2006, completion date Fall 2007, “.”

5 Undergraduate Research Students

1.Gerardo Holmann, Fall 1988, and Winter 1989, "Software for a General Purpose Circuit Database Interpreter."

2.Roy Myers, Jr., Summer 1989, Fall 1989, and Winter 1990, "Stability Analysis of Nonlinear Analog Circuit to Solve Power System Load Flows."

3.William Paradise, Summer 1989, Fall 1989, and Winter 1990, "Construction of a Discrete Analog Circuit to Solve Power System Load Flows."

4.Keith Schamis, Summer 1989, "Software for a General Purpose Circuit Database Interpreter."

5.Robert Sterling, Summer 1989, Fall 1989, and Winter 1990, "Software for Extraction of Parasitics Models for VLSI Interconnects to a User Specified Accuracy."

6.Shih-Cheng Wang, Summer 1989, "Construction of a Discrete Analog Circuit to Solve Power System Load Flows."

7.Jose Pino, Summer 1989, Fall 1989, and Winter 1990, "Design of an Analog CMOS Neural Network Integrated Circuit," see conference proceedings II.H.2.1.

8.Yuan Lou, Fall 1990, "Design of a Dynamically Loaded Static Random Access Memory Cell."

9.Jim Caravella, Winter 1990, "Develop Technology File for Analog Devices Bipolar IC Fabrication Process."

10.Roy Thompson, Winter 1991, "Design, Fabrication and Test of EEPROM Devices for Analog Neural Networks."

11.Jeremy Jones, Winter 1991, "Design, Fabrication and Test of EEPROM Devices for Analog Neural Networks."

12.Yorgen Anderson, Summer 1990, Fall 1990, Winter 1991, "Design of a Neural Network Signal Processor for Correction of 3-D Accelerometer Non-idealities."

13.Robin Williams, Summer 1990, Fall 1990, Winter 1991, "Design, Fabrication, and Test of BiCMOS Circuits."

14.Steve Carter, Summer 1990, Fall 1990, Winter 1991, "Fabrication and Test of EEPROM Devices for Analog Circuit Trimming."

15.Eddie Gauthier, Summer 1990, Fall 1990, Winter 1991, "Fabrication and Test of Test Structures to Measure the Effect of Layout Techniques on CMOS Device Matching."

16.John Boyes, Summer 1990, Fall 1990, Winter 1991, "Design, Fabrication, and Test of a Digitally Controlled Analog Neural Network IC."

17.Ho Tien Chen, Spring 1990, Summer 1990, Fall 1990, "Software for Variable Accuracy Modeling of Analog Interconnect Parasitics."

18.Ravi Poddar, Summer 1990, Fall 1990, Winter 1991, "Parasitics Extraction for High Speed Semiconductor Devices."

19.William Mansfield, Summer 1991, Fall 1991, Winter 1992, "Design, Fabrication and Test of an Analog Neurocomputer."

20.Daniel Rassmussen, Summer 1991, Fall 1991, Winter 1992, Summer 1992, "Design of an Analog Neurocomputer for Sensor Fusion."

21.Tracy Satterwhite, Fall 1992, Winter, Spring and Summer 1993, "Development of Test Components for MOSIS IC Foundry."

22.Lisa Riadi, Fall 1993, "Learning Algorithms for Focal Plane Processing."

23.David Coccarelli 2007, “Investigation of Spectroscopy using LEDs.”

6 Continuing Education

Unless otherwise stated Professor Brooke was the major contributor to the courses listed.

1. "Analog VLSI CAD," IEEE International Conference on Computer Aided Design, (one of three presenters), San Jose, CA, November, 1989.

2. "Analog VLSI CAD," IEEE International Symposium on Circuits and Systems (one of three presenters), New Orleans, LA, April 1990.

3. "Parallel Circuit Design Techniques for High-Speed Analog Circuits," video course recorded for the Semiconductor Research Corporation (SRC), Raleigh, NC, presented with Ph.D. student Terry Sculley, July 1990.

4. "Neural Networks: Theory and Application," 3-day short course taught with 6 other faculty from ECE, GTRI and Math Departments. Enrollment: 75. Dr. Brooke was an equal contributor to planning and presentation. Campus, March 28-30, 1994

5. "Neural Networks: Theory and Application," 3-day short course taught with 6 other faculty from ECE, GTRI and Math Departments. Enrollment: 45. Dr. Brooke was an equal contributor to planning and presentation. Campus, October 23-27, 1994

6. "Integrated Optoelectronics Onto Silicon Circuits: Devices, Integration, Systems," 5-day short course lecture and hands-on layout experience; ARPA is funding fabrication of short course participants' designs. Brooke has responsibility for 1/3 of lecture portion.

7. "Neural Networks, Genetic Algorithms, and Fuzzy Logic" 4-day short course to be taught with 9 other faculty from ECE, GTRI and Math Departments. Brooke was an equal contributor to planning and presentation. Campus, May 9-12, 1995

8. "Optoelectronics Integrated Onto Silicon VLSI, Devices, Circuits, Systems," IEEE International Symposium on Circuits and Systems, with N. Jokerst, and S. Wills, Atlanta GA, May 12–15, 1996.

7 Curriculum Development

A leading developer of the Georgia Tech Electrical and Computer Engineering Senior Design Course (ECE 4006). This is an ABET mandated Major Design Experience for all Electrical and Computer Engineering students. Dr. Brooke is focusing on the RF and Analog Circuits projects, especially circuits for Gigabit Ethernet optical data transmission. This course is now ECE 135 at Duke.

4 Awards

1.**Analog Devices Career Development Professorship**, 1988-1993.

2.National Science Foundation **Research Initiation Award** (RIA), 1990.

3.Sigma Xi Research Award: **Undergraduate Research Adviser**, 1990.

4.Undergraduate Research Opportunity Program, **Outstanding Research Award**, 1990.

5.IEEE Midwest Symposium on Circuits and Systems, Myril B. Reed **Best Paper Award** for Thomsen, A., and Brooke, M. A., "A Temperature Stable Current Reference Source with Programmable Output," 1992.

6.Advanced Technology Development Center **Faculty Research Commercialization** Award, 1993.

7.IEEE Electronic Components Technology Conference, **Outstanding Poster Paper Award**, 2003

8.Georgia Institute of Technology campus wide award: **Outstanding Doctoral Thesis Adviser**, 2003.

5 SCHOLARLY ACCOMPLISHMENTS

1 Published Books and Parts of Books

1. Brooke, M. A., "Chip Parasitics," in *The Circuits and Filters Handbook,* Chapter 10.1.5, (W. Chen, Ed.), CRC Press, Inc. (1993).

2 Refereed Journal Publications

1. Moinian, S., Brooke, M. A., and Choma Jr., J., "BITPAR: Process-Derived Bipolar Transistor Parameterization," *IEEE Journal of Solid-State Circuits*, vol. SC-21, no. 2, pp. 344-352, April, 1986.

2. Pong, T. S., and Brooke, M. A., "A Parasitics Extraction and Network Reduction Algorithm for VLSI," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 10, no. 2, pp. 145-149, February 1991.

3. Thomsen, A., and Brooke, M. A., "An EEPROM-device with Tunneling Injector Fabricated Using a Standard Double-Polysilicon CMOS-Process," *IEEE Electron Device Letters,* vol. 12, no. 3, pp. 111-113, March, 1991.

4. Camperi-Ginestet, C., Kim, Y. W., Jokerst, N. M., Allen, M. G., and Brooke, M. A., "Vertical Electrical Interconnection of Compound Semiconductor Thin Film Devices to Underlying Silicon Circuitry," *IEEE Photonics Technology Letters*, vol. 4, no. 9, pp. 1003-1006, September, 1992.

5. Thomsen, A., and Brooke, M. A., "A Programmable Piece-Wise Linear Large Signal CMOS Amplifier," *IEEE Journal of Solid State Circuits,* vol. 28, no. 1, pp. 84-89, January, 1993.

6. Goodman, S. D., and Brooke, M. A., "Symbolic Substitution System for Data Compression," *Applied Optics*, vol. 32, no. 5, pp. 752-760, 10 February, 1993.

7. Thomsen, A., and Brooke, M. A., "A Floating Gate CMOS Signal Conditioning Circuit for Nonlinearity Correction," *Analog Integrated Circuits and Signal Processing*, vol. 4, no. 1, pp. 21-29, July, 1993.

8. Thomsen, A., and Brooke, M. A., "A Multi-Gate Dual-Injector Floating Gate MOSFET and Its Applications," *IEEE Transactions on Circuits and Systems I*, vol. 41, no. 6, pp. 443- 454, June, 1994.

9. Tabler, J., Brooke, M. A., Dorsey, J. F., and Arayani, S., "Solution of the Power Flow Equations Using Parallel Analog Computing," *International Journal in Computer Simulation*, vol. 4, no. 4, 1994.

10. Bond, J. A., Dorsey, J. F., Brooke, M. A., Magill, J., and Tabler, J., "Fast Solution of Nonlinear Equations Using Parallel Analog Hardware," *Analog Integrated Circuits and Signal Processing*, no. 6, pp. 135-156, 1994.

11. Lacy, W. S., Camperi-Ginestet, C., Buchanan, B., Wills, S., Jokerst, N. M., and Brooke, M. A., "A Fine-Grain, High-Throughput Architecture Using Through-Wafer Optical Communication," *IEEE Journal of Lightwave Technology*, vol. 13, no. 4, pp. 1085-1092, June, 1995.

12. Sculley, T. L., and Brooke, M. A., "Nonlinearity Correction Techniques for High Speed, High Resolution A/D Conversion," *IEEE Transactions on Circuits and Systems*, vol. 42, no. 3, pp. 154-163, March, 1995.

13. Jokerst, N. M., Camperi-Ginestet, C., Buchanan, B., Wilkinson, S., and Brooke, M., "Communication Through Stacked Silicon Circuitry Using Integrated Thin Film InP-Based Emitters and Detectors," *IEEE Photonics Technology Letters*, vol. 7, no. 9, pp. 1028-1030, September, 1995.

14. Fike, S. Buchanan, B., Jokerst, N. M., Brooke, M., Morris, T., and DeWeerth, S., "8 X 8 Array of Thin Film Photodetectors Vertically Electrically Interconnected to Silicon Circuitry," *IEEE Photonics Technology Letters*, vol. 7, no. 10, pp. 1168-1170, October, 1995.

15. Jokerst, N., Brooke, M., Vendier, O., Wilkinson, S., Fike, S. Lee, M., Twyford, E., Cross, J., Buchanan, B., and Wills, S., "Thin Film Multimaterial Optoelectronic Integrated Circuits," *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part B*, vol. 19, no. 1, February, 1996, **Invited**.

16. Cross, J., Buchanan, B., Carastro, L., Lopez-Lagunas, A., Wang, T., Jokerst, N., Brooke, M., Wills, S., and Ingram, M., "A Single Fiber Bi-Directional Optical Link Using Co-Located Emitters and Detectors," *IEEE Phot. Tech. Lett.*, vol. 8, no. 10, October, 1996.

17. Burton, B.R., Kamran, F., Harley, R. G., Habetler, T. G., Brooke, M., and Poddar, R., "Identification and Control of Induction Motor Stator Currents Using Fast On-Line Random Training of a Neural Network," *IEEE Transactions on Industry Applications,* vol. 33, no. 3, pp. 697-704, May/June 1997.

18. Gibson, D., Poddar, R., May, G., and Brooke, M., "Statistically based parametric yield prediction for integrated circuits," *IEEE Transactions on Semiconductor Manufacturing*, vol. 10, no. 4, pp. 445-458, November, 1997.

19. Kamran, F., Harley, R. G., Burton, B. R., Habetler, T. G., and Brooke, M. A., "A Fast On-Line Neural-Network Training Algorithm for a Rectifier Regulator," *IEEE Transactions on Power Electronics*, vol. 13, no. 2, pp. 366-372, March, 1998.

20. May, P., Lee, M., Wilkinson, S., Vendier, O., Ho, Z., Bond, S., Wills, D., Brooke, M., Jokerst, N., and Brown, A., "Design Issues for Through-Wafer Optoelectronic Multicomputer Interconnects," *IEEE Journal of Parallel and Distributed Computing, Special Issue on Parallel Computing with Optical Interconnects,* vol. 41, no. 1, pp. 3019, February, 1997.

21. Lee, M., Brooke, M., Vendier, O., and Jokerst, N., "A Scaleable CMOS Current-Mode Preamplifier Design for an Optical Receiver," *The International Journal of Analog Circuits and Signal Processing*, vol. 12, no. 2, pp. 133-144, February, 1997.

22. May, P., Cross, J., Lopez, J., Wills, D., Jokerst, N., and Brooke, M., "Improvement in Bit Error Rate for Optoelectronic Multicomputer Interconnection Networks Using Cyclic Redundancy Code Error Detection" *IEEE Photonics Technology Letters,* vol. 9, no. 6, pp. 848-850, June, 1997.

23. Poddar, R., Moon, E., Brooke, M., and Jokerst, N., "Accurate, Rapid, High Frequency Empirically Based Predictive Modeling of Arbitrary Geometry Planar Resistive Passive Devices," *IEEE Trans. On Components, Packaging, and Manufacturing Technology, Part B,* vol. 21, no. 2, pp. 177-183, May, 1998.

24. Vendier, O., Bond, S., Lee M., Jung S., Brooke, M., Jokerst, N., and Leavitt, R., "Stacked Silicon CMOS Circuits with a 40-Mb/s Through-Silicon Optical Interconnect," *IEEE Photonics Technology Letters,* vol. 10, no. 4, pp. 606-608, April, 1998.

25. Poddar, R. and Brooke, M., "Accurate High Speed Empirically Based Predictive Modeling of Deeply Embedded Gridded Parallel Plate Capacitors Fabricated in a Multilayer LTCC Process," *IEEE Transactions on Advanced Packaging*, Vol. 22, No. 1, pp. 26-31, February, 1999.

26. Gibson, D.S., Poddar, R., May, G.S., and Brooke, M.A., "Using Multivariate Nested Distributions to Model Semiconductor Manufacturing," *IEEE Transactions on Semiconductor Manufacturing*," vol. 12, no. 1, pp. 53-65, February, 1999.

27. Bergman, J.I., Chang, J., Joo, Y., Matinpour, B., Laskar, J., Jokerst, N.M., Brooke, M.A., Brar, B., and Beam, E., "RTD/CMOS Nanoelectronic Circuits: Thin-Film InP-based Resonant Tunneling Diodes Integrated with CMOS Circuits," *IEEE Electron Device Letters*, vol. 20, no. 3, p.119-22, March, 1999.

28. Bond, S., Vendier, O., Lee, M., Jung, S., Lopez-Lagunas, A. Chai, S., Dagnall, G., Brooke, M., Jokerst, N., Wills, D., and Brown, A., "A Three Layer 3D Silicon System Using Through-Si Vertical Optical Interconnections and Si CMOS Hybrid Building Blocks," *IEEE Journal on Special Topics in Quantum Electronics: Smart Photonics*, vol. 5, no. 2, pp. 276-286, March, 1999.

29. Joo, Y., Park, J., Thomas, M., Chung, K., Brooke, M., Jokerst, N., and Wills, D., "Smart CMOS Focal Plane Arrays: A Si CMOS Detector Array and Sigma Delta Analog to Digital Converter Imaging System," *IEEE Journal on Special Topics in Quantum Electronics: Smart Photonics*, vol. 5, no. 2, pp. 296-305, March 1999.

30. Lopez-Lagunas, A., Chai, S., Cross, J., Buchanan, B., Carastro, L., Wang, S., Wills, D., Brooke, M., and Jokerst, N., "Bidirectional Single Fiber Low-cost Optoelectronic Interconnect for Automotive Applications," *IEEE Transactions on Vehicular Technology*, vol. 49, no. 1, pp. 281-286, 2000.

31. Jokerst, N., Brooke, M., Laskar, J., Wills, D., Brown, A., Vrazel, M., Jung, S., Joo, Y., and Chang, J., "Microsystem Optoelectronic Integration for Mixed Multisignal Systems," *IEEE Journal on Special Topics in Quantum Electronics Millennium Issue*, vol. 6, no. 6, pp. November/December, 2000, Invited**.**

32. Seo, S. W., Lee, K. K., Kang, S. B., Huang S., Doolittle, W. A., Jokerst, N. M., Brown, A. S., and Brooke, M. A., "The Heterogeneous Integration of GaN Thin Film Metal-Semiconductor-Metal Photodetectors Onto Silicon," *IEEE Photonics Technology Letters*, vol.14, no.2 pp.185-7, 2002

33. Liu, J., Brooke, M.A., and Hirotsu, K. "A CMOS feedforward neural-network chip with on-chip parallel learning for oscillation cancellation," *IEEE Transactions on Neural Networks*, vol. 13, no. 5, pp. 1178-1186, Sept., 2002.

34. Sang-Yeon Cho, Sang-Woo Seo, Brooke, M.A., Jokerst, N.M., "Integrated detectors for embedded optical interconnections on electrical boards, modules, and integrated circuits," *IEEE Journal on Selected Topics in Quantum Electronics*, vol. 8 , no. 6, pp. 1427 -1434, Nov.-Dec. 2002.

35. Jokerst, N. M., Brooke, M., Cho, S. Y., Wilkinson, S., Vrazel, M., Fike, S., Tabler, J., Joo, Y. J., Seo, S. W., Wills, D. S., Brown, A., "The Heterogeneous Integration of Optical Interconnections Into Integrated Microsystems," *IEEE Journal of Special Topics in Quantum Electronics*, vol. 9, no. 2, pp. 350-360, March/April, 2003.

36. Cho, Sang-Yeon, Brooke, M.A., Jokerst, N.M., "Optical interconnections on electrical boards using embedded active optoelectronic components," IEEE Journal on Selected Topics in Quantum Electronics, vol. 9, no. 2, pp. 465–476, March-April 2003.

37. Glytsis, E.N., Jokerst, N.M., Villalaz, R.A., Sang-Yeon Cho, Shun-Der Wu, Zhaoran Huang, Brooke, M.A., Gaylord, T.K., "Substrate-embedded and flip-chip-bonded photodetector polymer-based optical interconnects: analysis, design, and performance," *Journal of Lightwave Technology*, vol. 21, no. 10 , pp. 2382 - 2394, Oct. 2003.

38. Buchanan, B.; Brooke, M. "An experimental evaluation of error spectrum shaping applied to mixed-signal image convolutions," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 50, No 12, pp. 950-962 Dec. 2003.

39. High-speed large-area inverted InGaAs thin-film metal-semiconductor-metal photodetectors, Sang-Woo Seo; Sang-Yeon Cho; Sa Huang; Jeng Jung Shin; Jokerst, N.M.; Brown, A.S.; Brooke, M.A.; Selected Topics in Quantum Electronics, IEEE Journal of Volume 10, Issue 4, July-Aug. 2004 Page(s):686 - 693

40. Planar lightwave integrated circuits with embedded actives for board and substrate level optical signal distribution Jokerst, N.M.; Gaylord, T.K.; Glytsis, E.; Brooke, M.A.; Cho, S.; Nonaka, T.; Suzuki, T.; Geddis, D.L.; Shin, J.; Villalaz, R.; Hall, J.; Chellapa, A.; Vrazel, M.; Advanced Packaging, IEEE Transactions on [see also Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] Volume 27, Issue 2, May 2004 Page(s):376 - 385

41. Board-level optical interconnection and signal distribution using embedded thin-film optoelectronic devices Sang-Yeon Cho; Sang-Woo Seo; Jokerst, N.M.; Brooke, M.A.; Lightwave Technology, Journal of Volume 22, Issue 9, Page(s):2111 – 2118, Sept. 2004.

42. Parasitic modeling and analysis for a 1-Gb/s CMOS laser driverSungyong Jung; Brooke, M.A.; Jokerst, N.M.; Jin Liu; Youngjoong Joo; Circuits and Systems II: Express Briefs, IEEE Transactions on [see also Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on] Volume 51, Issue 10, Page(s):517 – 522, Oct. 2004.

43. Fang Liu, Sule Ozev, Martin Brooke, “Identifying the Source of BW Failures in High Frequency Linear Analog Circuits Based on S-Parameter,” *IEEE Transactions on Computer Automated Design*. Volume: 25, Issue: 11, pp 2594-2605, November 2006.

44. Jeffrey J. Lillie, Mikkel A. Thomas, Karla A. Dennis, Daeik Kim, Martin Brooke, Nan Marie Jokerst, Clifford L. Henderson, and Stephen E. Ralph, “Multimode Interferometric Sensors-on-Silicon Optimized for Fully Integrated CMOS Chem/Bio Sensor Platforms,” accepted for publication in the *Journal of the Optical Society of America, B,* vol 23, pp 642-651, 2006.

2. Conference Presentations with Proceedings (refereed)

1. Brooke, M. A. and Choma, J., Jr., "The Programmable Analog Array: A Reconfigurable General Purpose Analog Integrated Circuit," *Proceedings of the 31st Midwest Symposium of Circuits and Systems,* vol. 1, pp. 841-844, St. Louis, MO, August 9-12, 1988.

2. Sculley, T. L. and Brooke, M. A., "A Neural Network Approach to High Performance Analog Circuit Design," *Proceedings of the 32nd Midwest Symposium of Circuits and Systems,* vol. 1, pp. 497-501, Urbana-Champaign, IL, August 1989.

3. Pong, T. S. and Brooke, M. A., "A Parasitics Extraction and Network Reduction Algorithm Applied to VLSI," *Proceedings of the 32nd Midwest Symposium of Circuits and Systems,* vol. 1, pp. 559-562, Urbana-Champaign, IL, August 1989.

4. Thomsen, A. and Brooke, M. A., "An Analog-Divider-Design Based on a Perceptron-Neural-Network," *Proceedings of the International Joint Conference on Neural Networks,* vol. II, pp. 441-445, Washington, DC, 16-19th January 1990.

5. Sculley, T. L. and Brooke, M. A., "Obtaining High Precision Operation from Non-Ideal Neural Networks," *1990 IEEE International Symposium on Circuits and Systems Proceedings*, vol. 3, pp. 1847-1851, New Orleans, LA, May 1-3, 1990.

6. Thomsen, A. and Brooke, M. A., "A New Structure for an Analog Divider," *1990 IEEE International Symposium on Circuits and Systems Proceedings*, vol. 3, pp. 1721-1724, New Orleans, LA, May 1-3, 1990.

7. Pino, J. L., Sculley, T. L., and Brooke, M. A., "A Compact Digitally Controlled Perceptron Integrated Circuit Implementation with Process Insensitivity," *1990 IEEE International Symposium on Circuits and Systems Proceedings*, vol. 2, pp. 1066-1069, New Orleans, LA, May 1-3, 1990.

8. Goodman, S. D., Gray, W. S., and Brooke, M. A., "A Novel Neural Network for Temporal Pattern Identification with Applications to Control Systems," *The Proceedings of the Fifth IEEE International Symposium on Intelligent Control*, pp. 473-478, Philadelphia, PA, September 5-7, 1990.

9. Goodman, S. D. and Brooke, M. A., "A Novel Neural Network for Temporal Pattern Identification with Applications to Data Compression," *Proceedings of the International Joint Conference on Neural Networks,* vol. II, p. A-897, Seattle, WA, June 1991.

10. Thomsen, A. and Brooke, M. A., "A Low-Cost Application-Specific Neural Network Implementation with Floating Gate Weights," *Proceedings of the International Joint Conference on Neural Networks,* vol. II, pp. 565-570, Baltimore, MD, June 1992.

11. Sculley, T. and Brooke, M. A., "Simulation Results for an Adjustable A/D Converter Architecture," *Proceedings of the 35th Midwest Symposium of Circuits and Systems*, vol. 1, pp. 56-60, Washington, DC, August 1992.

12. Thomsen, A. and Brooke, M. A., "A Temperature Stable Current Reference Source with Programmable Output," *Proceedings of the 35th Midwest Symposium of Circuits and Systems,* vol. 2, pp. 831-835, Washington, DC, August 1992.

13. Buchanan, B., Brooke, M. A., and Madisetti, V. "A Parallel Analog Circuit to Perform Fourier Transforms," *Proceedings of the 35th Midwest Symposium of Circuits and Systems*, vol. 2, pp. 1353-1359, Washington, DC, August 1992.

14. Tabler, J. and Brooke, M. A., "Analog Solution of Nonlinear Equations," *Proceedings of the 32nd Midwest Symposium of Circuits and Systems*, vol. 1, pp. 764-768, Washington, DC, August 1992.

15. Camperi-Ginestet, C., Kim, Y., Jokerst, N., Allen, M., and Brooke, M., "Three Dimensional Integrated Circuits: Epitaxial Lift Off GaAs Photodetectors Integrated Directly on Top of Silicon Circuits," *Proceedings of the IEEE Summer Topical Meeting on Smart Pixels*, pp. 24-25, Santa Barbara, CA, August, 1992.

16. Hirotsu, K. and Brooke, M., "An Analog Neural Network Chip With Random Weight Change Learning Algorithm," *Proceedings of 1993 International Joint Conference on Neural Networks*, vol. 3, pp. 3031–3034, Nagoya, Japan, October 1993.

17. Camperi-Ginestet, C ,Buchanan, B., Jokerst, N. M., Allen, M. G., and Brooke, M. A., " Three Dimensional Smart Pixel Integration of a GaAs-Based Detector Array Directly on Top of Silicon Circuits," *Proceedings of the IEEE Summer Topical Meeting on Smart Pixels*, pp. 2-56 –2-58 Lake Tahoe, NV, July, 1994.

18. Lee, M., Camperi-Ginestet, C., Jokerst, N. M., and Brooke, M. A., "Silicon CMOS Optical Receiver Circuit with Integrated Compound Semiconductor Thin-Film P-i-N Detector," *Proceedings of the IEEE Summer Topical Meeting on Opto-Electronics*, pp. 58-59, Lake Tahoe, NV, July, 1994.

19. Wills, D., Jokerst, N., and Brooke, M., " A Fine-Grain, High-Throughput Architecture Using Through-Wafer Optical Interconnect," *Proceedings of the MPPOI Workshop,* pp. 27 –36, Cancun, Mexico, August, 1994. Held jointly with the IEEE Computer Society International Parallel Processing Symposium.

20. Tabler, J. and Brooke, M., "Compact Precise Digital to Analog Converter Arrays in a Low Cost, Low Precision Short Channel CMOS Process," *Proceedings of the 37th Midwest Symposium of Circuits and Systems,* vol. 2, pp. 1183-1186, Lafayette, LA, August 1994.

21. Buchanan, B., Camperi-Ginestet, C., Morris, T., Brooke, M. A., DeWeerth S., Jokerst, N. M. and Allen, M. G., "High Density Focal Plane Signal Processing Using 3-D Vertical Interconnects," *Proceedings of the 37th Midwest Symposium of Circuits and Systems*, vol. 1, pp. 191 –194, Lafayette, LA, August 1994.

22. Lee, M. and Brooke M. A., "Design, Fabrication, and Test of a 125Mbps Transimpedance Amplifier using MOSIS 1.2 micron Standard Digital CMOS Process," *Proceedings of the 37th Midwest Symposium of Circuits and Systems*, vol.1, pp. 155 –157, Lafayette, LA, August 1994.

23. Gibson, D., Poddar R., May G., and Brooke M., "Using Neural Networks to Estimate Probability Density Distributions," *1995 World Congress on Neural Networks*, pp. 122-127, Washington, DC., July 18, 1995.

24. Kamran, F., Harley, R. G., Burton, B.R., Habetler, T. G., and Brooke, M., "A Fast On-Line Neural Network Training Algorithm for a Rectifier Regulator," *Proceedings of the IEEE Industrial Electronics Conference (IECON),* vol. 2, pp. 1462-1467, November, 1995.

25. Burton, B.R., Kamran, F., Harley, R. G., Habetler, T. G., Brooke, M., and Poddar, R., "Identification and Control of Induction Motor Stator Currents Using Fast On-Line Random Training of a Neural Network," *IEEE-IAS Annual Meeting Conference Record*, pp. 1781-1794, October, 1995.

26. Brown, A., Jokerst, N., Brooke, M., Wills, D., and Allen, M., "Multi-Material Packaging for Optoelectronics and High Speed Electronics," *Proceedings of the First Annual Symposium on Advanced Packaging*, Atlanta, February 7-9, 1995.

27. Brooke, M., Lee, M., Jokerst, N., and Camperi-Ginestet, C., "Silicon CMOS Optical Receiver Circuits with Integrated Thin Film Compound Semiconductor Detectors," *Proceedings of the Society of Photo-Instrumentation Engineers Photonics West*, ***pp San Jose, CA, February 12-15, 1995.

28. Camperi-Ginestet, C., Buchanan, B., Wilkinson, S., Jokerst, N., and Brooke, M., "Thin Film InP-Based Emitters and Detectors Integrated Onto a Silicon Driver and Amplifier Circuit," *Proceedings of the Optical Society of America Topical Meeting on Optical Computing*, Salt Lake City, UT, March 13-17, 1995.

29. Jokerst, N., Brooke, M., Allen, M., and Wills, D., "Manufacturable Multi-Material Integrated Systems," *Proceedings of the Workshop in Manufacturing Process Development in Photonics*, pp. 225-227, Huntsville, AL, April, 1995.

30. Camperi-Ginestet, C., Buchanan, B., Jokerst, N., and Brooke, M., "Bi-Directional Communication Through Stacked Silicon Circuitry Using Integrated Thin Film InP-Based Emitters and Detectors," *Proceedings of the Conference on Lasers and Electro-Optics (CLEO)*, Baltimore, June, 1995, Published in *IEEE Photonics Technology Letters*, vol. 7, pp. 1028 –1030, Sept. 1995.

31. Fike, S., Buchanan, B., Jokerst, N., Brooke, M., Morris, T, and DeWeerth, S., "8 x 8 Array of Thin Film Photodetectors Integrated Directly on Top of Silicon Circuitry," *Proceedings of the Conference on Lasers and Electro-Optics (CLEO)*, Baltimore, June, 1995. , Published in *IEEE Photonics Technology Letters,* vol. 7, pp. 1168 –1170, Oct. 1995.

32. May, P., Wilkinson, S.T., Jokerst, N.M., Wills, D.S., Lee, M., Vendier, O., Bond, S.W., Hou, Z.; Dagnall, G., Brooke, M.A., Brown, A., "Design Issues for Through-Wafer Optoelectronic Multicomputer Interconnects," *Proceedings of the Second International Conference on Massively Parallel Processing Using Optical Interconnections (MPPOI)*, pp. 8-15, San Antonio, TX, October 23-24, 1995.

33. Lee, M., Vendier, O., Brooke, M.A., Jokerst, N.M., and Leavitt, R.P., "CMOS Optical Receiver with Integrated Compound Semiconductor Thin-Film Inverted MSM Detector Operating at 155 Mbps," *Proceedings of the 8th Annual IEEE Lasers and Electro-Optics Meeting*, pp. 47-48, San Francisco, CA, Oct. 30- Nov. 2, 1995.

34. Wills, D., Jokerst, N., Brooke, M., and Brown, A., "Two-Layer Image Processing System Incorporating Integrated Focal Plane Detectors and Through-Wafer Optical Interconnect," *Proceedings of the Optical Society of America Topical Meeting on Optical Computing*, pp. 19-22, Salt Lake City, UT, March 13-17, 1995.

35. Cat, H.H., Lee, M., Buchanan, B., Wills, D.S., Brooke, M., and Jokerst, N.M., "Silicon VLSI Processing Architectures Incorporating Integrated Optoelectronic Devices," in *Proceedings of the 16th Conference on Advanced Research in VLSI*, pp. 17-27, Chapel Hill, NC, March 1995.

36. Wills, D. S., Jokerst, N. M., Brooke, M. A., and Brown, A., **"**Three Dimensional, Massively Parallel, Optically Interconnected Silicon Computational Hardware and Architectures for High Speed IR Scene Generation," in *Proceedings of the 1995 SPIE Symposium on OE/ Aerospace Sensing and Dual Use Photonics: Targets and Backgrounds: Characterization and Representation*, Volume 2469, pp. 141-145, Orlando, FL, April 1995.

37. Jokerst, N. M., Brooke, M. A., Vendier, O., Wilkinson, S., Fike, S., Lee, M., Twyford, E., Cross, J., Buchanan, B., and Wills, D. S., "Thin Film Multi-Material Optoelectronic Integrated Circuits," in *Proceedings of the Society of Photo Instrumentation Engineers Annual Meeting*, ***pp 22 pages, San Diego, CA, July 1995.

38. Jokerst, N. M., Brooke, M. A., Vendier, O., Fike, S., Lee, M., Buchanan, B., Wills, D. S., and Brown, A., "Smart Detectors: Devices, Integration, Circuits, and Systems," in *Proceedings of the Society of Photo Instrumentation Engineers Annual Meeting*, ***pp 12 pages, San Diego, CA, July 1995.

39. Cat, H.H., Eble, J.C., Wills, D.S., De, V.K., Brooke, M., and Jokerst, N.M., "Low Power Opportunities for a SIMD VLSI Architecture Incorporating Integrated Optoelectronic Devices," *Proceedings of GOMAC'96*, pp. 59-62, Orlando, FL, March, 1996.

40. Vendier, O., Wilkinson, S. T., Bond, S. W. , Lee, M., Hou, Z., Lopez-Lagunas, A., May, P., Brooke, M., Jokerst, N. M., Wills, S., and Leavitt, R. P., "A 155 Mbps Digital Transmitter Using GaAs Thin Film LEDs Bonded to Silicon Driver Circuits," *Proceedings of the IEEE LEOS Summer Topical Meeting on Smart Pixels*, pp. 15-16, Keystone, CO, August, 1996.

41. Lee, M., Vendier, O., Brooke, M., Jokerst, N. M., and Leavitt, R. P., "A 250 Mbps CMOS optical receiver with an integrated InGaAs thin film inverted MSM detector," *Proceedings of the IEEE LEOS Summer Topical Meeting on Smart Pixels*, pp. 17-19, Keystone, CO, August, 1996.

42. Cross, J., Buchanan, B., Carastro, L., Lopez-Lagunas, A., Wang, T., Jokerst, N., Brooke, M., Wills, S., Ingram, M., "A Smart Pixel Single Fiber Bi-Directional Optical Link," *Proceedings of the IEEE Lasers and Electro-optic Society Summer Topical Meeting on Smart Pixels*, pp. 45-46, Keystone, CO, August, 1996.

43. Vendier, O., Lee, M., Brooke, M., Jokerst, N. M. and Leavitt, R. P., "An Integrated 200 Mb/s Receiver: A Silicon CMOS Transimpedance Amplifier with a Thin Film InGaAs Photodetector," *Proceedings of the Conference on Lasers and Electro-optics (CLEO'96)*, vol. 9, pp. 402-403, Anaheim, CA, May, 1996.

44. Bond, S.W., Lee, M., Chang, J .J., Vendier, O., Hou, Z., Brooke, M., Jokerst, N.M., and Leavitt, R.P., "An Integrated 155 Mbps Digital Transmitter Using a 1.3um Wavelength Thin Film LED," *Proceedings of the Ninth Annual IEEE Lasers and Electro-optics (LEOS) Meeting*, vol. 1, pp. 342–343, Boston, MA, November, 1996.

45. Cat, H.H.; Gentile, A.; Eble, J.C.; Myunghee Lee; Vendier, O.; Young Joong Joe; Wills, D.S.; Brooke, M.; Jokerst, N.M.; Brown, A.S, "SIMPil: An OE Integrated SIMD Architecture for Focal Plane Processing Applications," *Proceedings of the 3rd Massively Parallel Processing Using Optical Interconnections Conference (MPPOI '96)*, pp. 44-52. Maui, Hawaii, October, 1996.

46. Poddar, R. and Brooke, M. "Accurate, High Speed Modeling of Integrated Passive Devices in Multichip Modules," *IEEE Topical Meeting on Electrical Performance of Electronic Packaging*, pp. 184-186, Napa, CA, Oct. 1996.

47. Liu J., Burton, B., Kamran, F., Brooke, M.A., Harley, R.G., Habetler, T.G., "High Speed On-line Neural Network Control of an Induction Motor Immune to Analog Circuit Nonidealities," *Proceedings of the 1997 IEEE Symposium on Circuits and Systems (ISCAS)*, vol. 1, pp. 633–636, Hong Kong, June 1997.

48. Chai, S. M., Lopez-Lagunas, A., Wills, D. S., Jokerst, N. M., and Brooke, M. A., "Systolic Processing Architectures Using Optoelectronic Interconnects," *Proceedings of the Fourth International Conference on Massively Parallel Processing Using Optical Interconnections*, pp. 160-166, Montreal, Canada, June, 1997.

49. Joo, S. Fike, K. S. Chung, M. A. Brooke, N. M. Jokerst, D. S. Wills, "Application of Massively Parallel Processors to Real Time Processing of High Speed Images," *Proceedings of the Fourth International Conference on Massively Parallel Processing Using Optical Interconnections*, pp. 96-100, Montreal, Canada, June 1997.

50. Chun, C.; Vendier, O.; Moon, E.; Laskar, J.; Ki, H.C.; Jokerst, N.M.; Brooke, M. Mondal, J., "Integrated 1.55 μm receivers using GaAs MMICs and thin film InP detectors," *1998 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp.187-90, Baltimore, MD, 7-9 June 1998.

51. Laskar, J., Jokerst, N., Brooke, M., Harris, M., Chun, C., Pham, A., Liang, H., Staiculescu, D., and Sutono, S., "Review of RF packaging research at Georgia Tech's PRC," *Proceedings 4th International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces*, pp.139-50, Braselton, GA, March 15-18, 1998.

52. Robinson, W. H., Wills, D. S., Brooke, M., and Jokerst, N., "IRIS: An integrated, scalable focal plane architecture," *Proceedings of the 1998 11th Annual Meeting IEEE Lasers and Electro-Optics Society,* LEOS. Part 2 (of 2), pp. 184-185, Orlando, FL, Dec. 1-4, 1998.

53. Brooke, M., Jokerst, N. M., Bond, S. W.; and Wills, D. S., "Comparison of CMOS chip to chip interconnections: Vertical optical through-Si links versus high density electrical interconnect," *Proceedings of the 1998 11th Annual Meeting IEEE Lasers and Electro-Optics Society*, LEOS. Part 2 (of 2), pp. 186-187, Orlando, FL, Dec. 1-4, 1998.

54. Bond, S. W., Jung, S., Vendier, O., Brooke, M. A., and Jokerst, N. M., "3D stacked Si CMOS VLSI smart pixels using through-Si optoelectronic interconnections," *Proceedings of the 1998 IEEE/LEOS Summer Topical Meeting*, pp. 27-28, Monterey, CA, July 20-24, 1998.

55. Joo Y., Fike, S., Thomas, M., Kee S. C., Brooke, M., Jokerst, N.M., and Wills D. S., "High speed, smart focal plane processing using integrated photodetectors and Si CMOS VLSI sigma delta analog to digital converters," *Proceedings of the 1998 IEEE/LEOS Summer Topical Meeting*, pp. 55-56, Monterey, CA, July 20-24, 1998.

56. Liu, J. and Brooke, M. A. "Fully Parallel On-chip Learning Hardware Neural Network for Real Time Control," *1999 IEEE International Symposium on Circuits and Systems Proceedings*, vol. 5, pp. 371-374, Orlando, FL, May 1999.

57. Carastro, L.A.; Poddar, R.; Moon, E.; Brooke, M.A.; Jokerst, N. M., "Passive Device Modeling Methodology Using Nonlinear Optimization," Proceedings of the 1999 *IEEE International Symposium on Circuits and Systems Conference*, vol. 6, pp. 53-56, Orlando, FL, May 30-June 2, 1999.

58. Chang, J.J.; Myunghee L.; Sungyong J.; Brooke, M.A.; Jokerst, N.M.; Wills, D.S. "Fully Differential Current-Input CMOS Amplifier Front-End Suppressing Mixed Signal Substrate Noise for Optoelectronic Applications," *International Circuits and Systems Conference*, vol. 1, p. 327-330, Orlando, FL, June 1, 1999.

59. Park J., Tabler, J.A., Brooke, M.A., Jokerst, N.M., and Wills, D.S., "Adaptive Digital Bias Control for an Optical Receiver and Transmitter," *International Circuits and Systems Conference*, vol. 1, pp. 323-326, Orlando, FL, June 1, 1999.

60. Liu, J. and Brooke, M. A. "Fully Parallel Learning Neural Network Chip for Real-Time Control," *Proceedings of The International Joint Conference on Neural Networks (IJCNN '99)*, vol. 4, pp. 2323–2328, Washington, DC, USA, July 10-16, 1999.

61. Jokerst, N., Brooke, M., Laskar, J., Wills, D., Brown, A., and Ingram, M., "Building Collaborative Teams For Multi-Disciplinary Educational Projects in Optoelectronics," *Proceedings of the Education and Training in Optics and Photonics Conference*, Cancun, Mexico, July, 1999.

62. Jokerst, N.; Brooke, M.; Laskar, J.; Wills, D.; Brown, A.; Vendier, O.; Bond, S.; Cross, J.; Vrazel, M.; Thomas, M.; Lee, M.; Jung, S.; Joo, Y.; Chang, J., "Smart Photonics: Optoelectronics Integrated Onto Si CMOS Circuits," *IEEE Lasers and Electro-Optic Society (LEOS) Annual Meeting*, vol. 2, pp. 423-424, San Francisco, CA, November, 1999.

63. Jokerst, N. M., Brooke, M. A., Laskar, J., Wills, D. S., Brown, A. S., Vendier, O., Bond, S. W., Cross, J. B., Vrazel, M., Thomas, M., Lee, M., Jung, S., Joo, Y., and Chang, J. J., "Smart Photonics: Optoelectronics Integrated With Si CMOS VLSI Circuits," *Proceedings of the SPIE Special Symposium on the Future of Computing*, ***pp San Diego, CA, vol.4109, pp.241-51, July, 2000.

64. Jokerst, N., Brooke, M., Laskar, J., Wills, D., Brown, A., Vendier, O., Bond, S., Cross, J., Vrazel, M., Thomas, M., Lee, M., Jung, S., Joo, Y., and Chang, J., "Smart Photonics: Optoelectronics Integrated with Si CMOS VLSI Circuits," *Society of Photo Instrumentation Engineers Optical Science and Technology Meeting*, ***pp San Diego, CA, August, 2000.

65. Jokerst, N. M., Brooke, M. A., Laskar, J., Wills, D. S., Brown, A. S., Bond, S. W., Vrazel, M., Huang, R., Thomas, M., Kuo, H., Cho, S., Jung, S., Joo, Y., and Chang, J., "Smart Photonic Links: Optoelectronic Devices Integrated With Circuits and Interconnection Substrates," *Digest of the Optical Society of America Annual Meeting*, Providence, RI, p. 94, October, 2000.

66. Carastro, L., Ilgu Y., Poddar, R., Brooke, M.A., and May, G.S. "Statistical Analysis of Embedded Capacitors using Monte Carlo Simulation," *Proceedings of the 50th Electronic Components & Technology Conference*, pp. 198-205, Las Vegas, NV, USA, May, 2000.

67. Vrazel, M., Chang, J., Brooke, M., Jokerst, N., Joo, Y., Carastro, L., Dagnall, G., Brown, A., "Analysis of Alignment Tolerant Hybrid Optoelectronic Receivers for High Density Interconnection Substrates," *Proceedings of the 50th Electronic Components & Technology Conference*, pp. 223-230, Las Vegas, Nevada, May, 2000.

68. Chang, J., Vrazel, M., Brooke, M., Jokerst, N., "Mixed Signal Hybrid OEICs: An InP I-MSM Integrated Onto a CMOS Analog Optical Receiver with a Digital CMOS Microprocessor," *Optoelectronics in Computing Conference*, Quebec, Canada, June, 2000.

69. Vrazel, M., Chang, J., Brooke, M., Jokerst, N., Dagnall, G., and Brown, A., "Alignment Tolerant Hybrid Photoreceivers Using Inverted MSMs," *IEEE Lasers and Electro-Optics Society Topical Meeting on Electronics-Enhanced Optics*, pp.I23-I24, Florida, July, 2000.

70. Lee, K., Seo, S., Huang, S., Joo, Y., Doolittle, W., Fike, S., Jokerst, N., Brooke, M., and Brown, A., "Design of a Smart Pixel Multispectral Imaging Array Using 3D Stacked Thin Film Detectors on Si CMOS Circuits," *IEEE Lasers and Electro-Optics Society Topical Meeting on Electronics-Enhanced Optics*, pp. I57-I58, Florida, July, 2000.

71. Joo Y., Brooke, M.A., and Jokerst, N.M., "Compact current input oversampling modulator design for a scalable high frame rate focal plane arrays," *Proceedings of the 2000 IEEE International Symposium on Circuits and Systems: Emerging Technologies for the 21st Century*, p.9-12 vol.5, 2000.

72. Vrazel, M., Chang, J.J., Brooke, M., Jokerst, N.M., Dagnall, G., and Brown, A., "Alignment Tolerant InP/Si CMOS Hybrid Integrated Photoreceivers Operating at 0.9 Gbps," *Proceedings of the IEEE Lasers and Electro-Optics Society 2000 Annual Meeting*, San Juan, Puerto Rico, vol. 2, pp. 884-885, November, 2000.

73. Jung, S.; Brooke, M.A.; Jokerst, N.M., "Packaging Considerations for 1 Gbps Si CMOS Optical Driver," *Proceedings of the IEEE Lasers and Electro-Optics Society 2000 Annual Meeting*, Puerto Rico, vol. 2, pp. 882-883.November, 2000,

74. Joo, Y., Lee, K., Seo, S.; Jokerst, N., and Brooke, M., "A modulator design for smart pixel multispectral imaging arrays," *Proceedings of the IEEE Lasers and Electro-Optics Society 2000 Annual Meeting*, Puerto Rico, Volume: 1, November, 2000, pp. 171 –172.

75. Chang, J.J., Jung, S., Vrazel, M., Jung, K., Lee, M., Brooke, M.A., Jokerst, N.M., Wills, D.S., "Mixed Signal Hybrid OEICs: An InP I-MSM Integrated Onto a CMOS Analog Optical Receiver with a Digital CMOS Microprocessor," *Proceedings of the Optics in Computing Conference*, 2000.

76. Chang, J.J. and Brooke, M.A. "A clock extraction circuit using passive components-free filter in standard digital process," *Proceedings. ISCAS 2000 Geneva*. The 2000 IEEE International Symposium on Circuits and Systems 2000, vol. 2, pp. 261-264, Geneva, 2000.

77. Chang, J.J.; Jung, S.; Vrazel, M.; Jung, K.; Lee, M.; Brooke, M.A.; Jokerst, N. "Hybrid optically interconnected microprocessor: an InP I-MSM integrated onto a mixed-signal CMOS analog optical receiver with a digital CMOS microprocessor," *Proceedings of the SPIE*, vol.4089, pp.708-14, 2000.

78. Brooke, M.A., “Enhanced imaging arrays using a sigma delta ADC in Si CMOS for each array pixel,” *Digest of the LEOS Summer Topical Meetings*, pp. I11-I12, 2000.

79. Vrazel, M.; Jae Joon Chang; In-Dal Song; KeeShik Chung; Brooke, M.; Jokerst, N.M.; Brown, A.; Wills, D.S., “Highly alignment tolerant InGaAs inverted msm photodetector heterogeneously integrated on a differential Si CMOS receiver operating at 1 Gbps,” *Proceedings of the 51st Electronic Components and Technology Conference*, Las Vegas, May, 2001, pages 8-13.

80. Chu, L.C. and Brooke, M. “An enhancement study on the SDSL upstream receiver,” The 2001 *IEEE International Symposium on Circuits and Systems*, Melbourne, Australia, May, 2001, vol. 4, pp. 442–445.

81. Chu, L.C. and Brooke, M. “Mitigation of Crosstalk on The SDSL Upstream Transmission With Vector Equalization,” *Proceedings of the IEEE International Conference on Communications*, Helsinki, Finland, June 11-14, 2001, pages 165-169.

82. Chu, L.C. and Brooke, M. “A Study on Multi-user DSL Channel Capacity with Crosstalk Environment,” *Proceedings of IEEE Pacific Rim, Conference on Communications, Computers and signal Processing, 2001,* (PACRIM., 2001), pp. 176–179, August, 2001

83. Brown, A.S.; Jokerst, N.M.; Doolittle, A.; Brooke, M.; Kuech, T.F.; Sang-Woo Seo; Sangbeom Kang; Sa Huang; Jeng-Jung Shen, “Heterogeneous integration: from substrate technology to active packaging,” *IEDM Technical Digest*., pp. 9.3.1-4, 2001.

84. N. Jokerst, M.A. Brooke, A.S. Brown, S.Y. Cho, R. Huang, S.W. Seo, M. Thomas, I. Song, S.H. Hyun, D.I. Kim “*Optoelectronic microsystems integration for systems on a package and systems on chip applications,*” 2002 OSA Annual Meeting, TuV1, Orlando, Florida, Oct, 2002 (Invited).

85. Jeff Lillie, Dae-ik Kim, Mikkel Thomas, Martin Brooke, Nan Jokerst, S.E. Ralph, “Highly multimode interferometric sensors,”. 2002 *OSA Annual Meeting*, TuL37, Orlando, Florida, Oct, 2002.

86. Comparison of electrical and optical interconnect Jaernin Shin; Chung-Seok Seo; Chellappa, A.; Brooke, M.; Chattejce, A.; Jokerst, N.M.; Electronic Components and Technology Conference, 2003. Proceedings. 53rd May 27-30, 2003 Page(s):1067 - 1072

87. High speed optical interconnection using embedded PDs on electrical boards Sang-Yeon Cho; Hall, J.D.; Chellappa, A.; Jokerst, N.M.; Brooke, M.; Electronic Components and Technology Conference, 2003. Proceedings. 53rd May 27-30, 2003 Page(s):1046 - 1052

88. Optical chip-to-chip interconnects for memory systems Bourdreaux, O.; Sang-Yeon Cho; Jaemin Shin; Chellappa, A.; Schimmel, D.; Brooke, M.; Jokerst, N.M.; Lasers and Electro-Optics Society, 2003. LEOS 2003. The 16th Annual Meeting of the IEEE Volume 1, 27-28 Oct. 2003 Page(s):301 - 302 vol.1

89. Test-structure free modeling method for de-embedding the effects of pads on device modeling Cheolung Cha; Zhaoran Huang; Jokerst, N.M.; Brooke, M.A.; Electronic Components and Technology Conference, 2003. Proceedings. 53rd May 27-30, 2003 Page(s):1694 - 1700

90. A 1.4G samples/sec comb filter design for decimation of sigma-delta modulator output Kim, D.D.; Brooke, M.A.; Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on Volume 1, 25-28 May 2003 Page(s):I-1009 - I-1012 vol.1

91. Diagnosis of small-signal parameters for broadband amplifiers through S-parameter measurements and sensitivity-guided evolutionary search Fang Liu; Ozev, S.; Brooke, M.; Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference on 7-11 Nov. 2004 Page(s):641 - 647

92. Single fiber bi-directional links using 3D stacked thin film emitters and detectors integrated onto CMOS transceiver circuits Geddis, D.L.; Hyun, S.H.; Chang, J.; Jung, S.; Brooke, M.A.; Jokerst, N.M.; Lasers and Electro-Optics, 2004. (CLEO). Conference on Volume 2, 16-21 May 2004 Page(s):2 pp. vol.2

93. A 10 Gbit/s Si CMOS transimpedance amplifier with an integrated MSM photodetector for optical interconnections Indal Song; Sang-Woo Seo; Seokhun Hyun; Daeik Kim; Sa Huang; Brooke, M.; Jokerst, N.M.; Brown, A.; Lasers and Electro-Optics Society, 2004. LEOS 2004. The 17th Annual Meeting of the IEEE Volume 2, 7-11 Nov. 2004 Page(s):517 - 518 Vol.2

94. Etch enhanced low capacitance, large area thin film InGaAs metal-semiconductor-metal photodetectors Sang-Woo Seo; Cheolung Cha; Sang-Yeon Cho; Sa Huang; Jokerst, N.M.; Brooke, M.A.; Brown, A.S.; Lasers and Electro-Optics Society, 2004. LEOS 2004. The 17th Annual Meeting of the IEEE Volume 1, 7-11 Nov. 2004 Page(s):222 - 223 Vol.1

95. Data acquisition sensitivity determination of a sensor-on-a-chip integrated microsystem Kim, D.D.; Brooke, M.A.; Jokerst, N.M.; Lillie, J.J.; Thomas, M.A.; Ralph, S.E.; Sensors, 2004. Proceedings of IEEE 24-27 Oct. 2004 Page(s):1297 - 1300 vol.3

96. Wideband multiple resonance small-signal laser diode model for the co-design of laser drive circuits Jae Hong Kim; Jaemin Shin; Cheolung Cha; Jokerst, N.M.; Brooke, M.; Circuits and Systems, 2004. MWSCAS '04. The 2004 47th Midwest Symposium on Volume 2, 25-28 July 2004 Page(s):II-181 - II-183 vol.2

97. Jaemin Shin, Cheolung Cha, Sangycon Cho, Jaehong Kim, Jokerst, N.M., Brooke, M., " FR4 printed circuit board design for Giga-bits embedded optical interconnect applications," Proceedings of the Electronic Components and Technology Conference, ECTC '04. Volume 2, Pages 1996-2001, 2004.

98. An interferometric sensor for integration with Si CMOS signal processing circuitry: "Sensor on a chip" Thomas, M.A.; Lillie, J.; Dae-Ik Kim; Ralph, S.; Jokerst, N.M.; Brooke, M.; Dennis, K.; Comeau, B.; Henderson, C.L.; Lasers and Electro-Optics, 2004. (CLEO). Conference on Volume 1, 2004 Page(s):2 pp. vol.1

99. Comparative high speed optical interconnections using thin film photodetectors embedded in polymer waveguides Sang-Yeon Cho; Sang-Woo Seo; Jokerst, N.M.; Brooke, M.; Electronic Components and Technology, 2005. ECTC '05. Proceedings 31 May-3 June 2005 Page(s):1611 - 1616 Vol. 2

100. Time-interleaved switched-capacitor filter for reconfigurable triple-band delta-sigma converter Kim, D.D.; Brooke, M.A.; Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on 23-26 May 2005 Page(s):1402 - 1405 Vol. 2

101. Jaemin Shin, Jae Hong Kim, Cheolung Cha, Jokerst, N.M., Brooke M., "Rapid, predictive measurement-based modeling for high frequency interconnect on FR4 substrates," Proceedings of the Electronic Components and Technology Conference, ECTC '05. Vol. 2, Pages 1835-1841, 2005.

102. Integrated mixed-signal optoelectronic system-on-a-chip sensor Kim, D.D.; Thomas, M.A.; Lillie, J.J.; Dennis, K.S.; Comeau, B.M.; Brooke, M.A.; Jokerst, N.M.; Ralph, S.E.; Henderson, C.L.; Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on 23-26 May 2005 Page(s):1738 - 1741 Vol. 2

Other Publications

3 Published Papers (non-refereed)

1. Jokerst, N. M., Allen, M. G., Brooke, M. A., Drabik, T., and Toon, J., "Mixing Optics and Electronics: New Technology May Offer Low-Cost High Quality Integrated Optic Devices," *Georgia Tech News Release* published in whole or in part as:

2. "Mass Produced Integrated Optoelectronic Circuits," *Inside R & D: The Weekly Report on Technical Innovation*, vol. 20, no. 22, p. 1, May 29, 1991.

3. "New Technology May Offer Low-Cost High Quality Integrated Optic Devices," *C^{3}I News*, p. 2, June 1991.

4. "Mixing Optics and Electronics," *Industry Week*, Emerging Technologies Section, p. 54, July 1, 1991.

5. "New Technology May Offer Low-Cost Integrated Optoelectronics," *Optoelectronic Engineering Reports*, Society of Photo-Instrumentation Engineers, no. 91, p. 2, July 1991.

6. "Lift-Off Technology Mixes Optics and Electronics," *Design News*, p. 6, July 8, 1991.

7. "Georgia Tech Fabricates Integrated Optoelectronics," *Photonics Spectra*, p. 56, July 1991.

8. "Georgia Tech Makes GaAs 'Chiplets,'" *Lasers & Optronics*, July 1991.

9. "Georgia Tech Integrates Si, GaAs ICs Via 'Lift-Off,'" *Semiconductor International*, p. 30, August 1991.

10. "New Manufacturing Process Lowers OEIC Cost," *Optics and Photonics News*, Optical Society of America, p. 34, September 1991.

11. Thomsen, A., Brooke, M. A., and Toon, J. D., "Learning to Improve Themselves: Neural Networks Help Devices Enhance Their Own Accuracy and Performance," *Georgia Tech News Release*, September 25, 1992, published in whole or in part as:

12. "Analog IC Integrates Neural Network," *Electronic Design*, circulation 165,000, p. 26, October 15, 1992.

13. "Neural Net ICs," *Designfax*, circulation 110,189, November 1, 1992

14. "Neural Net ICs," *Medical Equipment Designer*, circulation 15,000, November 1, 1992.

15. "Neural Net ICs," *Design Engineering*, circulation 18,500, November 1, 1992.

16. "Neural Net ICs," *Design News*, circulation 169,392, November 9, 1992.

17. "Neural Nets Help Devices Help Themselves," *Advanced Manufacturing Technology*, vol. 13, no. 12, p. 12, December 15, 1992.

18. "Neural Net ICs," *Tooling and Production The Manufacturing Magazine*, circulation 80,100, p. 16, January 1, 1993.

19. "Neural Networks Become More Human," *R&D Magazine*, p. 71, May 1993.

20. Martin A. Brooke, Stephen P. DeWeerth, "Merging Optics and Electronics in Neural Networks," *Optics and Photonics News*, pp. 27-29, June 1993.

4 Other Scholarly Accomplishments

5 Software

1.ICEPAR: An Integrated Circuit Device Parasitics Modeling Tool. Installed at Analog Devices Inc., CLD Division, Greensboro, NC, August 1990. Brooke wrote first version of software and designed final version which was written by S. Moinian. Brooke and R. Poddar have updated software for Analog Devices.

2.JUMBLE: A Parasitics Extraction and Network Reduction Algorithm for VLSI, installed at Analog Devices Inc., Norwood, MA, February 1991, and Cadence Software, San Jose, CA, July 1993. Brooke co-developed theory, software written by Brooke's graduate student T. S. Pong.

6 Patents Granted

1."Processes for Lift-Off of Thin Film Materials and for the Fabrication of Three Dimensional Integrated Circuits," with N. Jokerst and M. Allen, U.S. Patent No. 5,244,818, Date: 9/14/1993, Referenced by 10 later Patents.

2.“Three Dimensional Integrated Circuits with Lift-Off,” ," with N. Jokerst and M. Allen, U.S. Patent No. 5,280,184, Date: 1/18/1994, Referenced by 6 later Patents.

3."Processes for Lift-Off and Deposition of Thin Film Materials," with N. Jokerst, M. Allen, and T. Drabik, U.S. Patent No. 5,286,335, Date: 2/15/1994, Referenced by 7 later Patents.

4."Processes for Lift-Off of Thin Film Materials or Devices for Fabricating Three Dimensional Integrated Circuits, Optical Detectors, And Micromechanical Devices," with N. Jokerst and M. Allen, U.S. Patent No. 5,401,983, Date: 3/28/1995, Referenced by 6 later Patents.

5."System and Method for Learning Neural Network for Generating Random Directions for Weight Changes," with Kenichi Hirotsu, US Patent No. 5,455,891, Date: 10/3/1995

6.“System and Method for Bi-Directional Optical Communication,” with N. Jokerst , US Patent No. 6,603,584, Date: 8/5/2003.

6 SERVICE

1 Professional Contributions

Memberships

1.Member, Institute of Electrical and Electronic Engineers, 1987-present.

Society Service

1. Member, Steering Committee, IEEE MWSCAS Conference, 2002-present

2. Chair Atlanta joint Section of IEEE Circuits and Systems and Solid State Circuits 1999-2003

3. Elected Chairperson of the Microelectronic and Microstructures Implementation Special Interest Group of the International Neural Network Society, May 1992. One-year term as Chairperson then one year as Past-Chairperson.

4. Elected a member of the Analog Signal Processing Subcommittee of the IEEE Circuits and Systems Society, two-year term, June 1992-94.

Proposal Review Activity

1.Reviewer of NSF Proposals in Analog Signal Processing for CISE/MIP directorate.

2.Reviewer of NSF Proposals in Design Tools and Test for CISE/MIP directorate.

3.Reviewer of NSF Proposals in Hybrid and Integrative Systems ENG direcortate.

Reviewer Work for Technical Journals

1. Reviewed a paper for *Neural Networks, The Journal of the International Neural Network Society*

2. Reviewer of papers for *IEEE Transactions on Circuits and Systems*.

3. Reviewer of papers for *IEEE Transactions on Electron Devices*.

4. Reviewer of papers for *IEEE Transactions on Neural Networks*.

5. Reviewer of papers for *IEEE Journal of Solid State Circuits*.

6. Reviewer of papers for *IEEE Journal of Lightwave Technology*.

7. Reviewer of papers for *Journal of Vacuum Science*.

8. Reviewer of papers for *IEEE Electron Device Letters*.

9. Reviewer of papers for *IEE Electronics Letters*.

2 Campus Contributions

Campus Wide Committees

1. Member of the Georgia Tech Olympic Task Force Committee 1991.

2. Chair of Sigma Xi best paper committee, 1992.

3. Chair of Sigma Xi best thesis committee, 1993.

C. Engineering Consulting

3 Cold King Inc., electronic circuit failure analysis for legal case, February to September 1991.

2. ABJ Integration Technologies Inc., analog circuit design. Customers include US Government (3 Phase I Small Business Innovative Research (SBIR) contracts), and Cypress Semiconductor. August 1993 to present.

7 Research Proposals and Grants

Dr. Brooke was awarded $6,633,210 in total funding in his career at Georgia Tech (including only his portion in “center funding” e.g. MURIs, NSF Centers, etc.). Of this amount $5,989,964 was “non center” related funding (“non center” funding numbers include total funding of team projects, but exclude projects with more than 4 co-investigators). He is also a founding participant in the “center funded” NSF-funded Packaging Research Center (having directly received over $400,000 in funding from this center); co-PI on a $1,200,000 NSF equipment grant; a participant in the Aerospace Engineering Intelligent Turbine Engine MURI program (receiving $361,130 in direct support from this program); and a founding member of the Georgia Tech Analog Consortium (GTAC), which has brought in more than $1,000,000 of corporate funds.