Spring 2005 Course Announcement

ECE 269: VLSI System Testing

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Class Times: Tuesday, Thursday 2:50-4:05 PM

This course will examine in depth the theory and practice of fault analysis, test generation, and design for testability for VLSI circuits and systems. Testing tools and systematic design-for-test (DFT) methodologies are necessary to handle design complexity, ensure reliable operation, and achieve short time-to-market. The topics to be covered in the course: fault modeling; fault simulation; test generation algorithms; testability measures; design for testability and scan design; built-in self-test; delay testing; IDDQ testing; memory testing; mixed-signal and analog IC testing; system-on-a-chip test. Grading will be based on homework assignments, two in-class exams, and a term project, which may be either a research survey or a software implementation of a test methodology. Current research issues, including topics suitable for M.S. and Ph.D. research, will also be discussed.


Supplementary reading: A collection of research papers and survey articles from various journals, conference proceedings, and magazines will be distributed by the instructor.

Prerequisites: Senior/graduate standing, course in logic design

Desirable: Some exposure to full-custom VLSI design, an introductory course in computer organization, basic knowledge of design and analysis of algorithms, and basic programming skills.

For an overview of the VLSI Testing field and the academic and professional community associated with it, please look up the IEEE Test Technology Technical Council (TTTC) website at www.computer.org/tttc.