**ECE 261: CMOS VLSI Design Methodologies**

Fall 2005

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Homework 3

Assigned: November 2, 2005, Due: November 17, 2005 (start of class)

**Instructions:** You are required to work on the homework on your own. Please be legible and state all assumptions clearly. Show all work in order to receive partial credit.

**Problem 1**

(a) [Thoughts on power supply voltage] What limits the power supply ($V_{DD}$) voltage level in a given CMOS technology (i.e. how low can you set it and how high can you set it)? Explain what you would expect the effect of these two extremes to be? Suggest situations where both of these extremes might be of use. Hint: think in terms of basic device physics and transistor equations.

(b) [Static logic design] Textbook problem 6.4 (Page 379).

[5 + 10 = 15]

**Problem 2**

[Skewed and asymmetric gates] (a) Textbook Problem 6.10, Page 379 (b) Textbook Problem 6.12, Page 379.

[8 + 7 = 15]

**Problem 3**

[Domino logic] (i) Explain how charge sharing can be prevented in domino CMOS.

(ii) Design a domino gate implementing the function $f_1 = A \oplus B$.

(iii) A possible modification of domino logic is to have multiple outputs from a single gate. Modify the domino gate of part (b) above to implement two additional functions $f_2 = A \oplus B \oplus C$ and $f_3 = A \oplus B \oplus C \oplus D$. Assume that complemented inputs are available and they do not come from dynamic gates.

(d) The practicality of this approach for designing multiple-output domino gates is a matter of debate in industry. Comment on the advantages and disadvantages of this approach. [4+4+4+3 = 15]
Problem 4 [Design of Forks] A fork consists of two strings of inverters that share a common input. The figure below shows a 2-1 fork and a 2-3 fork.

Design a 2-3 fork with capacitance $C_{in} = 10$ and total outputs capacitance $C_{out} = 200$. What is the total delay of the fork (in terms of an FO4 inverter)? Compare this delay to that for a 2-1 fork (Exam I problem). What can you say about optimal fork design?