Instructions: You are required to work on the homework on your own. Please be legible and state all assumptions clearly. Show all work in order to receive partial credit.

Problem 1 (a) [Thoughts on power supply voltage] What limits the power supply \( V_{DD} \) voltage level in a given CMOS technology (i.e. how low can you set it and how high can you set it)? Explain what you would expect the effect of these two extremes to be? Suggest situations where both of these extremes might be of use. Hint: think in terms of basic device physics and transistor equations.

(b) [Static logic design] Textbook problem 6.4 (Page 379).

Problem 2 [Skewed and asymmetric gates] (a) Textbook Problem 6.10, Page 379 (b) Textbook Problem 6.12, Page 379.

Problem 3 [Domino logic] (i) Explain how charge sharing can be prevented in domino CMOS.

(ii) Design a domino gate implementing the function \( f_1 = A \oplus B \).

(iii) A possible modification of domino logic is to have multiple outputs from a single gate. Modify the domino gate of part (b) above to implement two additional functions \( f_2 = A \oplus B \oplus C \) and \( f_3 = A \oplus B \oplus C \oplus D \). Assume that complemented inputs are available and they do not come from dynamic gates.

(iv) The practicality of this approach for designing multiple-output domino gates is a matter of debate in industry. Comment on the advantages and disadvantages of this approach. [4+4+4+3 = 15]
Problem 4 [More on Domino CMOS]: The figure below shows a dynamic circuit in Domino CMOS.

(i) What Boolean functions are implemented at outputs $F$ and $G$? If $A$ and $B$ are interpreted as two-bit binary words, $A = A_1A_0$ and $B = B_1B_0$, then what interpretation can be applied to output $G$?

(ii) Describe in at most 2-3 sentences the phenomenon of charge sharing in dynamic CMOS. Which gate (1 or 2) for the circuit below is more likely to suffer from harmful charge sharing? Explain why.

[7 + 8 = 15]