Instructions: You are required to work on the homework on your own. Please be legible and state all assumptions clearly. Show all work in order to receive partial credit.

Problem 1 (a) [CMOS transmission gates]: Prove that any boolean function $f(x_1, x_2, \ldots, x_n)$ can be implemented in VLSI using $2^{n+1} - 2$ CMOS transmission gates and $n$ inverters. Assume that the constant inputs 0 and 1 are available.

(b) [Cell minimization] Determine the optimal ordering of gate inputs (polysilicon lines) in a width-minimized CMOS cell for the transistor circuit shown below. Draw a stick diagram for the optimized cell. [10 + 15 = 25]

Problem 2 [Logical Effort]:
(a) Textbook, Page 266, Problem 4.6
(b) Textbook, Page 269, Problem 4.20
(b) Textbook, Page 269, Problem 4.26. For both parts, you need to read the previous question in the textbook. [8 + 8 + 7 = 25]

Problem 3 [Transistor resizing] For this problem, use the circuit of Problem 3(a) in Homework 1. Note that in the pull-up circuit, there are four pull-up paths to $V_{DD}$. Assuming that all the pMOS transistors in it are of minimum size ($W = 3\lambda$, $L = 2\lambda$), determine if it is possible to resize the pMOS transistors to make all the pull-up times equal. If it is indeed possible, determine the sizes of the transistors; otherwise, prove rigorously that it is not possible to achieve equal pull-up times. [10]