Instructions: You are required to work on the homework on your own. Please be legible and state all assumptions clearly. Show all work in order to receive partial credit.

Problem 1: Sketch the transistor-level schematic of a CMOS 3-input XOR gate. Assume that the inputs are available in both the complemented and uncomplemented forms. Your design must consist of only a single stage of logic.

Problem 2: A 3-input majority gate returns a true output if at least two of its inputs are true. A minority gate is its complement. Sketch a transistor-level schematic of a 3-input minority logic gate using a single-stage of logic.

Problem 3: Design a pull-down circuit corresponding to the pull-up circuit shown below for implementing the function $f$.

Problem 4: Textbook, Page 108, Problem 2.2 (b) Textbook, Page 109, Problem 2.8 (c) Textbook, Page 111, Problem 2.22.