CMOS Testing-2

- Design and test
- Design for testability (DFT)
  - Scan design
- Built-in self-test
- IDDQ testing

Design and Test Flow: Old View

- Test is merely an afterthought

Diagram:
- Specification
- Design
- Fabrication
- Testing
- Synthesis, full-custom simulation, verification, test generation
- Design errors
- Random defects
- Pass
- Fail
- Accept
- Reject
**Design and Test Flow: New View**

Design and test are tightly coupled

- **Specification**
- **Design for testability**
- **Design improvements**
- **Fabrication**
- **Process improvements**
- **Testing**
- **Diagnosis**

- **Design errors**
- **Random defects**

- **Pass**
- **Fail**
- **Accept**
- **Reject**

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**Testing Sequential Circuits**

Difficult problem—internal states cannot be directly controlled and observed
Long test sequences are necessary
Solution: Scan design—simplify to combinational circuit testing

- **Combinational logic**
- **Primary inputs (controllable)**
- **Primary outputs (observable)**
- **State inputs (not controllable)**
- **State outputs (not observable)**

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**Scan Design**

Make all flip-flops directly controllable and observable by adding multiplexers.

Popular design-for-test (DFT) technique-circuit is now combinational for testing purposes.

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**Scan Cell Design**

Data (Functional) → D → Q

Scan in (Test data) → Scan in

N/T = 1: Test mode

N/T = 0: Normal mode

4-bit scan register
**Scan Design**
- Separate input and output 4-bit scan registers
- Test sequence: \{01100, 11011\}, first 4 bits are for flip-flops

**Steps in Scan Testing**
- \(\overline{N}/T = 1\): Scan in test pattern, hold appropriate bit pattern on controllable primary inputs
- \(N/T = 0\): Apply test pattern to combinational circuit
- \(N/T=1\): Scan out test responses
- Scan provides complete controllability and observability
- Testing time? How many cycles? How to test scan registers?
Long Scan Chains

Test vectors need to be translated to scan format

Built-in Self Testing (BIST)

On-chip test generator and response monitor
**BIST: Advantages**

- Lower cost due to elimination of external tester
  - Sematech’s projection: 500 MHz tester (400 pins) will cost $50M in 2010, 90% of on-chip testing will be done using BIST
- In-system, at-system, high-quality testing
- Faster fault detection, ease of diagnosis
- Overcomes pin limitations and related interfacing problems
- Reduces maintenance and repair costs at system level

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**BIST: Issues**

Test strategy (random, exhaustive, deterministic)
Circuit partitioning
Test pattern generation
  - Exhaustive: counters
  - Random: Linear-feedback shift registers (LFSRs)
  - Deterministic: ROM, other methods?
Response analysis
Test control and scheduling
**BIST Logic Circuits**

- Linear-feedback shift-register (LFSR)

![LFSR Diagram]

- Multiple-input signature register (MISR)

![MISR Diagram]

**BIST in Industry**

AT&T (Lucent) has incorporated BIST in hundreds of commercial chips

Intel: 80386, Pentium, Pentium Pro

Hardware overhead typically 15% of self-tested portion (around 5% for entire chip, e.g. 6% for the Pentium Pro)

Regular embedded arrays (RAMs, PLAs) almost always tested using BIST: DEC Alpha, PowerPC

BIST for irregular logic not so widespread
### IDDQ Testing

- Based on current measurements, not voltage
  - IDDQ = $I_{DD}$ quiescent
- In CMOS technology, quiescent current is very low
- Testing idea: check for faults by detecting current spikes
  - Advantage: Massive observability, good for detecting shorts
  - Disadvantage: slow, leakage current closer to quiescent current for deep submicron