Sequential Circuit Design: Part 2

- C²MOS Latch
- Two-phase clock generators
- Four-phase clocking
- Pipelining and NORA-CMOS
- TSPC logic

C²MOS Logic

- Goal: Make circuit operation independent of phase overlap
- No need to worry about careful design of clock phases, clock inversions, etc
- Really ingenious design!
Flip-flop insensitive to clock overlap

C2MOS master-slave negative edge-triggered D flip-flop

- **Insensitive to clock overlap as long as clock rise and fall times are “small”**

**Modes of operation:**
1) Evaluate ($\Phi = 1$)  
   - $\Phi$-section acts as inverter  
   - $\Phi$-section is in high-impedance (hold) mode
2) Roles reversed for $\Phi = 0$

C2MOS avoids Race Conditions

Signal propagation requires pull-up followed by pull-down, or vice versa

- (1-1) overlap: Only pull-down networks are enabled
- (0-0) overlap: Only pull-up networks are enabled
C$^2$MOS avoids Race Conditions

Caution: If clock has low rise/fall times, then both pMOS and nMOS may conduct

Typically need rise/fall time at most five times clock propagation delay

Pipelining

- Common in high-speed designs
- Combinational logic (stages) separated by registers
- Alternating clock phases typically used
- Race may occur if clock phases overlap
Pipelined Logic using C^2MOS

What are the constraints on F and G?

Example

Number of static inversions should be even
NORA CMOS

- Targets implementation of fast, pipelined datapaths using dynamic logic
- Combines C\textsuperscript{2}MOS pipeline registers and np-CMOS dynamic logic functional blocks
  - Combinational logic can be a mixture of static and dynamic logic
  - Latch and logic (feeding latch) are clocked in such a way that both are simultaneously in either evaluation or hold (precharge)
  - Block in evaluation during $\Phi=1$ is a $\Phi$-module, inverse is a $\Phi$-module
  - $\Phi$-modules and $\Phi$-modules alternate

NORA CMOS Modules
NORA Logic Modules

Operation Modes

<table>
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<th>Φ-block</th>
<th>Φ-block</th>
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<tr>
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<td>Latch</td>
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<tr>
<td>Φ = 0</td>
<td>Precharge</td>
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<tr>
<td>Φ = 1</td>
<td>Evaluate</td>
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Doubled C²MOS Latches

- Single clock (no inverse clock is sufficient)
- Requires redesign of C²MOS latch
Doubled C²MOS Latches

Doubled n-C²MOS latch

Doubled p-C²MOS latch

$\Phi = 1$, latch in transparent, evaluate mode

$\Phi = 0$, latch in hold mode, only pull-up network active

Dual-stage approach: no races

Doubled C²MOS Latches: Advantages

• No even-inversion constraints between two latches, or between latch and a dynamic block
• Dynamic and static circuits can be mixed freely
• Logic functions can be included in the n-C²MOS or p-C²MOS latches, or placed between them
• Disadvantage: More transistors per latch (six, instead of four)
TSPC - True Single Phase Clock Logic

Including logic into the latch

Inserting logic between latches

Simplified TSPC Latch (Split-Output)

- Reduced area
- Voltage degradation at A
Master-Slave Flip-flops

(a) Positive edge-triggered D flip-flop
(b) Negative edge-triggered D flip-flop
(c) Positive edge-triggered D flip-flop using split-output latches

Two-Phase Clock Generator

- Considerations:
  - Drive: added buffers
  - Non-overlap: Two phases inverted with respect to each other
  - Minimum skew
  - Implement with NAND gates?
Registers with Load/Enable Inputs

Multiplexed input

Gated clock

Clock enable circuit
Comments on Transmission Gates
(Common Misconceptions)

Transmitting gate used here as an AND gate

\[ F = ab \]

Transmission gate is not an AND gate

\[ F \neq a \cdot b \]

Transmission gate network does not serve as an OR gate

\[ F \neq a + b \]
Four-Phase Clocking

1) $\Phi_1 = 0$, $n_1$ precharges
2) $\Phi_2 = 1$ and $\Phi_1 = 1$, $n_1$ conditionally discharges
3) $\Phi_3 = 0$, value held on $n_1$ regardless of $D$
4) $\Phi_4 = 1$, $\Phi_3 = 1$, $Q$ is conditionally discharges according to the state of $n_1$

Charge sharing: $(n1,inv1)$, $(Q,inv2)$

Four-Phase Clocking: Solving Charge Sharing Problems

"Four" clock phases

"Four" clock phases