Sequential Circuit Design: Part 1

- Design of memory elements
  - Static latches
  - Pseudo-static latches
  - Dynamic latches
- Timing parameters
- Two-phase clocking
- Clocked inverters

Sequential Logic

2 storage mechanisms
- positive feedback
- charge-based
Flip-Flop: Timing Definitions

Maximum Clock Frequency

\[ t_{pFF} + t_{p\text{comb}} + t_{\text{setup}} + T \]
Design of Memory Elements

Positive edge-triggered D flip-flop
Why use inverters on outputs?
Skew Problem: \( \Phi \) may be delayed with respect to \( \Phi \) (both may be 1 at the same time)
This is what happens-

Eliminating/Reducing skew:
Transmission gate acts a buffer, should have same delay as inverter

Latch design

Static D latch

"Jamb" latch

Weak inverter
Dynamic Latches

- So far, all latches have been static-store state when clock is stopped but power is maintained
- Dynamic latches reduce transistor count
- Eliminate feedback inverter and transmission gate
- Latch value stored on the capacitance of the input (gate capacitance)
Dynamic Latch and Flip-Flop

- Difficult to ensure reliable operation
- Similar to DRAM
- Refresh cycles are required

Charge-Based Storage

Pseudo-static Latch
Overlap Clocks Can Cause
• Race Conditions
• Undefined Signals

To reduce skew: generate complement of clock within the cell
Extra inverter per cell

Master-Slave Flip-Flop

Two-Phase Clocking

• Inverting a single clock can lead to skew problems
• Employ two non-overlapping clocks for master and slave sections of a flip-flop
• Also, use two phases for alternating pipeline stages
Two-Phase Clocking

\[ \Phi_1(t) \cdot \Phi_2(t) = 0 \]

\[ \Phi_1 = 1, \Phi_2 = 0 \]

\[ \Phi_1 = 0, \Phi_2 = 1 \]

Important: Non-overlap time \( t \) must be kept small

2-phase non-overlapping clocks

Pseudo-static D flip-flop

Important: Non-overlap time \( t \) must be kept small

Krish Chakrabarty
2-phase dynamic flip-flop

Use of “p” Leakers

Flip-flop based on nMOS pass gates

Degraded voltage $V_{DD}-V_t$

No need to route $\Phi$ signals

Problem: Increased delay (extra inverter)

pMOS leaker transistors provide full-restored logic levels
Clocked Inverters

Similar to tristate buffer

\[ \Phi = 1, \text{ acts as inverter} \]

\[ \Phi = 0, \text{ output } = Z \]

D Latch

Flip-flop insensitive to clock overlap

C\textsuperscript{2}MOS LATCH
C\textsuperscript{2}MOS avoids Race Conditions

\begin{figure}
\centering
\includegraphics[width=0.8\textwidth]{c2mos.pdf}
\caption{(a) (1-1) overlap (b) (0-0) overlap}
\end{figure}