Dynamic Logic

2 phase operation:
• Precharge
• Evaluation

• N+2 transistors for N-input function
  – Better than 2N transistors for complementary static CMOS
  – Comparable to N+1 for ratio-ed logic
• No static power dissipation
  – Better than ratio-ed logic
• Careful design, clock signal $\Phi$ needed
Dynamic Logic: Principles

- **Precharge**
  \( \Phi = 0 \), \( Out \) is precharged to \( V_{DD} \) by \( M_p \).
  \( M_e \) is turned off, no dc current flows (regardless of input values)

- **Evaluation**
  \( \Phi = 1 \), \( M_e \) is turned on, \( M_p \) is turned off.
  Output is pulled down to zero depending on the values on the inputs. If not, precharged value remains on \( C_L \).

Important: Once \( Out \) is discharged, it cannot be charged again!
Gate input can make only one transition during evaluation

- Minimum clock frequency must be maintained
- Can \( M_e \) be eliminated?
Dynamic 4 Input NAND Gate

Reliability Problems — Charge Leakage

(1) Leakage through reverse-biased diode of the diffusion area
(2) Subthreshold current from drain to source

Minimum Clock Frequency: > 1 MHz
**Charge Sharing (redistribution)**

- Assume: during precharge, A and B are 0, \( C_a \) is discharged
- During evaluation, B remains 0 and A rises to 1
- Charge stored on \( C_L \) is now redistributed over \( C_L \) and \( C_a \)

\[
C_L V_{DD} = C_L V_{out}(t) + C_a V_X
\]

\[
V_X = V_{DD} - V_t, \text{ therefore } \delta V_{out}(t) = V_{out}(t) - V_{DD} = \frac{C_a}{C_L} (V_{DD} - V_t)
\]

Desirable to keep the voltage drop below threshold of pMOS transistor (why?) \( \Rightarrow C_a/C_L < 0.2 \)

**Charge Redistribution - Solutions**

1. **Static bleeder**
   - (a) Static bleeder

2. **Precharge of internal nodes**
   - (b) Precharge of internal nodes
Cascading Dynamic Gates

Internal nodes can only make 0-1 transitions during evaluation period

Domino Logic

Static inverters between dynamic stages

Static Inverter with Level Restorer
Domino Logic - Characteristics

- Only non-inverting logic
- Very fast - Only 1-0 transitions at input of inverter
  - Precharging makes pull-up very fast
  - Adding level restorer reduces leakage and charge redistribution problems
- Optimize inverter for fan-out

np-CMOS (Zipper CMOS)

- Only 1-0 transitions allowed at inputs of PUN
- Used a lot in the Alpha design
### np CMOS Adder

![np CMOS Adder Diagram]

### CMOS Circuit Styles - Summary

<table>
<thead>
<tr>
<th>Style</th>
<th>Ratioed</th>
<th>Static Power</th>
<th># transistors</th>
<th>Area (μm²)</th>
<th>Propagation Delay (nsec)</th>
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<tr>
<td>Complementary</td>
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<td>8</td>
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<td>Pseudo-NMOS</td>
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*4-input NAND Gate*