Dynamic Combinational Circuits

- Dynamic circuits
  - Charge sharing, charge redistribution
- Domino logic
- np-CMOS (zipper CMOS)

Dynamic Logic

- *Dynamic* gates use a clocked pMOS pullup
- Two modes: *precharge* and *evaluate*

![Dynamic Logic Diagram](image-url)
Dynamic Logic

2 phase operation:
- Precharge
- Evaluation

Logical Effort

Inverter

NAND2

NOR2

unfooted

foothed

Krish Chakrabarty
Dynamic Logic

- N+2 transistors for N-input function
  - Better than 2N transistors for complementary static CMOS
  - Comparable to N+1 for ratio-ed logic
- No static power dissipation
  - Better than ratio-ed logic
- Careful design, clock signal \( \Phi \) needed

Dynamic Logic: Principles

- Precharge
  \( \Phi = 0, \text{Out is precharged to } V_{DD} \) by \( M_p \).
  \( M_e \) is turned off, no dc current flows (regardless of input values)
- Evaluation
  \( \Phi = 1, M_e \) is turned on, \( M_p \) is turned off.
  Output is pulled down to zero depending on the values on the inputs. If not, precharged value remains on \( C_L \).

Important: Once Out is discharged, it cannot be charged again!
Gate input can make only one transition during evaluation

- Minimum clock frequency must be maintained
- Can \( M_e \) be eliminated?
The Foot

• What if pulldown network is ON during precharge?
• Use series evaluation transistor to prevent fight.

Example

\[
\begin{align*}
V_{DD} & \\
\Phi & M_p & \text{Out} \\
A & C & \text{• Ratioless} \\
B & \text{• No Static Power Consumption} \\
\Phi & M_e & \text{• Noise Margins small (NM)} \\
& & \text{• Requires Clock}
\end{align*}
\]
Dynamic 4 Input NAND Gate

Cascading Dynamic Gates
**Monotonicity**

- Dynamic gates require *monotonically rising* inputs during evaluation
  - 0 -> 0
  - 0 -> 1
  - 1 -> 1
  - But not 1 -> 0

- Monotonicity Woes
  - But dynamic gates produce monotonically falling outputs during evaluation
  - Illegal for one dynamic gate to drive another!
Reliability Problems — Charge Leakage

(a) Leakage sources

1. Leakage through reverse-biased diode of the diffusion area
2. Subthreshold current from drain to source

(b) Effect on waveforms

A = 0

Leakage

- Dynamic node floats high during evaluation
  - Transistors are leaky (\( I_{OFF} \neq 0 \))
  - Dynamic value will leak away over time
  - Formerly miliseconds, now nanoseconds!
- Use keeper to hold dynamic node
  - Must be weak enough not to fight evaluation
Charge Sharing (redistribution)

- Assume: during precharge, A and B are 0, $C_a$ is discharged
- During evaluation, B remains 0 and A rises to 1
- Charge stored on $C_L$ is now redistributed over $C_L$ and $C_a$

\[ C_L V_{DD} = C_L V_{out}(t) + C_a V_X \]

\[ V_X = V_{DD} - V_t, \text{ therefore} \]
\[ \delta V_{out}(t) = V_{out}(t) - V_{DD} = -\frac{C_a}{C_L} (V_{DD} - V_t) \]

Desirable to keep the voltage drop below threshold of pMOS transistor (why?) \( \Rightarrow \frac{C_a}{C_L} < 0.2 \)

Charge Sharing

- Dynamic gates suffer from charge sharing

\[ V_x = V_y = \frac{C_Y}{C_x + C_Y} V_{DD} \]
Charge Redistribution - Solutions

(a) Static bleeder

(b) Precharge of internal nodes

Secondary Precharge

- Solution: add secondary precharge transistors
  - Typically need to precharge every other node
- Big load capacitance $C_Y$ helps as well
**Domino Logic**

![Diagram of Domino Logic]

**Domino Gates**

- Follow dynamic stage with inverting static gate
  - Dynamic / static pair is called domino gate
  - Produces monotonic outputs
Domino Logic - Characteristics

• Only non-inverting logic
• Very fast - Only 1->0 transitions at input of inverter
  • Precharging makes pull-up very fast
• Adding level restorer reduces leakage and charge redistribution problems
• Optimize inverter for fan-out

Domino Optimizations

• Each domino gate triggers next one, like a string of dominos toppling over
• Gates evaluate sequentially but precharge in parallel
• Thus evaluation is more critical than precharge
• HI-skewed static stages can perform logic (fast rising output)

- Compound domino
- 8-input domino mux
- HI-skew static NAND gate
**Dual-Rail Domino**

- Domino only performs noninverting functions:
  - AND, OR but not NAND, NOR, or XOR
- Dual-rail domino solves this problem
  - Takes true and complementary inputs
  - Produces true and complementary outputs

<table>
<thead>
<tr>
<th>sig_h</th>
<th>sig_l</th>
<th>Meaning</th>
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<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Precharged</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>‘0’</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>‘1’</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>invalid</td>
</tr>
</tbody>
</table>

**Example: AND/NAND**

- Given $A_h, A_l, B_h, B_l$
- Compute $Y_h = A \times B$, $Y_l = \sim(A \times B)$
- Pulldown networks are conduction complements
Example: XOR/XNOR

• Sometimes possible to share transistors

\[ Y_L = A \text{ xor } B \]
\[ Y_H = A \text{ xor } B \]

Noise Sensitivity

• Dynamic gates are very sensitive to noise
  – Inputs: \( V_{\text{IH}} \approx V_{\text{IN}} \)
  – Outputs: floating output susceptible to noise noise

• Noise sources
  – Capacitive crosstalk
  – Charge sharing
  – Power supply noise
  – Feed-through noise
  – And more!
Power

• Domino gates have high activity factors
  – Output evaluates and precharges
    • If output probability = 0.5, $\alpha = 0.5$
      – Output rises and falls on half the cycles
    – Clocked transistors have $\alpha = 1$
  • Leads to very high power consumption

Pass Transistor Circuits

• Use pass transistors like switches to do logic
• Inputs drive diffusion terminals as well as gates

• CMOS + Transmission Gates:
  – 2-input multiplexer
  – Gates should be restoring
LEAP

- LEAn integration with Pass transistors
- Get rid of pMOS transistors
  - Use weak pMOS feedback to pull fully high
  - Ratio constraint

Domino Summary

- Domino logic is attractive for high-speed circuits
  - 1.5 – 2x faster than static CMOS
  - But many challenges:
    - Monotonicity
    - Leakage
    - Charge sharing
    - Noise
- Widely used in high-performance microprocessors
CPL

• **Complementary Pass-transistor Logic**
  – Dual-rail form of pass transistor logic
  – Avoids need for ratioed feedback
  – Optional cross-coupling for rail-to-rail swing

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Pass Transistor Summary

• Researchers investigated pass transistor logic for general purpose applications in the 1990’s
  – Benefits over static CMOS were small or negative
  – No longer generally used
• However, pass transistors still have a niche in special circuits such as memories where they offer small size and the threshold drops can be managed
np-CMOS (Zipper CMOS)

- Only 1-0 transitions allowed at inputs of PUN
- Used a lot in the Alpha design

np CMOS Adder

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# CMOS Circuit Styles - Summary

<table>
<thead>
<tr>
<th>Style</th>
<th>Ratioed</th>
<th>Static Power</th>
<th># transistors</th>
<th>Area ($\mu$m$^2$)</th>
<th>Propagation Delay (nsec)</th>
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<tbody>
<tr>
<td>Complementary</td>
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<td>Pseudo-NMOS</td>
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<td>Dynamic (NP)</td>
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<td>No</td>
<td>6</td>
<td>212</td>
<td>0.37</td>
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*4-input NAND Gate*