MOS Transistor Theory

- So far, we have viewed a MOS transistor as an ideal switch (digital operation)
  - Reality: less than ideal

MOS Transistor Theory

- Study conducting channel between source and drain
  - Modulated by voltage applied to the gate (voltage-controlled device)
  - nMOS transistor: majority carriers are electrons (greater mobility), p-substrate doped (positively doped)
  - pMOS transistor: majority carriers are holes (less mobility), n-substrate (negatively doped)
**Gate Biasing**

- $V_{gs}=0$: no current flows from source to drain (insulated by two reverse biased pn junctions)
- $V_{gs}>0$: electric field created across substrate
- Electrons accumulate under gate: region changes from p-type to n-type
- Conduction path between source and drain

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**nMOS Device Behavior**

- $V_{gs}<<V_{t}$: Accumulation mode
  - Enhancement-mode transistor: Conducts when gate bias $V_{gs}>V_{t}$
- $V_{gs}=V_{t}$: Depletion mode
  - Depletion-mode transistor: Conducts when gate bias is zero
- $V_{gs}>V_{t}$: Inversion mode
  - Depletion region (n-type)
Transistor Operating Regions

- Cut-off region: accumulation mode, zero current flow
- Linear region: \( V_{ds} \leq V_{gs} - V_t \), weak inversion layer, drain current depends on \( V_{gs} \) and \( V_{ds} \)
- Saturated region: \( V_{ds} > V_{gs} - V_t \), strong inversion layer, drain current independent of \( V_{ds} \)

Threshold Voltage: Concept
Current-Voltage Relations

MOS transistor and its bias conditions

Current-Voltage Relations

Linear Region: \( V_{DS} \leq V_{GS} - V_T \)

\[
I_D = \kappa' \frac{W}{L} (V_{GS} - V_T)(V_{DS} - \frac{V_{DS}^2}{2})
\]

with

\[
\kappa' = \mu_n C_{ox} = \frac{\mu_n \kappa_{ox}}{\kappa_{ox}} \quad \text{Process Transconductance Parameter}
\]

Saturation Mode: \( V_{DS} \geq V_{GS} - V_T \)

Channel Length Modulation

\[
I_D = \kappa' \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})
\]
Current-Voltage Relations

\[ k'_n : \text{transconductance of transistor} \]
\[ \frac{W}{L} : \text{width-to-length ratio} \]

- As \( W \) increases, more carriers available to conduct current
- As \( L \) increases, \( V_{ds} \) diminishes in effect (more voltage drop). Takes longer to push carriers across the transistor, reducing current flow

Typical Parameter Values

<table>
<thead>
<tr>
<th></th>
<th>( k'_n )</th>
<th>( V_t )</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-type</td>
<td>24 microA/V^2</td>
<td>0.8V</td>
</tr>
<tr>
<td>p-type</td>
<td>9 microA/V^2</td>
<td>-0.8V</td>
</tr>
</tbody>
</table>

Why is \( k'_n \) higher for n-type transistors?
Transistor in Saturation

The Gate Capacitance

\[ C_{\text{gate}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \pi W L \]
**Diffusion Capacitance**

$$C_{\text{diff}} = C_{\text{bottom}} + C_{\text{sw}} = C_j \times \text{AREA} + C_{j\text{SW}} \times \text{PERIMETER}$$

$$= C_j L_g W + C_{j\text{SW}} (2 L_g + W)$$

**Parasitic Resistances**

$$R_S = \frac{L_S}{W} R_\alpha + R_C$$

$$R_D = \frac{L_D}{W} R_\alpha + R_C$$

$R_C$: contact resistance

$R_\alpha$: sheet resistance per square of drain-source diffusion
Body Effect

- Many MOS devices on a common substrate
  - Substrate voltage of all devices are normally equal
- But several devices may be connected in series
  - Increase in source-to-substrate voltage as we proceed vertically along the chain

\[
\begin{align*}
V_{s1} &= 0 \\
V_{s2} &\neq 0
\end{align*}
\]

\[
V_{t2} > V_{t1}
\]

• Net effect: slight increase in threshold voltage \( V_t \)
  \( V_{t2} > V_{t1} \)