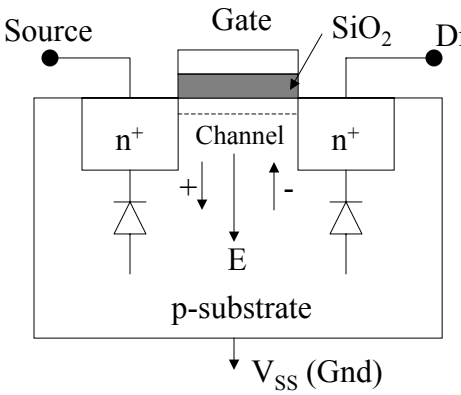
MOS Transistor Theory

- So far, we have viewed a MOS transistor as an ideal switch (digital operation)
  - Reality: less than ideal

MOS Transistor Theory

- Study conducting channel between source and drain
  - Modulated by voltage applied to the gate (voltage-controlled device)
  - nMOS transistor: majority carriers are electrons (greater mobility), p-substrate doped (positively doped)
  - pMOS transistor: majority carriers are holes (less mobility), n-substrate (negatively doped)

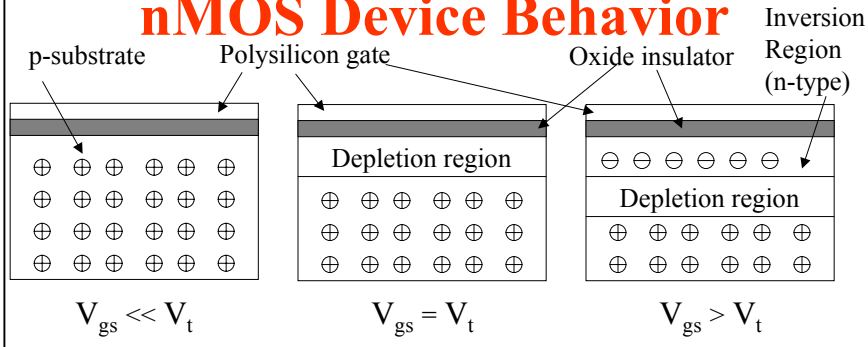
Gate Biasing



- V_{gs}=0: no current flows from source to drain (insulated by two reverse biased pn junctions
- V_{gs}>0: electric field created across substrate

- Electrons accumulate under gate: region changes from p-type to n-type
- Conduction path between source and drain

nMOS Device Behavior



$V_{gs} << V_t$ Accumulation mode

$V_{gs} = V_t$ Depletion mode

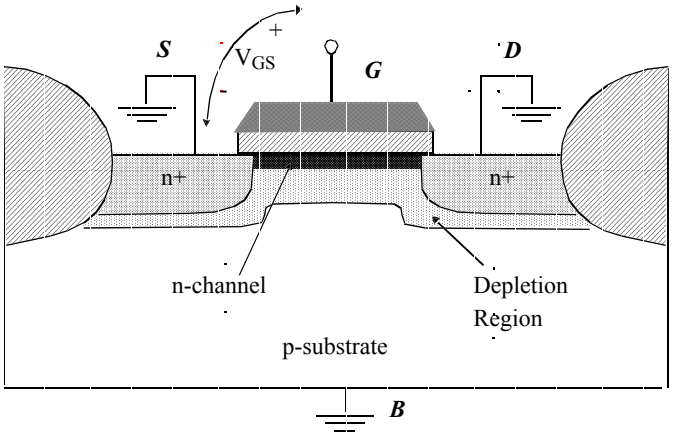
$V_{gs} > V_t$ Inversion mode

- Enhancement-mode transistor: Conducts when gate bias $V_{gs} > V_t$
- Depletion-mode transistor: Conducts when gate bias is zero

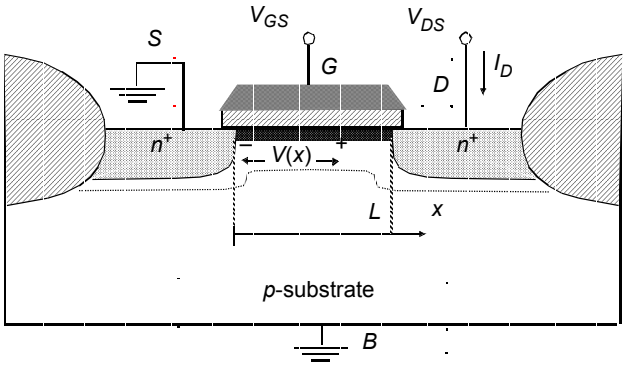
Transistor Operating Regions

- Cut-off region: accumulation mode, zero current flow
- Linear region: $V_{ds} <= V_{gs}-V_t$, weak inversion layer, drain current depends on V_{gs} and V_{ds}
- Saturated region: $V_{ds} > V_{gs}-V_t$, strong inversion layer, drain current independent of V_{ds}

Threshold Voltage: Concept



Current-Voltage Relations



MOS transistor and its bias conditions

Current-Voltage Relations

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

Current-Voltage Relations

k'_n: transconductance of transistor

$\frac{W}{L}$: width-to-length ratio

• As W increases, more carriers available to conduct current

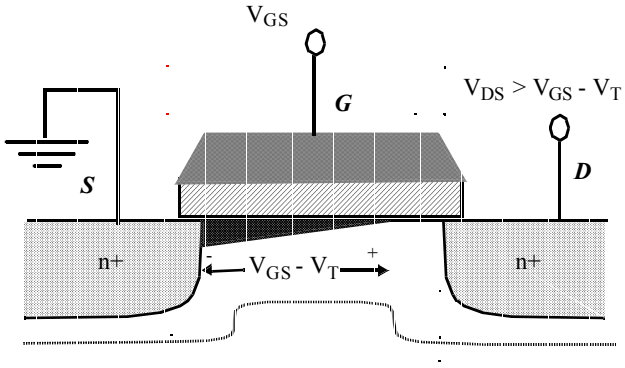
• As L increases, V_{ds} diminishes in effect (more voltage drop). Takes longer to push carriers across the transistor, reducing current flow

Typical Parameter Values

	k'	V_t
n-type	24 microA/V^2	0.8V
p-type	9 microA/V^2	-0.8V

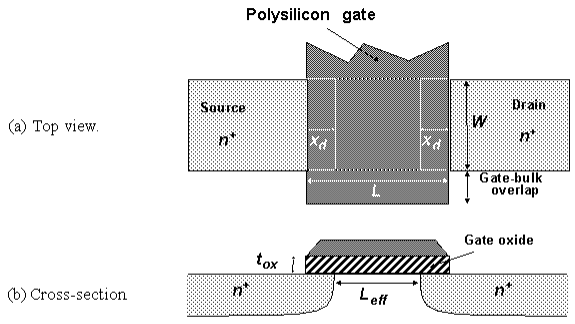
Why is k' higher for n-type transistors?

Transistor in Saturation



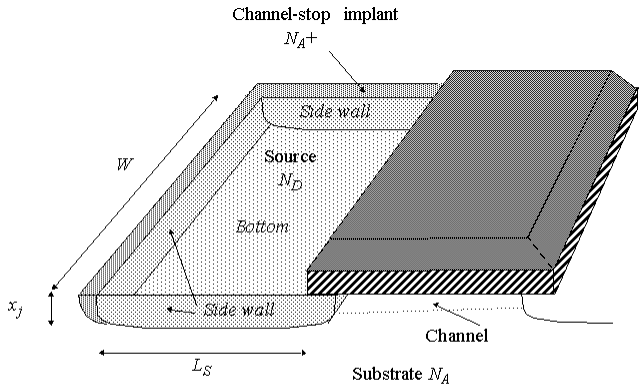
Channel is pinched off

The Gate Capacitance



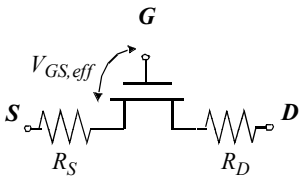
$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

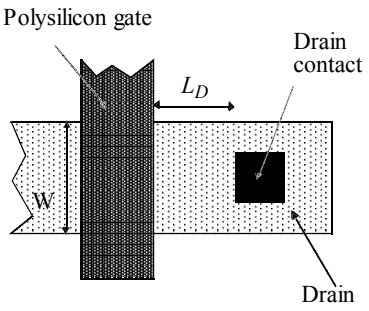
Diffusion Capacitance



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

Parasitic Resistances





$R_S = (L_S/W)R_{\square} + R_C$

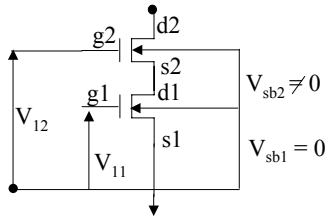
$R_D = (L_D/W)R_{\square} + R_C$

R_C: contact resistance

$R_{\square}$: sheet resistance per square of drain-source diffusion

Body Effect

- Many MOS devices on a common substrate
  - Substrate voltage of all devices are normally equal
- But several devices may be connected in series
  - Increase in source-to-substrate voltage as we proceed vertically along the chain



- Net effect: slight increase in threshold voltage V_t, $V_{t2}>V_{t1}$