An Overview of Test at IBM Microelectronics

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Agenda

- IBM as a Chip Maker
- Challenges of Test
- Test Methodology
  - Overview
  - LSSD
  - OPMISR
  - OPMISR + Illinois Test
  - Macro Isolation
  - How customers implement test methodology
IBM as a Chip Maker

- IBM has been producing chips for internal consumption since the mid-1960's in support of the IBM System/360 Mainframe
  - Currently – approximately 20% internal use / 80% for others
- OEM ASICs vendor since mid 1990's
  - Currently releasing 100-150 designs / year
  - Focus Areas:
    - Networking
    - Consumer Products
      - Digital Cameras
      - Video Games
  - OEM business provides economies of scale to support fabs and development for internal consumption

IBM as a Chip Maker

- Fabs
  - East Fishkill, New York
    - State of the art 300 mm wafer facility
      - 130 nm, 90 nm, 65 nm, 45 nm (planned)
  - Burlington, Vermont
    - Previous Generation 200 mm wafer facility
      - 250 nm, 180 nm, 130 nm
- Support Engineers
  - Process Development
    - Main lab in East Fishkill, New York
  - Design Support, 5 locations in North America, additional WW locations
  - Approx 500 Engineers World Wide
- Tools
  - Mixture of Internally Developed, Partner and Third Party Tools
IBM as a Chip Maker

- Typical Chip
  - 12 mm x 12 mm (range is from 5 to 18 mm)
  - 5 – 15 million gates
  - 700 I/O Pins (can be as many as 2500)
  - 4 Mbit of SRAM
  - Capability for up to 32 Mbit of DRAM
  - Multiple Types of Hard IP Blocks
    - PLL's, High Speed SERDES (+12 Gbit/Sec), Microprocessors, CAM's

Challenges of Test

- Customers are Very Demanding
  - Few customers will accept more than 1000 bad parts / million shipped
    - Some expect less than 100 / million
  - 99.5 % DC Stuck / 95% Transition Fault Coverage not always good enough
- Chips are getting large and very complex
  - 15 Million Gates is NOT UNUSUAL – 50 million is in sight
  - Mixture of differing type of Mixed Signal and Hard IP
- For 180 nm and less, DC Stuck at Fault testing not totally satisfactory.
  - Must be supplemented by Transition Testing to meet customer expectations
  - At sub 130 nm, demand for At Speed Testing is common
- Test is OVERHEAD
  - Less Test Cost = Greater Profit
    - Minimize Tester Time
    - Leverage Older / Cheaper Testers
Test Methodology

- Full Scan
  - 100% ATPG Based
    - Typically 99.5% DC Stuck at Fault Coverage achieved
      - Mixture of Target Patterns
      - Weighted Random Pattern Testing
    - AC Transition Fault Coverage varies
      - “No Cost Option” – 50-60% coverage is typical
      - “Premium” - 90%+ achievable
- Reduced Pin Count Testing
  - Allows use of Low Cost Testers (current workhorse Advantest 6670)
    - 64 High Speed Channels (->125 MHz)
    - 64 Low Speed Channels (-> 1 KHz)
    - 128 VDD/GND Channels
Test Methodology

- LSSD
  - Level Sensitive Scan Design
    - Developed in late 1960's at IBM
    - First major use of Full Scan Test
  - Race Free on designs with multiple clock domains
  - Supports Structure based ATPG with simple straightforward testers
  - IBM Challenge:
    - Make it trivial to use on most designs
    - Solution IBM / Cadence DFT tool

Test Methodology

- Conventional MUX Scan
  - What happens if Clock #2 is somewhat later than Clock #1 ???
Test Methodology

- Flip Flop Implementation
  - Master Latch
  - Slave Latch
  - Clock Overhead

- LSSD Implementation
  - Independent Test Clocks
  - More Complex Clock Overhead (Clock Splitter)
  - Better Control During Test
  - Shared among several flops
Test Methodology

- Future Mux Scan / LSSD Hybrid
  - More Commonality with Industry
  - Less switching when signals are functional
  - Less Switching during Test
  - Adds new function – Better AC Test
  - Most of LSSD Advantage (Race Free) – Loses Little (Ability of Scan Flush)

Test Methodology

- Problem
  - Scan test time for latest chips takes too long
    - Tester Capacity
    - Tester Operational Cost
    - Tester Time slows production line
  - Solutions
    - Move More data through less pins
      - OPMISR
      - OPMISR + Illinois Test
Test Methodology

- Scan to OPMISR
  - Introduced with 130 nm chips
  - OPMISR = On Product Multiple Input Signature Register
  - Eliminates need for Scan Out pins
  - Doubles number of Scan Chains / Halves Tester Time
  - Signature read out and compared against known good value at end of test cycle

Test Methodology

- Before Scan to OPMISR
  - 6 I/O's
  - 3 Scan Chains
Test Methodology

- After Scan to OPMISR
  - 6 I/O’s
  - 6 Scan Chains

- Illinois Scan + Scan to MISR
  - Introduced in 90 nm technology
  - Observation:
    - High Percentage of bits in Scan Chain are “Don’t Cares”
    - Scan Multiple Scan Chains from one input lining up “Don’t Cares”
Test Methodology

- Illinois Scan + OPMISR
  - Empirical Observations
    - 10:1 Ratio of Scan In is optimal for most designs
    - Normally Yields 6:1 test productivity improvement
  - Negative
    - What happens if inconvenient bits just happen to line up
      - Typically happens in a 20-30 places / chip
    - Solution
      - Supplement with limited amount full scan testing
  - ATPG time increases by 50%
    - Who cares – You only do it once / chip !!!
    - IBM is leading maker of UNIX Server Boxes

Test Methodology

- Hard IP / Mixed Signal
  - Macro Isolation Strategy
    - Selected signals must have path to chip pins
    - Other ports must be controllable or observable via scan latches
Test Methodology

- Implementation
  - I/O Padring compiled to customer spec by tool
  - Customer logic contains
    - Flops + Gates
    - Hard IP wrapped to hide test issues
  - Test Insertion done with DFT Synthesis tool
  - Verification of ATPG Design Rule conformance done by tool
    - Full Scan
    - Macro Isolation
    - I/O Boundary Testing