Design Methodologies

• Design styles
  – Full-custom design
  – Standard-cell design
  – Programmable logic
    • Gate arrays and field-programmable gate arrays (FPGAs)
    • Sea of gates
      – System-on-a-chip (embedded cores)
• Design tools

Full-Custom Design

• Every gate is carefully designed and optimized
  – Hierarchical design may be used, place-and-route tools typically used
• Advantages:
  – High density, ideal for high volumes
  – Performance optimization
• Disadvantages:
  – High design time, cumbersome
• Applications: Datapaths in microprocessors
• High-paying jobs!
Full-Custom Design (Contd.)

- Simple CAD tools suffice
  - Design entry
  - Schematic editor
  - Layout editor
  - DRC, LVS, Spice
- No need for sophisticated synthesis and design partitioning tools

Standard Cell Design

- Use pre-optimized SSI or MSI library cells
  - NAND gates, multiplexers, adder slices, decoders, comparators, RAM, ROM
- Reduces design time
- Lower density and lower performance
- Standardized at the logic or function level

![Pitch-matched cells]

![Routing channel]
Standard Cells (Contd)

- CAD tools needed for partitioning design
- Technology mapping
- Design entry, DRC, LVS, simulations tools needed
- Place and route tools
- Good for moderate volumes, as in ASICs, typically used for non-critical portions of a CPU

Programmable Logic

- Programmable logic blocks
  - PLDs, PALs
  - Fusible links (fuses) blown when current is exceeded
- Programmable interconnects
  - Mask-programmed gate-arrays (MPGAs)
  - Field-programmable gate-arrays (FPGAs)
  - Sea of gates
Programmable Logic

- **PLDs**
  - Wide fan-in, 2-level SOP, optional flip-flops on output
  - Best known: 22V10 with 22 inputs, 10 outputs, from AMD
  - Programmed by users
  - Fusible links

- **MPGAs**
  - Also called gate arrays
  - More dense than PLDs
  - Predesigned transistors with customized wiring
  - Wiring done during manufacture (not user)

FPGAs: complex designs, user programmable

MPGAs vs FPGAs

- **X-axis:** Volume (units)
- **Y-axis:** Number of designs

Graph showing the trend of designs over years with FPGA, MPGAs, and PLDs.
FPGAs

FPGAs

- SRAM-programmed
- Antifuse-programmed channel
- EPROM-programmed array

Analog FPGAs (FPAAs) now commercially available

FPGAs

- Advantages
  - Low design cost (custom masks not needed)
  - Rapid turnaround
  - Low risk
  - Effective design verification
  - Low testing costs-test program same for all designs

- Disadvantages
  - Programming circuitry: area penalty, ten times larger for same gate capacity as MPGA
  - Speed: 2-3 times slower than MPGA
  - Design methodology: “too easy” to use, encourages “try-it-and-see-what-happens” methodology
Programmable Interconnects

• Program the routing

• PLICE: Programmable Low-Impedance Circuit Element, “antifuse”
  – Normally high resistance (> 100MΩ)
  – Antifuse can be permanently changed to a low-resistance (200-500Ω) structure, i.e. form links

• Low gate utilization

• E.g. 32-bit adder using Actel FPGAs:
  – 160 logic modules, 65 ns for addition
  – 3.5 32-bit adders on an FPGA chip

Comments on Gate Utilization for FPGAs

• 32-bit adder using Actel FPGAs:
  – 160 logic modules, 65 ns for addition
  – 3.5 32-bit adders on an FPGA chip
  – Design time: one afternoon, $5-$10 design cost
  – Lot of wasted logic

• 32-bit full-custom adder (1 micron)
  – 1300 adders on one chip, 33 ns addition time
  – Design time: 6 months, $200,000
Actel Logic Cell

- All 2-input functions are realized (select inputs carefully)
- All 3-input functions are realized (if?)
- Which 4-input functions?
- How to implement a latch?

Xilinx FPGAs

- Configurable logic blocks (contain SRAMs), CLBs
- Programmable interconnect
- 500 CLBs on a chip
- 100K bits of RAM per chip
- 32-bit adder example:
  - 62 CLBs, 8 adders per chip
  - Speed: 20-50 MHz
Sea of Gates Design

- Goal: reduce design cost of IC, rapid prototyping, fast turnaround time
  - Not useful for high-volume production (more area per IC)
- Core of chip (base array) contains continuous array of n and p transistors
  - Polysilicon laid a-priori (transistors formed in advance)
- Personalization done by using design-specific metallization and contacts
- Highly automated process: sophisticated CAD tools used

Sea of Gates

Routing possible over unused rows
Sea of Gates

- Design Decisions
  - How many n and p rows per strip?
  - Size and ratio of transistors
  - Number, direction of routing tracks

Embedded Cores

- Complex “off-the-shelf”, optimized, pre-designed circuits: processors, ASICs, memories, controllers
- Used for system-on-a-chip (SOC) designs
- Hot intellectual property (IP)
- IC consists of several embedded cores along with custom-designed blocks