Circuit Pitfalls

On how to avoid bad circuit design!

Outline

• Circuit Pitfalls
  – Detective puzzle
  – Given circuit and symptom, diagnose cause and recommend solution
  – All these pitfalls have caused failures in real chips
• Noise Budgets
• Reliability
Bad Circuit 1

- Circuit
  - 2:1 multiplexer

Principle:

Solution:

- Symptom
  - Mux works when selected D is 0 but not 1.
  - Or fails at low $V_{DD}$.

Bad Circuit 2

- Circuit
  - Latch

Principle:

Solution:

- Symptom
  - Load a 0 into Q
  - Set $\phi = 0$
  - Eventually Q spontaneously flips to 1
Bad Circuit 3

• Circuit
  – Domino AND gate

  \[ \phi \quad 0 \quad 1 \]

  \[ X \quad Y \]

  Principle:

Solution:

• Symptom
  – Precharge gate (Y=0)
  – Then evaluate
  – Eventually Y spontaneously flips to 1

Bad Circuit 4

• Circuit
  – Pseudo-nMOS OR

  \[ \phi \quad X \quad B \quad Y \]

Principle:

Solution:

• Symptom
  – When only one input is true, Y = 0.
**Bad Circuit 5**

- **Circuit**
  - Latch

![Diagram of a latch circuit](image)

- **Symptom**
  - Q stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.

**Principle:**

**Solutions:**

**Bad Circuit 6**

- **Circuit**
  - Domino AND gate

![Diagram of a domino AND gate](image)

- **Symptom**
  - Precharge gate while A = B = 0, so Z = 0
  - Set $\phi = 1$
  - A rises
  - Z is observed to sometimes rise

**Principle:**

**Solutions:**
**Bad Circuit 7**

- Circuit
  - Dynamic gate + latch

Principle:

Solution:

- Symptom
  - Precharge gate while transmission gate latch is opaque
  - Evaluate
  - When latch becomes transparent, X falls

**Bad Circuit 8**

- Circuit
  - Latch

Principle:

Solution:

- Symptom
  - Q changes while latch is opaque
  - Especially if D comes from a far-away driver
Bad Circuit 9

- Circuit
  - Anything

- Symptom
  - Some gates are slower than expected

Principle:

Noise

- Sources
  - Power supply noise / ground bounce
  - Capacitive coupling
  - Charge sharing
  - Leakage
  - Noise feedthrough

- Consequences
  - Increased delay (for noise to settle out)
  - Or incorrect computations
Reliability

- Hard Errors
- Soft Errors

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<table>
<thead>
<tr>
<th>Time</th>
<th>Failure Rate</th>
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<tbody>
<tr>
<td>Infant Mortality</td>
<td></td>
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<tr>
<td>Useful Operating Life</td>
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<tr>
<td>Wear Out</td>
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</tbody>
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Electromigration

- “Electron wind” causes movement of metal atoms along wires
- Excessive electromigration leads to open circuits
  - Most significant for unidirectional (DC) current
    - Depends on current density $J_{dc}$ (current / area)
    - Exponential dependence on temperature $E_kT$
    - Black’s Equation:
      $$MTTF \propto \frac{e^{\frac{E_kT}{J_{dc}n}}}{J_{dc}}$$
    - Typical limits: $J_{dc} < 1–2$ mA / $\mu$m²
Self-Heating

- Current through wire resistance generates heat
  - Oxide surrounding wires is a thermal insulator
  - Heat tends to build up in wires
  - Hotter wires are more resistive, slower
- Self-heating limits AC current densities for reliability

\[ J_{\text{rms}} = \sqrt{\frac{\int \text{heat} \, dt}{T}} \]

- Typical limits: \( J_{\text{rms}} < 15 \text{ mA/\mu m}^2 \)

Hot Carriers

- Electric fields across channel impart high energies to some carriers
  - These “hot” carriers may be blasted into the gate oxide where they become trapped
  - Accumulation of charge in oxide causes shift in \( V_t \) over time
  - Eventually \( V_t \) shifts too far for devices to operate correctly
- Choose \( V_{DD} \) to achieve reasonable product lifetime
  - Worst problems for inverters and NORs with slow input rise time and long propagation delays
Latchup

- Latchup: positive feedback leading to $V_{DD} - GND$ short
  - Major problem for 1970’s CMOS processes before it was well understood
- Avoid by minimizing resistance of body to GND / $V_{DD}$
  - Use plenty of substrate and well taps

Guard Rings

- Latchup risk greatest when diffusion-to-substrate diodes could become forward-biased
- Surround sensitive region with guard ring to collect injected charge
Overvoltage

- High voltages can damage transistors
  - Electrostatic discharge
  - Oxide arcing
  - Punchthrough
  - Time-dependent dielectric breakdown (TDDB)
    - Accumulated wear from tunneling currents
- Requires low $V_{DD}$ for thin oxides and short channels
- Use ESD protection structures where chip meets real world

Summary

- Static CMOS gates are very robust
  - Will settle to correct value if you wait long enough
- Other circuits suffer from a variety of pitfalls
  - Tradeoff between performance & robustness
- Very important to check circuits for pitfalls
  - For large chips, you need an automatic checker.
  - Design rules aren’t worth the paper they are printed on unless you back them up with a tool.
Soft Errors

- In 1970’s, DRAMs were observed to occasionally flip bits for no apparent reason
  - Ultimately linked to alpha particles and cosmic rays
- Collisions with particles create electron-hole pairs in substrate
  - These carriers are collected on dynamic nodes, disturbing the voltage
- Minimize soft errors by having plenty of charge on dynamic nodes
- Tolerate errors through ECC, redundancy
- Soft errors are now a problem for logic too!