Solutions for Homework 1

[Problem 1]

[Problem 2]
[Problem 3]

First we draw the pull-up graph for the given pull-up circuit. Next we draw the pull-down graph according to the pull-up graph. The pull-up and pull-down graphs are shown as following:

Finally, the pull-down circuit can be derived from the pull-down graph, shown as following:
[Problem 4]

In (a), the transistor sees $V_{gs} = V_{DD}$ and $V_{ds} = V_{DS}$. The current is

$$I_{DS1} = \frac{\beta}{2} \left( V_{DD} - V_i - \frac{V_{DS}}{2} \right) V_{DS}$$

In (b), the bottom transistor sees $V_{gs} = V_{DD}$ and $V_{ds} = V_1$. The top transistor sees $V_{gs} = V_{DD} - V_1$ and $V_{ds} = V_{DS} - V_1$. The currents for the bottom and top transistors are identical. That is,

$$I_{DS2} = \beta \left( V_{DD} - V_i - \frac{V_1}{2} \right) V_i = \beta \left( V_{DD} - V_i - V_i - \frac{V_{DS} - V_1}{2} \right) \left( V_{DS} - V_1 \right).$$

Solving for $V_1$, we find

$$V_1 = \left( V_{DD} - V_i \right) - \sqrt{\left( V_{DD} - V_i \right)^2 - \left( V_{DD} - V_i - \frac{V_{DS}}{2} \right) V_{DS}}.$$

Substituting $V_1$ into $I_{DS2}$ equation and simplifying gives $I_{DS1} = I_{DS2}$.

[Problem 5]

(a) Since nMOS transistor can pass strong 0, we have $V_{out} = 0$.

(b) The output of the first pMOS is $|V_{tp}|$ since pMOS transistor pulls no lower than $|V_{tp}|$. For the second pMOS, its output will discharge until $V_{out}$ equals to $|V_{tp}|$ (gate voltage) + $|V_{tp}|$ (threshold of pMOS). Thus, the final voltage of $V_{out}$ is $2|V_{tp}|$.

(c) The output of the pMOS is $|V_{tp}|$ since pMOS transistor pulls no lower than $|V_{tp}|$. For the nMOS, its output is $|V_{tp}|$ (when $|V_{tp}|$ is smaller than $V_{DD} - V_{tn}$).

(d) The output of the pMOS is $V_{DD}$ since pMOS can pass strong 1. The output of the nMOS is $V_{DD} - V_{in}$.

[Problem 6]

(a) nMOS transistor can pass strong 0. When $V_{in} = 0V$, we have $V_{out} = 0V$. 
(b) When $V_{in}=0.6V$, the output will be charged until any of the two conditions ($V_{out}=V_{in}$ or $V_{out}=V_{DD}-V_t$) is met. Since $V_{DD}-V_t=1.2V-0.4V=0.8V$ and $V_{in}=0.6V$, we have $V_{out}=V_{in}=0.6V$.

(c) When $V_{in}=0.9$, the output will be charged until any of the two conditions ($V_{out}=V_{in}$ or $V_{out}=V_{DD}-V_t$) is met. Since $V_{DD}-V_t=1.2V-0.4V=0.8V$ and $V_{in}=0.9V$, we have $V_{out}=V_{DD}-V_t=0.8V$.

(c) When $V_{in}=1.2$, the output will be charged until any of the two conditions ($V_{out}=V_{in}$ or $V_{out}=V_{DD}-V_t$) is met. Since $V_{DD}-V_t=1.2V-0.4V=0.8V$ and $V_{in}=1.2V$, we have $V_{out}=V_{DD}-V_t=0.8V$. 