Problem 1: (a) The high voltage limit is determined by junction breakdown and gate oxide breakdown phenomena. The low voltage limit is set by the threshold voltages of the transistors, $V_{DD} > \max (V_{TN}, V_{TP})$. Raising the VDD supply voltage would result in the diffusion junction breaking down. While this may be nondestructive for the diffusion, it may cause excessive currents, and this may blow the metal lines (like fuses). Gate breakdowns may cause shorts between gate and the substrate.

(b) The charge sharing calculation is

$$Q_T = 2(37)V_{max}$$

$$= [(37)(3) + 85]V_f$$

where $V_{max} = 4.25$ V (ignoring body bias). Then

$$V_f = \left(\frac{74}{196}\right)4.25 = 1.60 \text{ V}$$

(b) For this problem, note that only the charge on two of the initially-charged capacitors contribute to the final sharing problem. Equating initial and final values gives

$$Q_T = 2(37)V_{max}$$

$$= [(37)(2) + 85]V_f$$

which gives $V_f = 1.98$ V.

Problem 2: (a) When CLK is low, the master is enabled and the slave is disabled (pMOS pass transistor on, nMOS pass transistor off). The reverse is true when CLK is high. The limitations are that the master inverter input does not reach Gnd (it is off by the p threshold) and the slave inverter does not reach VDD (n threshold away). Both these conditions can lead to static power dissipation and noise immunity problems. These can be addressed by using a p keeper on the slave inverter and an n keeper on the master inverter.

(b) (i) Refer to lecture notes and textbook. Charge sharing can be prevented by using “p leakers” or precharging.

(ii) and (iii)
(iv) **Advantages:** Overall area can be quite small (no need for separate gates), and the load on preceding gate is only a single transistor. Hence the overall delay can be quite small.

**Disadvantage:** Extra inverters slow down the gate due to increased internal parasitic capacitances. There is a need to precharge more nodes, which implies additional area due to pMOS transistors, and there is additional load on clock drivers.

**Problem 3:** (i) Two-bit magnitude comparator.

(ii) Gate 2 will suffer more from charge sharing since it has a longer pull-down stack.