Solutions for Homework 2

**Problem 1**

a) Use Shannon’s Expansion Theorem (from logic design):

\[ f(x_1, x_2, \ldots, x_n) = x_i f(x_1, x_2, \ldots, x_{i-1}, 1, x_{i+1}, \ldots, x_n) + x'_i f(x_1, x_2, \ldots, x_{i-1}, 0, x_{i+1}, \ldots, x_n) \]

Apply Shannon’s Expansion Theorem recursively. This can be easily mapped to a tree of multiplexers, where the \( x_i \)'s are control inputs.

For general \( n \), we need \( 2^n - 1 \) multiplexers, which can be implemented using \( 2(2^n - 1) = 2^{n+1} - 2 \) transmission gates. We also need \( n \) inverters for the control signals.

b) It can be easily seen from the pull up and pull down graph that there is no Euler path common to both graphs. Therefore, one diffusion gap is necessary. One solution is \{a,b\}, \{c,d,f,e\}.

**Problem 2**

4.10 (a) should be faster than (b) because the NAND has the same parasitic delay but lower logical effort than the NOR. In each design, \( H = 6, B = 1, P = 1 + 2 = 3 \).

For (a), \( G = (4/3) \times 1 = (4/3) \). \( F = GBH = 8 \). \( f = 81/2 = 2.8 \). \( D = 2f + P = 8.6 \). \( x = 6C \times 1 / f = 2.14C \).

For (b), \( G = 1 \times (5/3) \). \( F = GBH = 10 \). \( f = 101/2 = 3.2 \). \( D = 2f + P = 9.3 \). \( x = 6C \times (5/3) / f = 3.16C \).

4.20 NAND: \( g = (\mu + k) / (\mu + 1) \); NOR: \( g = (\mu k + 1) / (\mu + 1) \). As \( \mu \) increases, NOR gates get worse compared to NAND gates because the series pMOS devices become more expensive.

4.26 Let the sizes be \( x \) and \( y \) in the 2-stage path and \( C_1 - x \) in the 1-stage path.

\[ D = 2 \sqrt{\frac{C_2}{x}} + 2 p_{\text{inv}} = \frac{C_2}{C_1 - x} + p_{\text{inv}} \]

This has a nasty third-order closed form solution, but can be solved numerically for \( x \) and thus \( D \).

\[ y = \sqrt{xC_2} \].
**Problem 3**

Let $t_a$, $t_b$, $t_c$, $t_d$, $t_e$ be the contribution of each of the 5 pmos transistors to the pull-up times.

We need to determine $t_a$, $t_b$, $t_c$, $t_d$, $t_e$ such that

$$t_a + t_b = t_c + t_d = t_a + t_d + t_e = t_b + t_c + t_e$$

This yields a total of six equations that must be satisfied from which it follows that $t_e=0$. This implies that the pmos transistor with input $e$ on its gate must be either eliminated or designed to operate infinitely fast.

Hence, resizing in this case is not possible.