

*ECE 538*

# VLSI System Testing

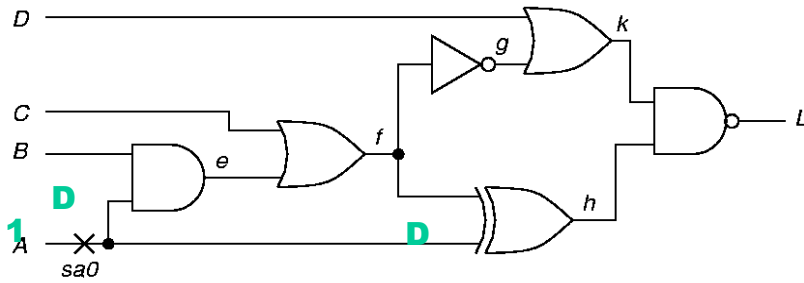
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Test Generation: 2

## Outline

- Problem with D-Algorithm
- PODEM
- FAN
- Fault-independent ATPG
  - Critical path tracing
- Random test generation
- Redundancy identification

- Step 1 – *D-Drive* – Set  $A = 1$

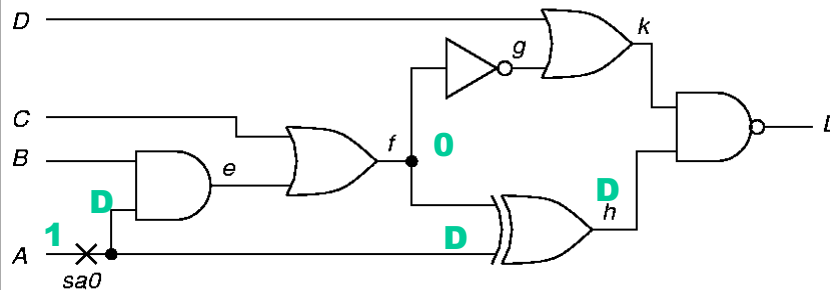


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- Step 2 – *D-Drive* – Set  $f = 0$

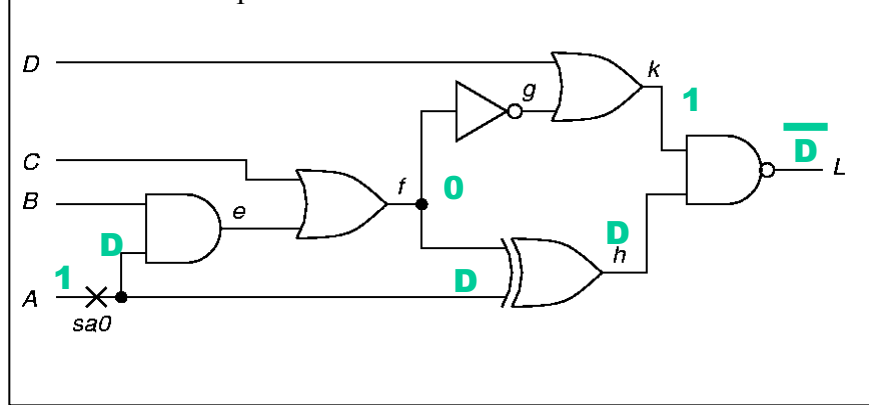


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- Step 3 – *D-Drive* – Set  $k = 1$

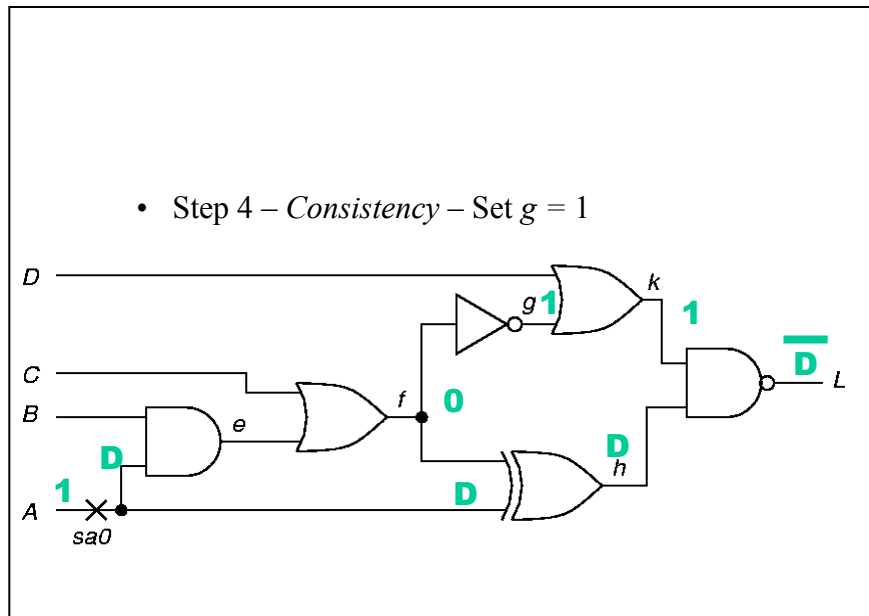


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- Step 4 – *Consistency* – Set  $g = 1$

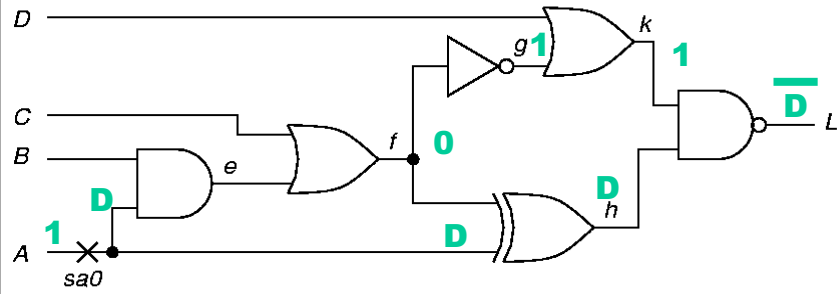


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- Step 5 – Consistency –  $f = 0$  Already set

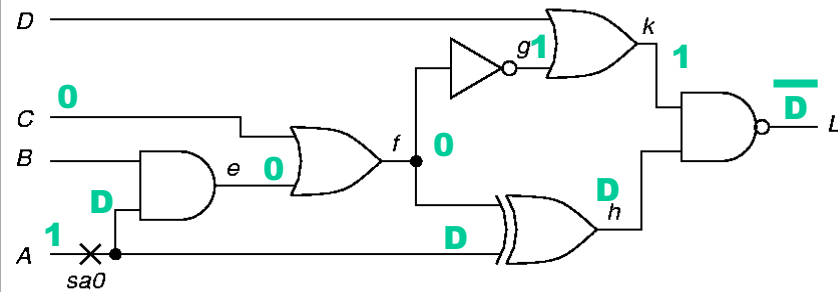


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- Step 6 – Consistency – Set  $c = 0$ , Set  $e = 0$

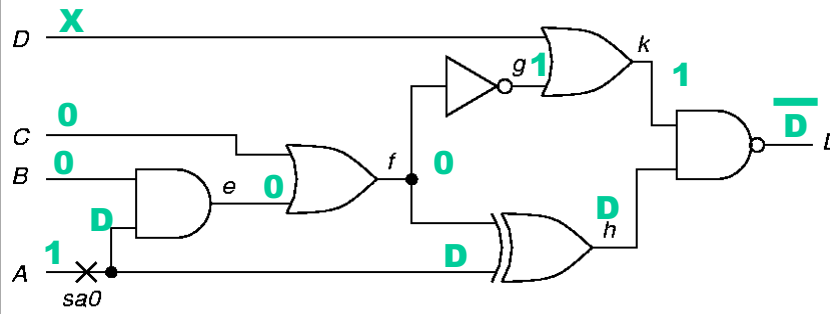


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- Step 7 – Consistency – Set  $B = 0$

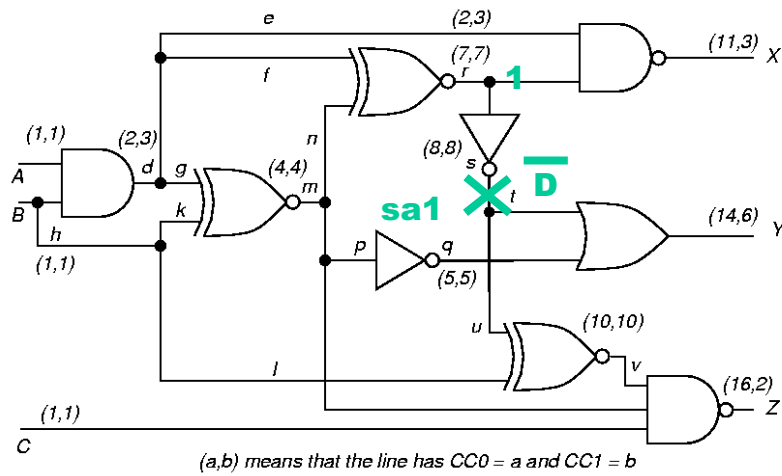


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### Example 7.3 – Fault $sa1$



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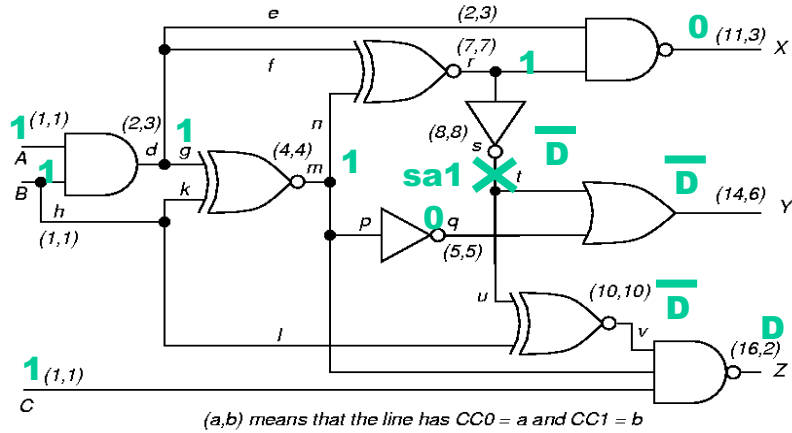
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## Example 7.3 – Step 3 *sa1*

- Test found!

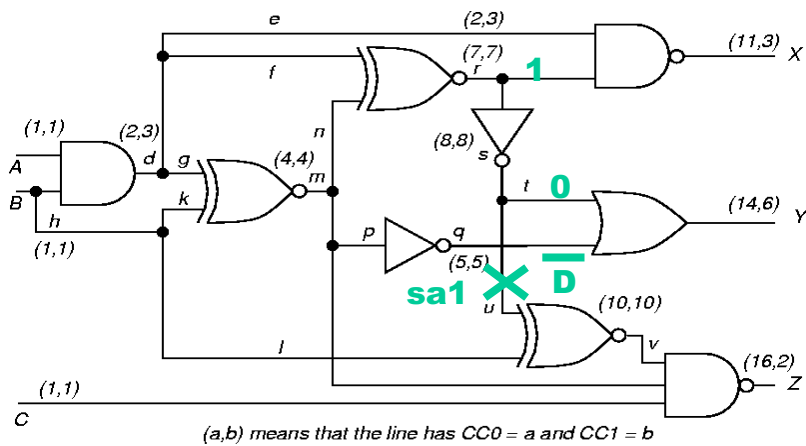


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## Example 7.3 – Fault *u sa1*

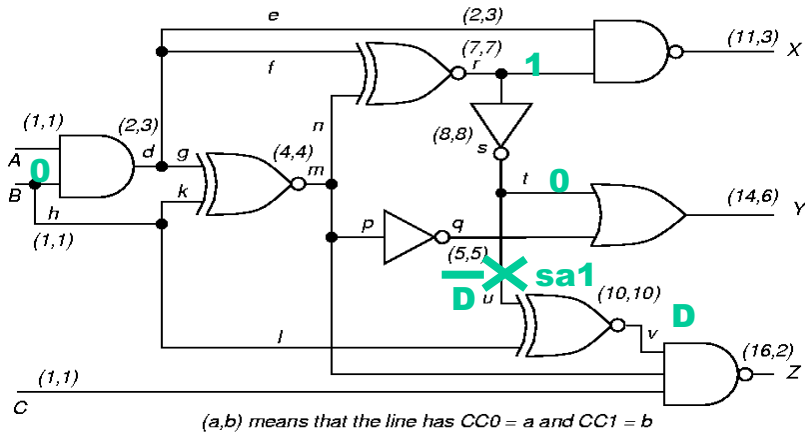


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## Example 7.3 – Step 2 *u sa1*



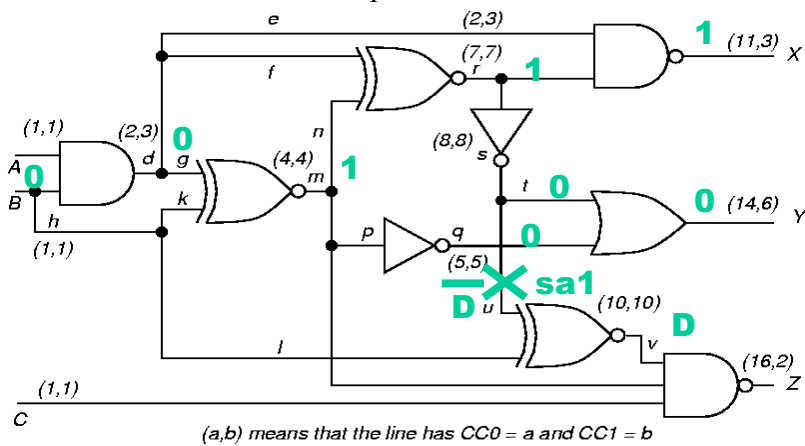
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## Example 7.3 – Step 2 *u sa1*

- Forward and backward implications



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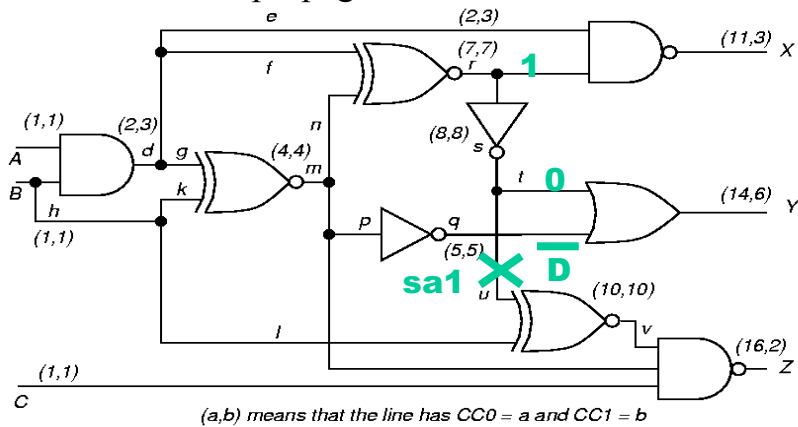


# Inconsistent

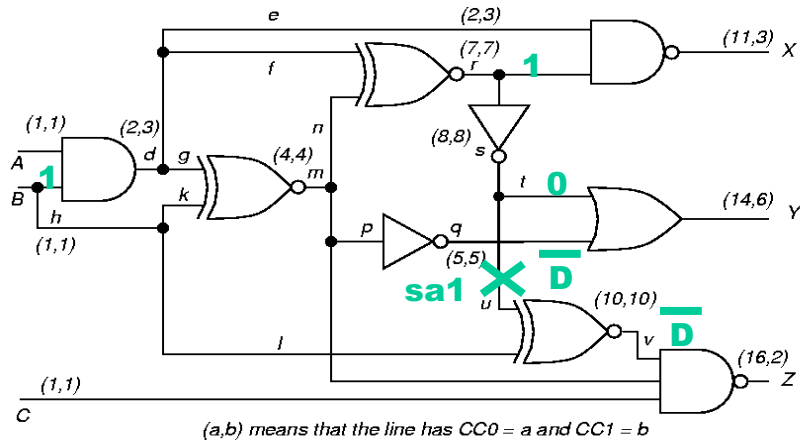
- $d = 0$  and  $m = 1$  cannot justify  $r = 1$  (equivalence)
  - Backtrack
  - Remove  $B = 0$  assignment

## Example 7.3 – Backtrack

- Need alternate propagation



## Example 7.3 – Step 3 *u sa1*

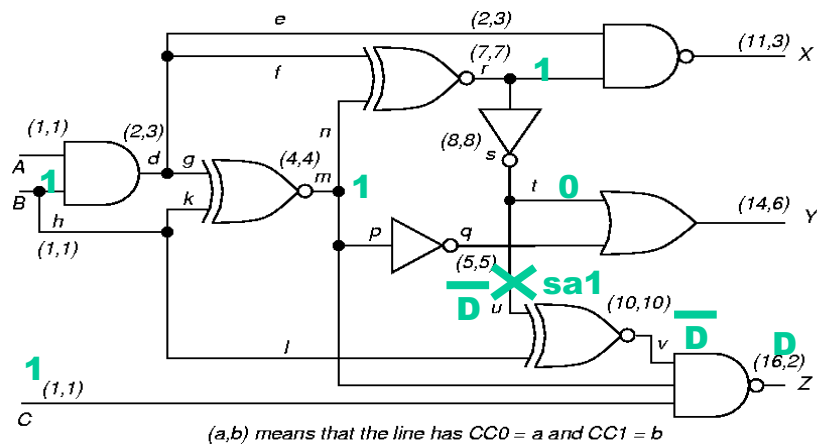


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## Example 7.3 – Step 4 *u sa1*

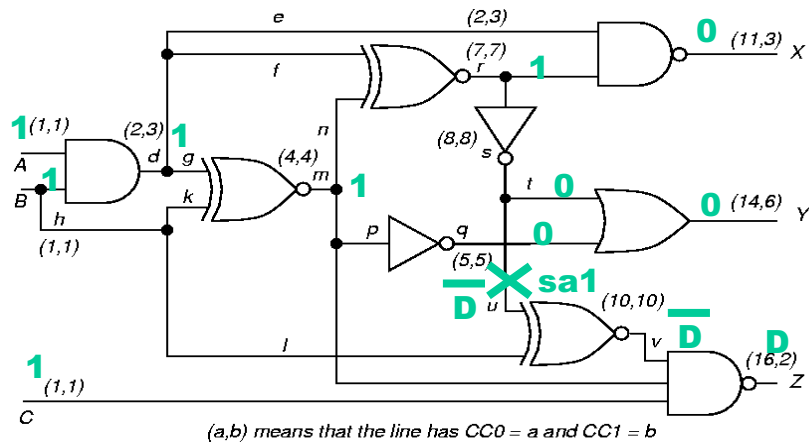


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## Example 7.3 – Step 4 *u sa1*



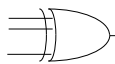
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## Problem with D-Algorithm

Excessive backtracking occurs in certain types of circuits

$2^{n-1}$  justifying values  1

Causes “ripple effect” in many circuits, e.g. adders, parity circuits, error correcting circuits

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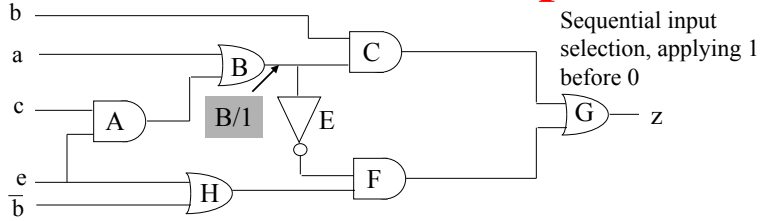
## PODEM: “Path-Oriented Decision Making”

- *Similarity with D-algorithm*: circuit-based, fault-oriented
- *Difference*: Signal values explicitly assigned only at primary outputs, others computed by implication
- Justification not needed!
- Backtracking means reassigning primary inputs when contradiction occurs: “implicit enumeration”
- Simple “backtrace” heuristic used to select primary input

## Branch and Bound Search

- Efficiently searches binary search tree
- *Branching* – At each tree level, selects which input variable to set to what value
- *Bounding* – Avoids exploring large tree portions by artificially restricting search decision choices
  - Complete exploration is impractical
  - Uses *heuristics*

# PODEM Example



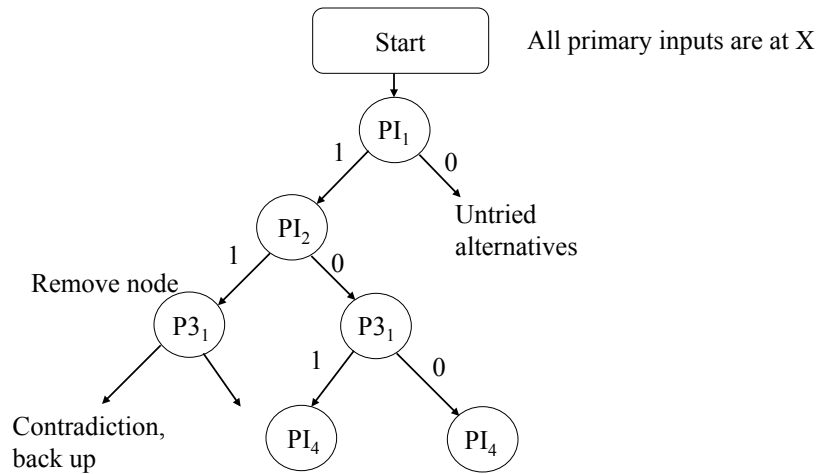
Decision	Implication	Comment
a = 1		Contradiction at fault Backtrack
a = 0		
b = 1		
c = 1		
e = 1	A = 1, B = 1	Contradiction, backtrack
e = 0	A = 0, B = $\bar{D}$ , E = D, H = 0, F = 0, C = $\bar{D}$ , z = $\bar{D}$	Test found!

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# PODEM Decision Tree



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## PODEM Steps

- Input Assignment
  - Unassigned PIs are selected and assigned new values systematically
  - All implications of each assignment are determined
  - If  $D/\bar{D}$  is implied on a primary output, a test has been found; otherwise a new assignment or a new primary input line is selected

## PODEM Steps

- Primary inputs selection:
  - INITIAL OBJECTIVE: A series of “initial” objectives of the form  $IO_j = (l, v)$  are determined. The first  $IO_0$  is to apply  $v = D/\bar{D}$  to the fault site.
  - BACKTRACING: For each initial objective  $IO_j$ , a path is traced backwards through the circuit to a primary input via a series of “current” objectives
  - Current objectives are selected by heuristics

## PODEM Procedures

```
Procedure Backtrace( $k, v_k$ )  
/* Map objective into PI assignment */  
begin  
   $v = v_k$ ;  
  while  $k$  is a gate input  
  begin  
     $i$  = inversion value of  $k$ ;  
    select an input ( $j$ ) of  $k$  with value  $x$ ;  
     $v = v \oplus i$ ;  
     $k = j$ ;  
  end  
/*  $k$  is a PI */  
  return ( $k, v$ );  
end
```

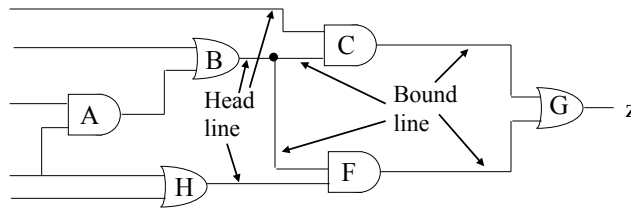
```
Procedure Objective()  
begin  
  /* the target is  $l/v$  */  
  if (value of  $l$  is X) then return ( $l, v$ );  
  select a gate ( $G$ ) from the D-frontier;  
  select an input ( $j$ ) of  $G$  with value X;  
   $c$  = controlling value of  $G$ ;  
  return ( $j, c$ );  
end
```

## PODEM Procedures

```
PODEM()  
begin  
  if (error at PO) then return SUCCESS  
  if (test not possible) then return FAILURE  
  ( $k, v_k$ ) = Objective();  
  ( $j, v_j$ ) = Backtrace( $k, v_k$ );  
  Imply( $j, v_j$ );  
  if PODEM() = SUCCESS then return SUCCESS  
  /* reverse decision */  
  Imply( $j, v_j$ );  
  if PODEM() = SUCCESS then return SUCCESS;  
  Imply( $j, X$ );  
  return FAILURE
```

## FAN: “Fanout-Oriented Test Generation”

- Two major extensions to PODEM
  - Backtracing may stop at internal lines
  - Multiple backtrace-procedures attempts to simultaneously satisfy a set of objectives
- Backtracing can stop at *head lines*



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## Selection Criteria

- Controllability (CC0 and CC1) and observability measures (CO)
  - Exact values can only be determined by exhaustive simulation
  - Estimates are useful for guiding test generation (more controllable  $\Leftrightarrow$  low values, more observable  $\Leftrightarrow$  low values)

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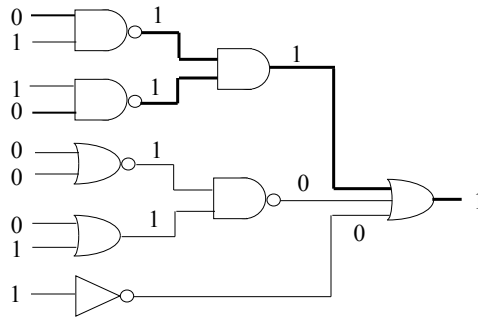
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## Critical Path Test Generation

- Recursively determine critical paths

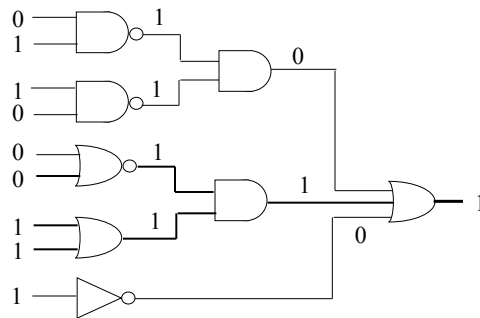


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## Critical Path Test Generation



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## Redundancy Removal Using ATPG

- Redundancy identification
- Redundancy removal

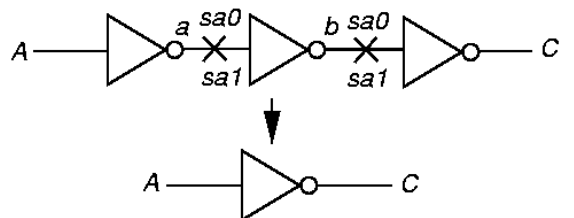
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## Irredundant Faults

- Combinational ATPG can find redundant (unnecessary) hardware



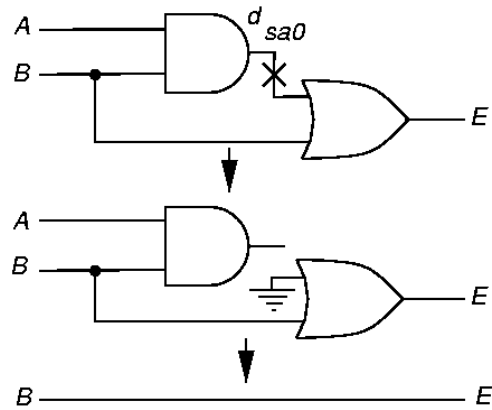
- |                  |         |
|------------------|---------|
| • Fault          | Test    |
| $a\ sa1, b\ sa0$ | $A = 1$ |
| $a\ sa0, b\ sa1$ | $A = 0$ |
- Therefore, these faults are not redundant

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## Redundant Hardware and Simplification

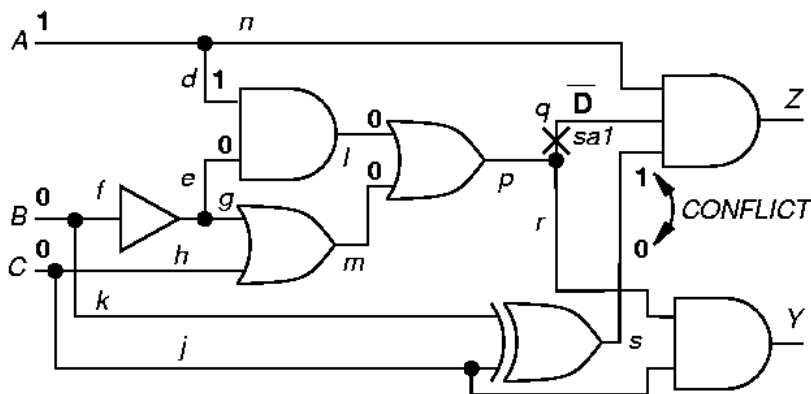


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## Redundant Fault Example



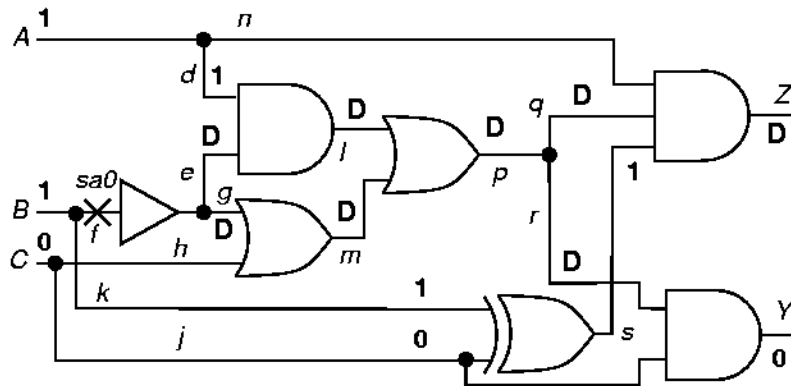
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## Multiple Fault Masking

- $f$  sa0 tested when fault  $q$  sa1 not there



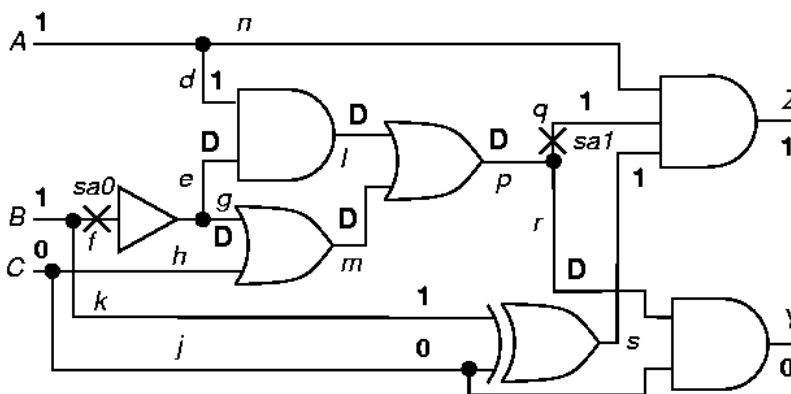
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## Multiple Fault Masking

- $f$  sa0 masked when fault  $q$  sa1 also present



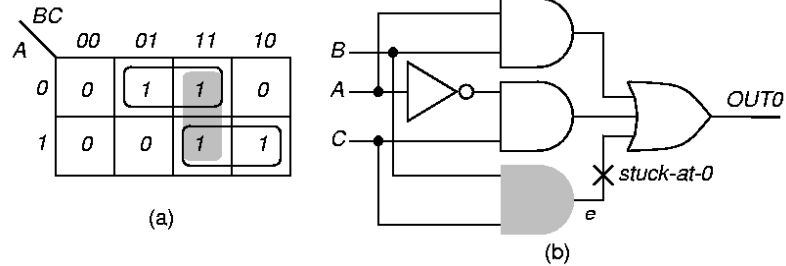
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## Intentional Redundant Implicant *BC*

- Eliminates hazards in circuit output



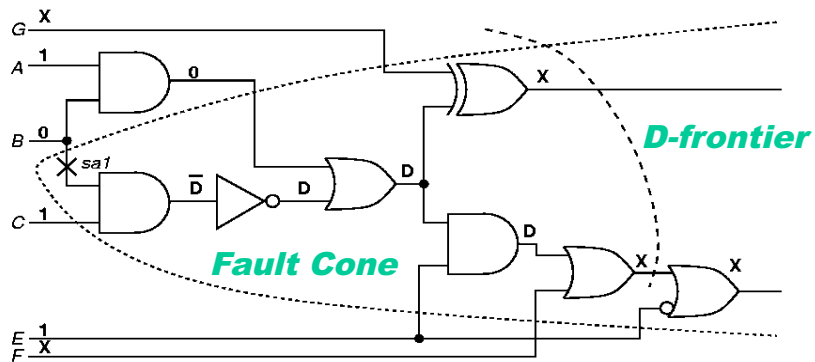
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## Fault Cone and D-Frontier

- Fault Cone* -- Set of hardware affected by fault
- D-frontier* -- Set of gates closest to POs with fault effect(s) at input(s)



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## Redundancy Removal

Repeat until there are no more redundant faults:

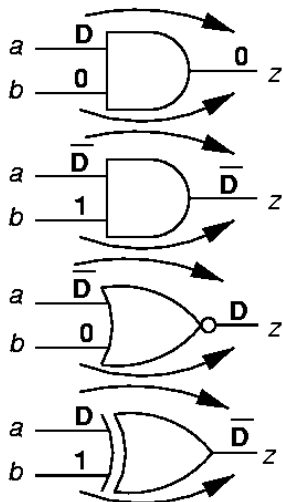
- {
- Use ATPG to find all redundant faults;
- Remove all redundant faults with non-overlapping fault cone areas;
- }

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## Forward Implication



- Results in logic gate inputs that are significantly labeled so that output is uniquely determined
- AND gate forward implication table:

	<i>a</i> \ <i>b</i>	0	1	X	D	$\bar{D}$
0		0	0	0	0	0
1		0	1	X	D	$\bar{D}$
X		0	X	X	X	X
D		0	D	X	D	0
$\bar{D}$		0	$\bar{D}$	X	0	$\bar{D}$

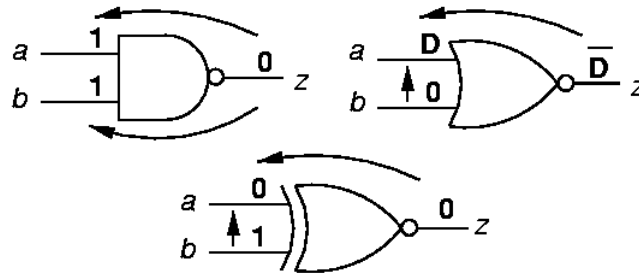
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## Backward Implication

- Unique determination of all gate inputs when the gate output and some of the inputs are given



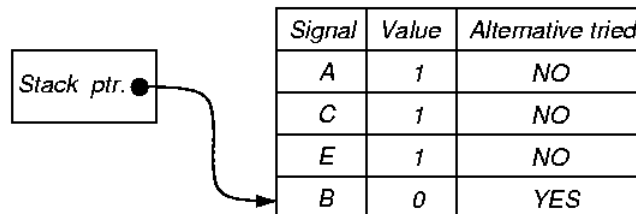
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## Implication Stack

- Push-down stack. Records:
  - Each signal set in circuit by ATPG
  - Whether alternate signal value already tried
  - Portion of binary search tree already searched

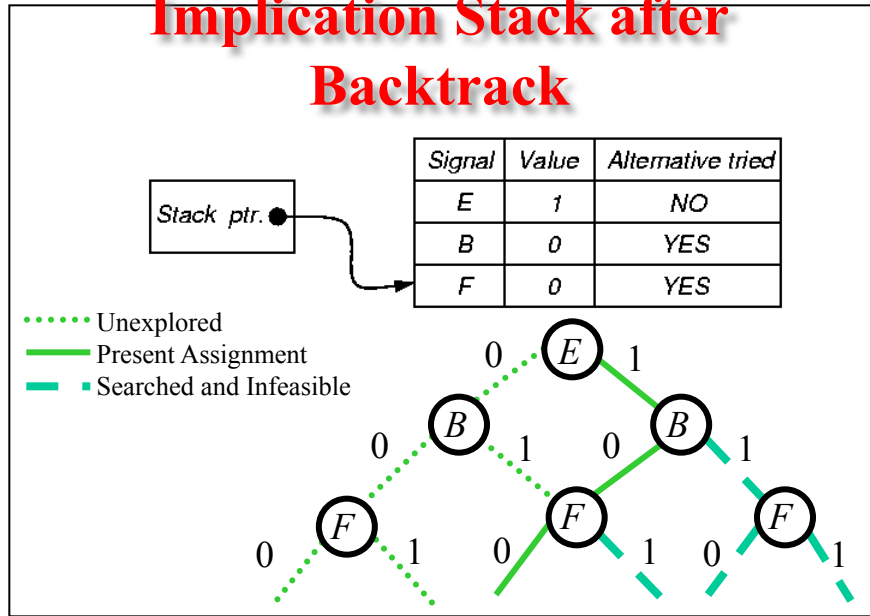


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## Implication Stack after Backtrack

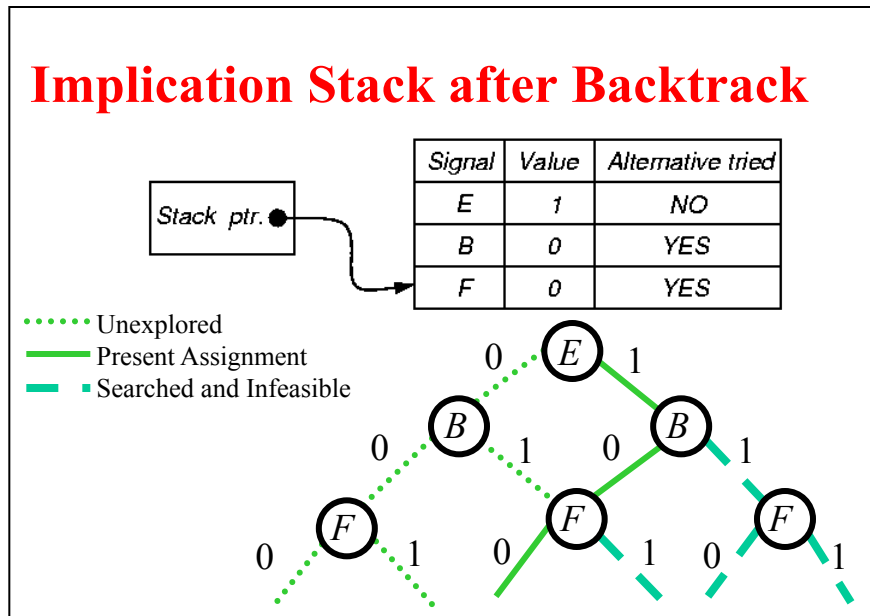


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## Implication Stack after Backtrack



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