ECE 538

VLSI System Testing

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Lecture 2:
Test Process and Equipment

Lecture 2 VLSI Testing Process and Equipment

- **Motivation**
- **Types of Testing**
- **Test Specifications and Plan**
- **Test Programming**
- **Test Data Analysis**
- **Automatic Test Equipment**
- **Parametric Testing**
- **Summary**

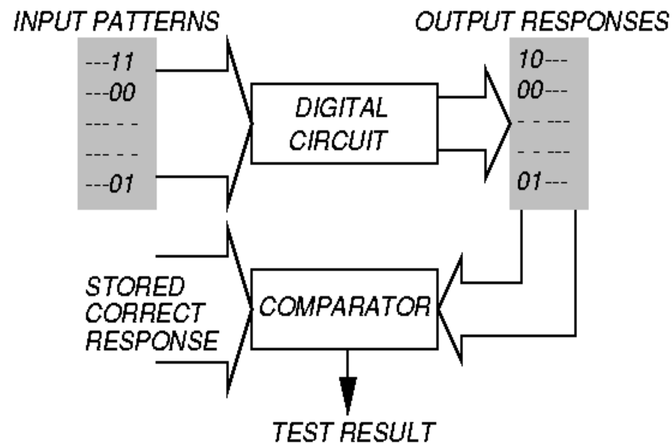
Motivation

- **Need to understand some *Automatic Test Equipment* (ATE) technology**
  - **Influences what tests are possible**
  - **Serious analog measurement limitations at high digital frequency or in the analog domain**
  - **Need to understand capabilities for digital logic, memory, and analog test in *System-on-a-Chip* (SOC) technology**
- **Need to understand parametric testing**
  - **Used to take setup, hold time measurements**
  - **Use to compute** V_{IL}, V_{IH}, V_{OL}, V_{OH}, t_r, t_f, t_d, I_{OL}, I_{OH}, I_{IL}, I_{IH}

Types of Testing

- ***Verification testing*, *characterization testing*, or *design debug***
  - **Verifies correctness of design and of test procedure – usually requires correction to design**
- ***Manufacturing testing***
  - **Factory testing of all manufactured chips for parametric faults and for random defects**
- ***Acceptance testing* (*incoming inspection*)**
  - **User (customer) tests purchased parts to ensure quality**

Testing Principle



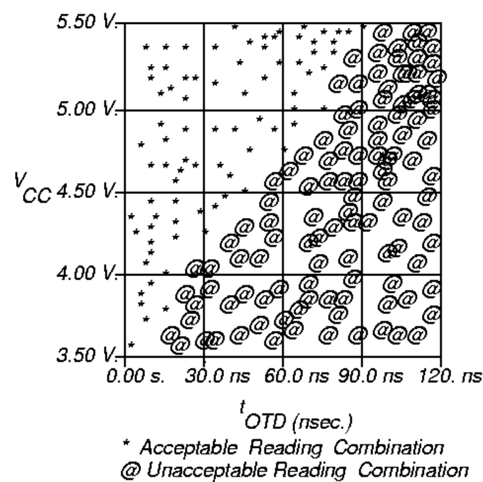
Automatic Test Equipment Components

- **Consists of:**
  - **Powerful computer**
  - **Powerful 32-bit *Digital Signal Processor* (DSP) for analog testing**
  - **Test Program (written in high-level language) running on the computer**
  - **Probe Head (actually touches the bare or packaged chip to perform fault detection experiments)**
  - ***Probe Card* or *Membrane Probe* (contains electronics to measure signals on chip pin or pad)**

Characterization Test

- Worst-case test
  - Choose test that passes/fails chips
  - Select statistically significant sample of chips
  - Repeat test for every combination of 2+ environmental variables
  - Plot results in *Schmoo plot*
  - Diagnose and correct design errors
- Continue throughout production life of chips to improve design and process to increase yield

Schmoo Plot



Manufacturing Test

- Determines whether manufactured chip meets specs
- Must cover high % of modeled faults
- Must minimize test time (to control cost)
- No fault diagnosis
- Tests every device on chip
- Test at speed of application or speed guaranteed by supplier

Burn-in or Stress Test

- Process:
  - Subject chips to high temperature & over-voltage supply, while running production tests
- Catches:
  - *Infant mortality* cases – these are damaged chips that will fail in the first few days of operation – causes bad devices to actually fail before chips are shipped to customers
  - *Freak failures*

Types of Manufacturing Tests

- *Wafer sort* or *probe* test – done before wafer is scribed and cut into chips
  - Includes test site characterization – specific test devices are checked with specific patterns to measure:
    - Gate threshold
    - Polysilicon field threshold
    - Poly sheet resistance, etc.
- Packaged device tests

Sub-types of Tests

- *Parametric* – measures electrical properties of pin electronics – delay, voltages, currents, etc. – fast and cheap
- *Functional* – used to cover very high % of modeled faults – test every transistor and wire in digital circuits – long and expensive

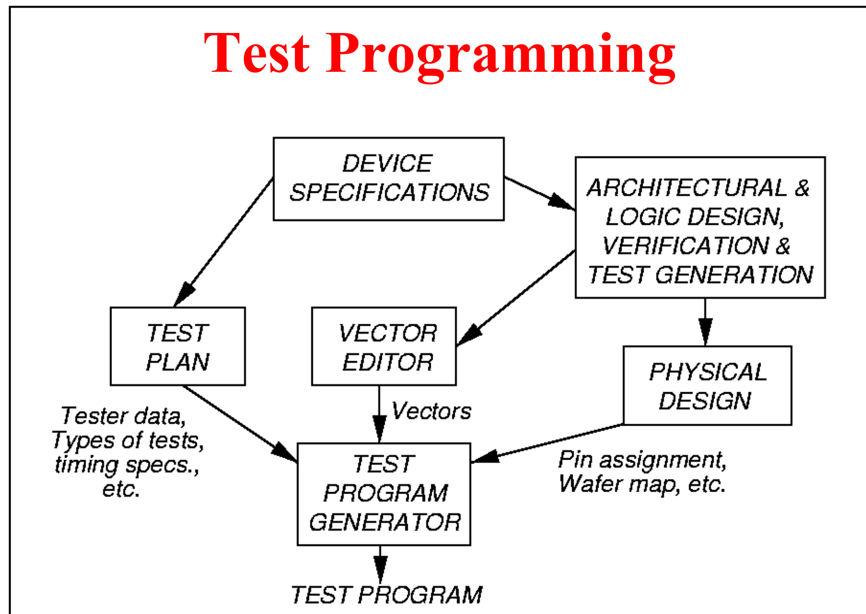
Two Different Meanings of Functional Test

- *ATE and Manufacturing World* – any vectors applied to cover high % of faults during manufacturing test
- *Automatic Test-Pattern Generation World* – testing with *verification vectors*, which determine whether hardware matches its specification – typically have low fault coverage (< 70 %)

Test Specifications & Plan

- Test Specifications:
  - Functional Characteristics
  - Type of *Device Under Test* (DUT)
  - Physical Constraints – Package, pin numbers, etc.
  - Environmental Characteristics – supply, temperature, humidity, etc.
  - Reliability – acceptance quality level (defects/million), failure rate, etc.
- Test plan generated from specifications
  - Type of test equipment to use
  - Types of tests
  - Fault coverage requirement

Test Programming



Test Data Analysis

- **Uses of ATE test data:**
  - **Reject bad DUTs**
  - **Fabrication process information**
  - **Design weakness information**
- **Devices that did not fail are good only if tests covered 100% of faults**
- ***Failure mode analysis* (FMA)**
  - **Diagnose reasons for device failure, and find design and process weaknesses**
  - **Allows improvement of logic & layout design rules**

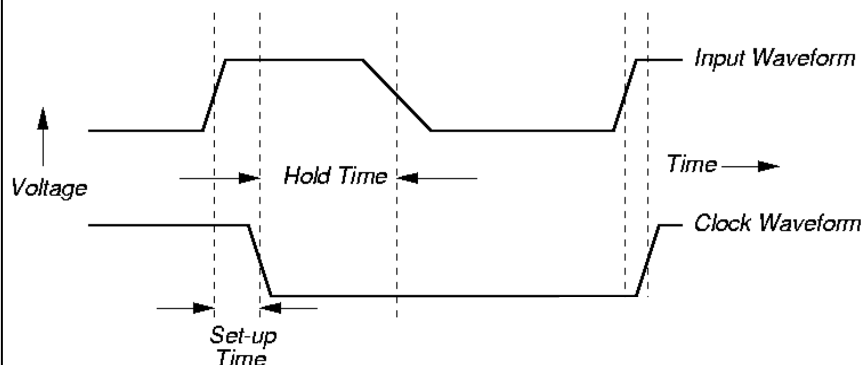
ADVANTEST Model T6682 ATE

LTX FUSION HF ATE

Multi-site Testing – Major Cost Reduction

- One ATE tests several (usually identical) devices at the same time
- For both probe and package test
- DUT interface board has > 1 socket
- Add more instruments to ATE to handle multiple devices simultaneously
- Usually test 2 or 4 DUTS at a time, usually test 32 or 64 memory chips at a time
- Limits: # instruments available in ATE, type of handling equipment available for package

Set-up and Hold Time Tests



Wrap-Up

- **Parametric tests – determine whether pin electronics system meets digital logic voltage, current, and delay time specs**
- **Functional tests – determine whether internal logic/analog sub-systems behave correctly**
- **ATE Cost Problems**
  - **Pin inductance (expensive probing)**
  - **Multi-GHz frequencies**
  - **High pin count (1024)**
- **ATE Cost Reduction**
  - **Multi-Site Testing**
  - **DFT methods like Built-In Self-Test**

Economics of Design for Testability (DFT)

- Consider life-cycle cost; DFT on chip may impact the costs at board and system levels.
- Weigh costs against benefits
  - Cost examples: reduced yield due to area overhead, yield loss due to non-functional tests
  - Benefit examples: Reduced ATE cost due to self-test, inexpensive alternatives to burn-in test

Benefits and Costs of DFT

Level	Design and test	Fabri-cation	Manuf. Test	Maintenance test	Diagnosis and repair	Service interruption
Chips	+ / -	+	-			
Boards	+ / -	+	-		-	
System	+ / -	+	-	-	-	-

\+ Cost increase
\- Cost saving
+/- Cost increase may balance cost reduction

Summary

- Economics teaches us how to make the right trade-offs.
- It combines common sense, experience and mathematical methods.
- The overall benefit/cost ratio for design, test and manufacturing should be maximized; *one should select the most economic design over the cheapest design.*
- A DFT or test method should be selected to improve the product quality with minimal increase in cost due to area overhead and yield loss.

Yield Analysis and Product Quality

- Yield and manufacturing cost
- Clustered defect yield formula
- Defect level

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VLSI Chip Yield

- A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process.
- A chip with no manufacturing defect is called a good chip.
- Fraction (or percentage) of good chips produced in a manufacturing process is called the *yield*. Yield is denoted by symbol *Y*.
- Cost of a chip:

$$\frac{\text{Cost of fabricating and testing a wafer}}{\text{Yield} \times \text{Number of chip sites on the wafer}}$$

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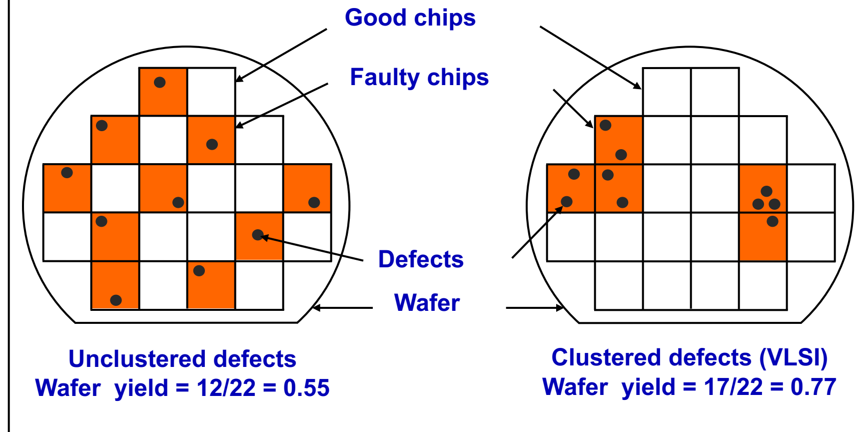
Clustered VLSI Defects



Yield Parameters

- Defect density (d) = Average number of defects per unit of chip area
- Chip area (A)
- Clustering parameter (α)
- Negative binomial distribution of defects,

  $p(x)$ = Prob (number of defects on a chip = x)

$$= \frac{\Gamma(a+x)}{x!\,\Gamma(a)} \cdot \frac{(Ad/\alpha)^{x}}{(1+Ad/\alpha)^{\alpha+x}}$$

where Γ is the gamma function

$\alpha = 0$, $p(x)$ is a delta function (maximum clustering)

$\alpha = \infty$, $p(x)$ is Poisson distribution (no clustering)

Yield Equation

Y = Prob (zero defect on a chip) = p (0)

$$Y = (1 + Ad / \alpha)^{-\alpha}$$

Example: $Ad = 1.0$, $\alpha = 0.5$, $Y = 0.58$

Unclustered defects: $\alpha = \infty$, $Y = e^{-Ad}$

Example: $Ad = 1.0$, $\alpha = \infty$, $Y = 0.37$

too pessimistic !

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Defect Level or Reject Ratio

- *Defect level* (DL) is the ratio of faulty chips among the chips that pass tests.
- DL is measured as *parts per million* (ppm).
- DL is a measure of the effectiveness of tests.
- DL is a quantitative measure of the manufactured product quality. For commercial VLSI chips a DL greater than 500 ppm is considered unacceptable.

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Determination of DL

- From field return data: Chips failing in the field are returned to the manufacturer. The number of returned chips normalized to one million chips shipped is the DL.
- From test data: Fault coverage of tests and chip fallout rate are analyzed. A modified yield model is fitted to the fallout data to estimate the DL.

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Modified Yield Equation

- Three parameters:
  - Fault density, f = average number of stuck-at faults per unit chip area
  - Fault clustering parameter, β
  - Stuck-at fault coverage, T
- The modified yield equation:

$$Y(T) = (1 + TAf / \beta)^{-\beta}$$

Assuming that tests with 100% fault coverage (T = 1.0) remove all faulty chips,

$$Y = Y(1) = (1 + Af / \beta)^{-\beta}$$

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Defect Level

$$DL(T) = \frac{Y(T) - Y(1)}{Y(T)}$$

$$= 1 - \frac{(\beta + TAf)^{\beta}}{(\beta + Af)^{\beta}}$$

Where T is the fault coverage of tests, Af is the average number of faults on the chip of area A, β is the fault clustering parameter. Af and β are determined by test data analysis.

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Summary

- VLSI yield depends on two process parameters, defect density (d) and clustering parameter (α).
- Yield drops as chip area increases; low yield means high cost.
- Fault coverage measures the test quality.
- Defect level (DL) or reject ratio is a measure of chip quality.
- DL can be determined by an analysis of test data.
- For high quality: DL < 500 ppm, fault coverage ~ 99%

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