Perspective

# Quo Vadis Test? The Past, the Present, and the Future: No Longer a Necessary Evil

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**For a long** time, test was considered to be an afterthought in the design and manufacturing of integrated circuits. Designers were the heroes of the industry and the foundry was the magical (and mysterious) place where wafers were produced and revenue generated. The test engineers worked in the background—quietly and without much fuss—and they were there just to catch the chips that were tossed to them, and toss back the chips that passed scrutiny. Test was a "four-letter word" and it was indeed deemed to be a necessary evil. The world of design and test was separated by an insurmountable brick wall. The test industry was dominated by tester companies that made the "Big Iron" automatic test equipment (ATE).

All that changed with the advent of design-for-testability (DfT) in the 1980s and today's *IEEE Design&Test* (D&T) was launched as *IEEE Design & Test of Computers* to showcase the importance of DfT. Test was no longer an afterthought—it was now a part of the design flow, as we saw the adoption of structured DfT techniques such as scan design, and EDA companies developed automatic test generation (ATPG) tools. These tools were adopted by chipmakers, and most leading semiconductor companies even had their own EDA teams with a focus on DfT tools. From being an exclusive concern of chipmakers, test also became important for board (PCB) makers, who needed automated and practical solutions for high-density boards and systems. The test community rallied around standards such as the IEEE 1149.1 Boundary Scan, which was not only adopted widely, but also served as a first step toward newer standards in subsequent years.

The early years of DfT saw considerable resistance from designers, who saw the insertion of testability logic as overhead that they could not afford. In fact, the use of the term "overhead" was rather unfortunate. Overhead had an immediate negative connotation and we should have avoided the use of this word. The test community made valiant attempts to push back, and I recall a very persuasive article in D&T in 1994, in which Ben Bennetts argued that overhead should be replaced with "quality improvement factor (Quif)." I applauded as I read the article, but it is a pity that the industry continued to refer to DfT as overhead. There was endless resistance to scan insertion and all other types of DfT solutions.

The 1990s saw continued process scaling and the emergence of diagnosis and yield learning as key to timely volume production ("time to money"). This came as a boon to test, since now overhead could be justified for additional reasons—defect screening and quality (defects per million) were not the only incentives to test more and test better. The need for diagnosis also facilitated increased adoption of scan design. Test tools from EDA companies flourished and were widely used by chip designers. In addition, we started seeing tools for diagnosis and defect localization.

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The turn of the century saw major breakthroughs in DfT solutions related to test compression, as EDA companies, chip companies, and university researchers responded to the challenges of high test data volume and test application time. Test also received a major boost with the advent of system-on-chip (SoC) designs and the realization that SoC testing requires a completely new DfT paradigm since we no longer have a known-good-die when we assemble a system. Test cost was estimated to be as much as half the manufacturing cost and test challenges were emerging as scary showstoppers. There was a famous graph from the ITRS 2003, which predicted that the test cost per transistor would exceed the manufacturing cost per transistor before 2015. As a result, a new generation of researchers emerged to address these challenges, and both academia and industry responded with agility to ensure that the SoC revolution became a reality. The IEEE 1500 standard made modular testing of SoCs practical and keywords such as core test wrappers, core test language, test-access mechanisms, and test scheduling showed up prominently in all major conferences and journals in the field. New standards continue to flourish; e.g., IEEE 1687 addresses embedded test instruments, and there is a lot of activity related to IEEE P1838, which is targeted at 3-D stacked ICs.

A major change over the years has been the consolidation of ATE companies and now there are only a handful of companies that survive. Until a few years back, the International Test Conference (ITC), the flagship conference in the field, used to attract attendees, with a large exhibit floor where testers would be displayed. Today the exhibits are smaller, and a lot of the floor space is taken up by booths set up by EDA companies. Some of these changes mirror the consolidation that we have seen in the foundry world; there are only a few fabs worldwide that produce chips at the leading edge of process technology.

Over the past few years, test technology has continued to evolve and flourish. As SoCs integrate more analog content, the testing of mixed-signal SoCs is now a new frontier—test costs for analog and RF blocks in mixed-signal SoCs are escalating and timely test solutions are necessary. In addition, the "big data" revolution has had a major influence on test. We have seen impressive gains made in leveraging machine learning and data analytics to reduce the cost of test, increase yield, and improve the quality of fault diagnosis. Advances in silicon debug have reduced product bring-up costs and decreased the number of design respins. New technologies such as 2.5-D/3-D integration have given a boost to research in testing. There is also considerable interest now in using test to bridge the gap between working silicon and working system. The test community has developed techniques to ensure that no-trouble-founds can be diagnosed quickly and with minimum disruption to product utilization. Adaptive allows us to reduce test cost and test time by learning from recent test outcomes. The pass margins are being dynamically tuned as we strive to make better decisions about pass and fail, and tradeoff yield loss with test escapes. The overhead due to DfT is much more acceptable, especially since we are in the "dark silicon era," transistors are cheap, and we cannot turn on all the devices at the same time anyway. More important today is the impact of DfT on timing closure and power consumption.

The value of test is no longer limited to manufacturing. Test is an investment that provides benefits over the lifetime of the product. Built-in-self-test in a chip can be used for health assessment after system integration and field deployment. On-chip sensors and performance monitors provide a "sea of data" that are used for runtime monitoring and dynamic adaptation. Test is being used to overcome process variations, ensure desired performance through post-silicon tuning, and counter aging in the field.

**Looking Ahead:** What lies ahead for test? I will dare to make several predictions, and I am sure at least some of them will turn out to be accurate!

First, there will be even more emphasis on knowledge discovery and adaptive testing. New technologies such as neuromorphic computing and hardware accelerators (based, for example, on synaptic components and memristors) for machine learning will change the way we view test. Some amount of imperfections might be desirable, since the computation in such systems will have an analog flavor. Companies such as Google, Apple, Microsoft, and Amazon will participate in test conferences. Other new technologies such as silicon nanophotonics, wireless network-on-chip, and quantum computing will introduce unique test challenges as well as opportunities.

Second, a lot of emphasis will shift to anomaly detection using time-series data analysis. If failures can be predicted, we can be proactive and take action to avoid failures. Such a strategy is even more compelling if, as predicted, defects will inevitably escape detection in future technologies. We will have to learn to live with defective components.

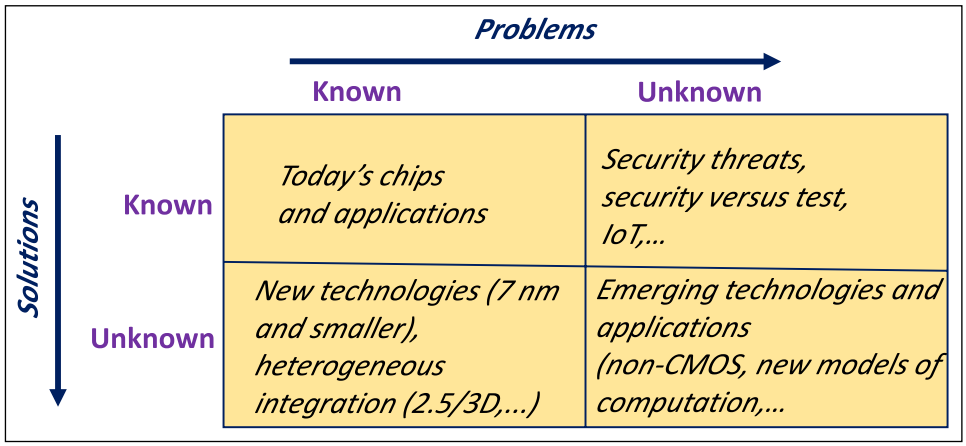


**Figure 1. The knowns and unknowns of test.**

The application landscape will also be vastly different. We have already seen a lot of interest in the Internet of things (IoT). When there are billions of extremely low-power and low-cost IoT edge devices, are we going to test all of them with the same quality levels? It is more likely that we will develop distributed test techniques where IoT devices will collectively test each other and self-organize into reliable networks. Finally, new kinds of MEMS and biomedical devices will become prevalent. These devices will need more functional and noninvasive test solutions. Chips with moving parts and chips that go into pacemakers and implants will have to conform to a different set of specifications.

**Figure 1 highlights** these problems and potential solutions in terms of "knowns" and "unknowns." Test is resilient and will continue to flourish. I was told as a graduate student in the early 1990s that testing is dead. I did not believe it then and I don't want today's students to believe that either. There are still too many open and emerging problems that need to be tackled from the test perspective. Vivat test! Vivat, crescat, floreat! ■

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