ECE 538

VLSI System Testing

Krish Chakrabarty

Lecture 1:
Overview

Lecture 1: Introduction

Class website: people.ee.duke.edu/~krish/teaching/538.html

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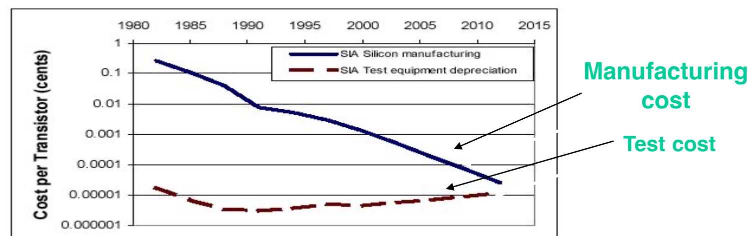
- VLSI realization process
- Verification and test
- Ideal and real tests
- Costs of testing
- Roles of testing
- A modern VLSI device - system-on-a-chip
- Course outline
  - Part I: Introduction to testing
  - Part II: Test methods
  - Part III: Design for testability

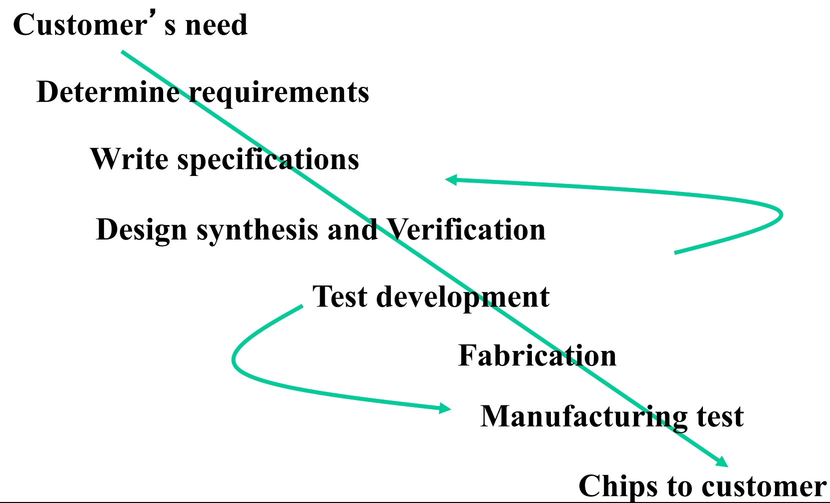
HW #0 – Due Monday Jan 10

- Goal: to make me familiar with your background
  - Submit (e-mail me) a 1-page document that has background information about you:
    - Your name
    - Educational background (e.g.“B.S. in ECE from Duke”)
    - Technical work background (e.g. “I worked at Company C designing ICs”)
    - Which research group at Duke are affiliated with, if any? What is your research on?
    - Have you ever (and briefly describe your yes/no answers):
      - Taken the following courses at undergrad level: circuits, devices, architecture, VLSI design?
      - Used CAD tools for circuit/chip design?
      - Worked on complex software development projects?
    - Why are you taking this course?

International Technology Roadmap for Semiconductors

Updated reports available at http://www.itrs2.net





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Definitions

- Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification: Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- Test: A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

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Verification vs. Test

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

- Verifies correctness of manufactured hardware.
- Two-part process:
  - 1. Test generation: software process executed once during design
  - 2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.

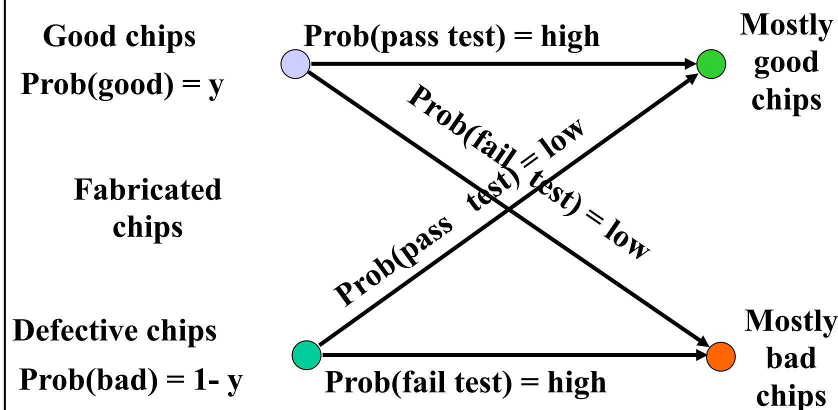
Problems of Ideal Tests

- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. *Defect-oriented testing is an open problem.*

Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the *yield loss.*
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the *defect level.*

Testing as a Filter Process



Costs of Testing

- *Design for testability* (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Software processes of test
  - Test generation and fault simulation
  - Test programming and debugging
- Manufacturing test
  - *Automatic test equipment* (ATE) capital cost
  - Test center operational cost

Cost of Test

- "The emergence of more advanced ICs and SOC semiconductor devices is causing test costs to escalate to as much as 50 percent of the total manufacturing cost."
  - M. Kondrat, "Bridging design and ATE cuts test cost - Test & Measurement - automatic test equipment", Electronic News, Sept 9, 2002.
- "As a result, semiconductor test cost continues to increase in spite of the introduction of DFT, and can account for up to 25-50% of total manufacturing cost".
  - T. Cooper, G. Flynn, G. Ganesan, R. Nolan, C. Tran, Motorola, "Demonstration and Deployment of a Test Cost Reduction Strategy Using Design-for-Test (DFT) and Wafer Level Burn-In and Test", (6/29/2001) Future Fab Intl. Volume 11.
- "Test may account for more than 70% of the total manufacturing cost - test cost does not directly scale with transistor count, dies size, device pin count, or process technology", ITRS 2003.

Motivation: XBox 360 Technical Problems

- The "Red Ring of Death": Three red lights on the Xbox 360 indicator, representing "general hardware failure" (http://en.wikipedia.org/wiki/3_Red_Lights_of_Death)
- The Xbox 360 can be subject to a number of possible technical problems. Since the Xbox 360 console was released in 2005 the console gained reputation in the press in articles portraying poor reliability and relatively high failure rates.
- On 5 July 2007, Peter Moore (Corporate Vice President of the Interactive Entertainment Business in the Entertainment and Devices Division at Microsoft, until August 2007) published an open letter recognizing the problem and announcing 3 years warranty expansion for every Xbox 360 console that experiences the general hardware failure indicated by the three flashing red lights on the console.

XBox 360 Technical Problems (Contd.)

- July 5, 2007, Xbox issues to cost Microsoft $1 billion-plus. Unacceptable number of repairs leads to company extending warranties.
- Matt Rosoff, an analyst at the independent research group Directions on Microsoft, estimates that Microsoft's entertainment and devices division has lost more than $6 billion since 2002.

Roles of Testing

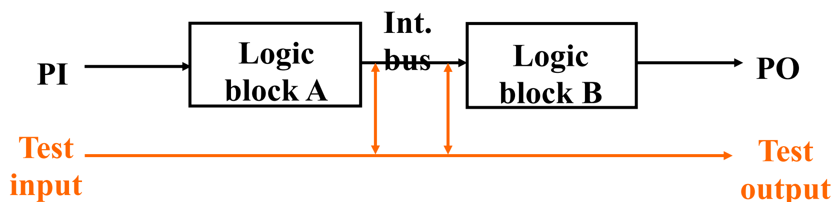
- Detection: Determination whether or not the *device under test* (DUT) has some fault.
- Diagnosis: Identification of a specific fault that is present on DUT.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- *Failure mode analysis* (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

Design for Testability (DFT)

DFT refers to hardware design styles or added hardware that reduces test generation complexity.

Motivation: Test generation complexity increases exponentially with the size of the circuit.

Example: Test hardware applies tests to blocks A and B and to internal bus; avoids test generation for combined A and B blocks.



Cost of Manufacturing Testing

- 0.5-1.0GHz, analog instruments,1,024 digital pins: ATE purchase price
  - = $1.2M + 1,024 x $3,000 = $4.272M
- Running cost (five-year linear depreciation)
  - = Depreciation + Maintenance + Operation
  - = $0.854M + $0.085M + $0.5M
  - = $1.439M/year
- Test cost (24 hour ATE operation)
  - = $1.439M/(365 x 24 x 3,600)
  - = 4.5 cents/second

Automatic Test Equipment

Agilent 93000 series

Top Chip Manufacturers (2016)

Source : iHS iSuppli Semiconductor rankings for 2016 (foundries excluded)

Rank 2015	Rank 2016	Company	Revenue (million $USD)	2016/2015 changes	Market share
1	1	Intel	54 981	+6.9%	15.6%
2	2	Samsung Electronics	40 323	+4.2%	11.4%
4	3	Qualcomm	15 405	-6.6%	4.4%
N/A	4	Broadcom Limited*	14 979	-2.1%	4.2%
3	5	SK Hynix	14 699	-10.9%	4.2%
5	6	Micron Technology	12 963	-7.9%	3.7%
6	7	Texas Instruments	12 686	+3.5%	3.6%
8	8	Toshiba	10 258	+16.1%	2.9%
7	9	NXP	9 306	-3.3%	2.6%
13	10	MediaTek	8 733	+31.2%	2.5%

**Avago+Broadcom (Avago Technologies acquired Broadcom in January, 2016)*

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Top Chip Manufacturers (2019)

Source : Semiconductors (world market)
(foundries excluded) https://tadviser.com/index.php/Article:Semiconductors_(world_market)

Rank 2018	Rank 2019	Company	Revenue (million $USD)	2019/2018 changes	Market share
2	1	Intel	70 785	+1.3%	16.5%
1	2	Samsung Electronics	52 511	-29.7%	12.3%
3	3	SK Hynix	22 868	-36.9%	5.3%
4	4	Micron Technology	19 926	-32.8%	4.7%
5	5	Broadcom Limited	18 275	5.2%	4.3%
6	6	Qualcomm	14 391	-13.3%	3.4%
7	7	Texas Instruments	14 052	-8.6%	3.3%
10	8	STMicroelectronics	9 556	-1.1%	2.2%
9	9	NVIDIA	9 491	-7.0%	2.2%
11	10	Infineon Technologies	8 891	-2.7%	2.1%

- *For the first time in 2020, fabless chip developers had a third of the semiconductor market share.*

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Course Outline
Part I: Introduction

- Basic concepts and definitions (Chapter 1)
- Test process and ATE (Chapter 2)
- Test economics and product quality (Chapter 3)
- Fault modeling (Chapter 4)

Course Outline (Cont.)
Part II: Test Methods

- Logic and fault simulation (Chapter 5)
- Testability measures (Chapter 6)
- Combinational circuit ATPG (Chapter 7)
- Sequential circuit ATPG (Chapter 8)
- Memory test (Chapter 9)
- Delay test (Chapter 12)

Course Outline (Cont.)
Part III: DFT

- Scan design (Chapter 14)
- BIST (Chapter 15)
- Boundary scan (Chapter 16)
- Core-based SOC testing (Chapter 18)