ECE 269

VLSI System Testing

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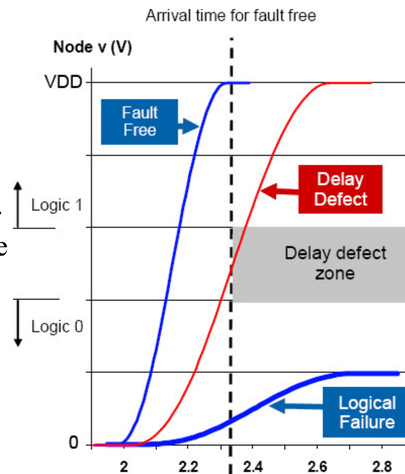
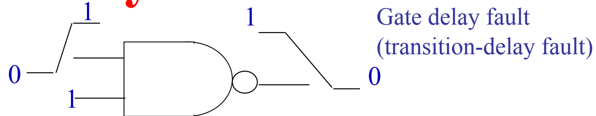
Delay Fault Testing (I)

Delay Faults

- Affect propagation delay of the circuit, circuit fails at high speeds
- More important for high-speed circuits
- Gate delay fault (GDF): slow 1-to-0 or 0-to-1 transition at a gate output
- Path delay fault (PDF): exists a path from a primary input to primary output that is slow to propagate a 0-to-1 or 1-to-0 transition



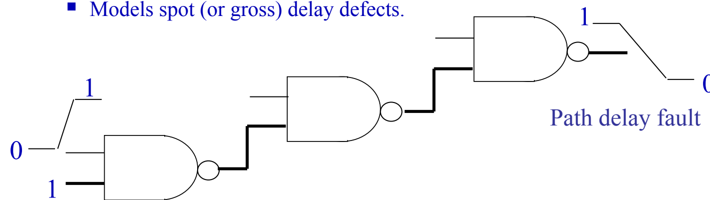
Delay Faults



Gate delay fault
(transition-delay fault)

Transition faults:

- Two faults per gate; slow-to-rise and slow-to-fall.
- Tests are similar to stuck-at fault tests. For example, a line is initialized to 0 and then tested for s-a-0 fault to detect slow-to-rise transition fault.
- Models spot (or gross) delay defects.



Path delay fault

Path-Delay Faults:

- Two PDFs (rising and falling transitions) for each physical path.
- Total number of paths is an exponential function of gates. Critical paths, identified by static timing analysis (e.g., *Primetime* from Synopsys), must be tested.

Types of GDFs

- Gross GDFs (G-GDF): gate delay defect size is greater than system clock period
  - DFs in all paths going through faulty gate, hence catastrophic
  - Also called transition faults (TFs)
- Small GDFs (S-GDF): delay defect size is smaller than system clock period
  - Detectable if causes PDF in at least one path through the gate

Other Delay Fault Models

- *Segment-delay* fault -- A segment of an I/O path is assumed to have large delay such that all paths containing the segment become faulty.
- *Transition* fault -- A segment-delay fault with segment of unit length (single gate):
  - Two faults per gate; slow-to-rise and slow-to-fall.
  - Tests are similar to stuck-at fault tests. For example, a line is initialized to 0 and then tested for s-a-0 fault to detect slow-to-rise transition fault.
  - Models spot (or gross) delay defects.
- *Line-delay* fault – A transition fault tested through the longest delay path. Two faults per line or gate. Tests are dependent on modeled delays of gates.
- *Gate-delay* fault – A gate is assumed to have a delay increase of certain amount (called *fault size*) while all other gates retain some nominal delays. Gate-delay faults only of certain sizes may be detectable.

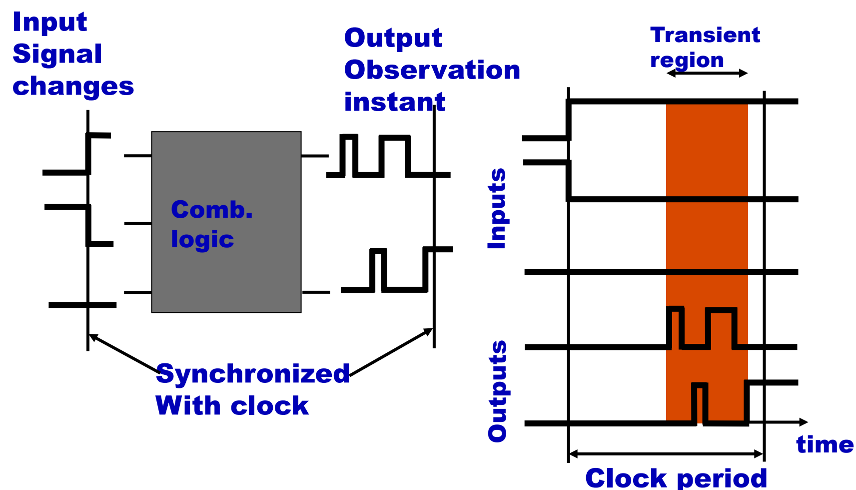
Circuit Delays

- Switching or inertial delay is the interval between input change and output change of a gate:
  - Depends on input capacitance, device (transistor) characteristics and output capacitance of gate.
  - Also depends on input rise or fall times and states of other inputs (second-order effects).
  - Approximation: fixed rise and fall delays (or min-max delay range, or single fixed delay) for gate output.
- Propagation or interconnect delay is the time a transition takes to travel between gates:
  - Depends on transmission line effects (distributed R, L, C parameters, length and loading) of routing paths.
  - Approximation: modeled as lumped delays for gate inputs.

Delay Test Definition

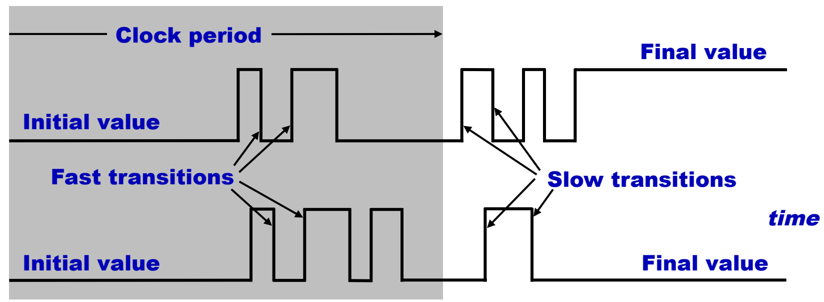
- A circuit that passes delay test must produce correct outputs when inputs are applied and outputs observed with specified timing.
- For a combinational or synchronous sequential circuit, delay test verifies the limits of delay in combinational logic.
- Delay test problem for asynchronous circuits is complex and not well understood.

Digital Circuit Timing



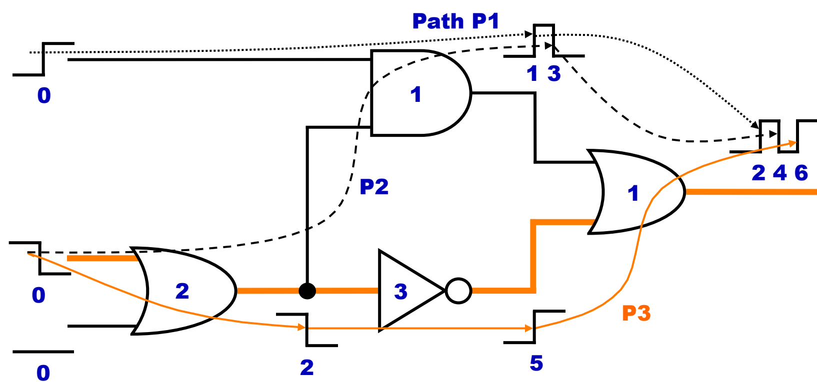
Circuit Outputs

- Each path can potentially produce one signal transition at the output.
- The location of an output transition in time is determined by the delay of the path.



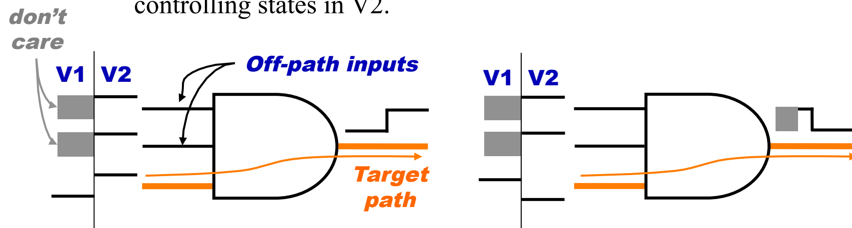
Event Propagation Delays

Single lumped inertial delay modeled for each gate
PI transitions assumed to occur without time skew



Singly-Testable Paths (Non-Robust Test)

- The delay of a target path is tested if the test propagates a transition via path to a path destination.
- Delay test is a combinational vector-pair, V1,V2, that:
  - Produces a transition at path input.
  - Produces static sensitization -- All off-path inputs assume non-controlling states in V2.



Static sensitization guarantees a test when the target path is the only faulty path. The test is, therefore, called *non-robust.* It is a test with minimal restriction. A path with no such test is a *false path.*

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Robust Test

- A robust test guarantees the detection of a delay fault of the target path, irrespective of delay faults on other paths.
- A robust test is a combinational vector-pair, V1, V2, that satisfies following conditions:
  - Produce *real events* (different steady-state values for V1 and V2) on all on-path signals.
  - All on-path signals must have *controlling events* arriving via the target path.
- A robust test is also a non-robust test.
- Concept of robust test is general – robust tests for other fault models can be defined.

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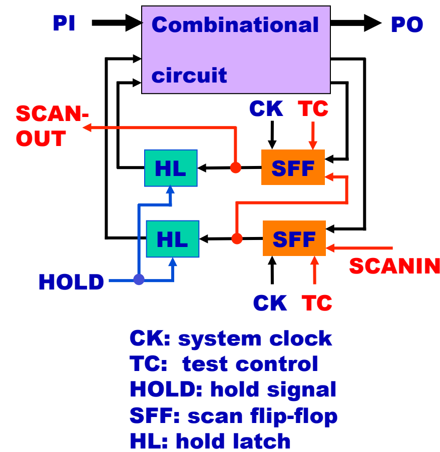
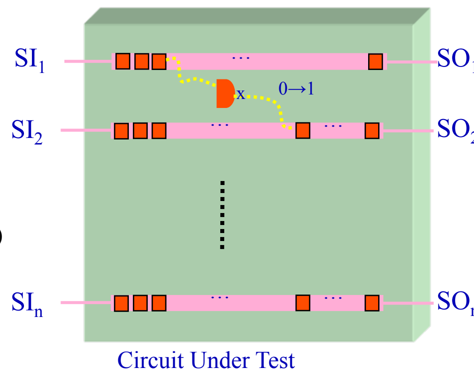
Enhanced-Scan Test

- Apply a transition at the inputs (PIs/states) of a combinational circuit
- Insert hold latch & hold signal
- Generate any arbitrary pattern-pair



Scan-Based Transition Delay Test (Normal Scan)

- Transition Test
  - Pattern pair (V_1, V_2)
  - V_1 – Initialization pattern
  - V_2 – Launch pattern
  - Capture result
- Scan-based Transition Test
  - Shift-in (Initialization pattern)
  - Launch a transition
  - Capture result
  - Shift-out contents



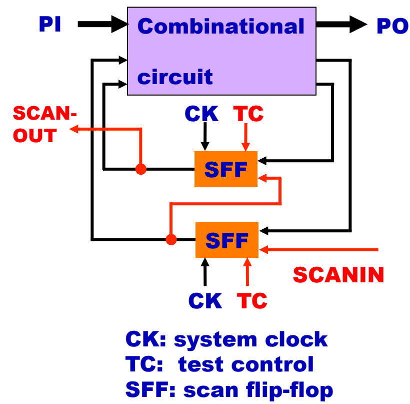
Launch-off-Shift (LOS) and launch-off-capture (LOC) are the two most widely used transition fault test methods.

Normal-Scan Test

- Apply a V_1->V_2 transition at the inputs (PIs/states) of a combinational circuit
- Normal full-scan circuits
- V_1 states serially shifted in
- V_2 states generated by

  (A) one-bit scan shift of V_1

  (B) apply V_1 in normal mode



CK: system clock
TC: test control
SFF: scan flip-flop

No additional hold latches, but pattern-pair not arbitrary

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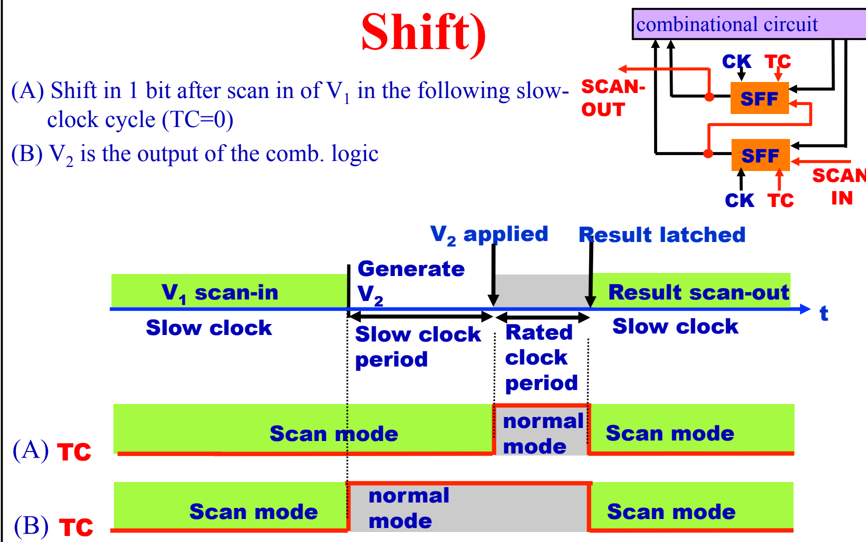
Normal-Scan Test (Launch-on-Shift)

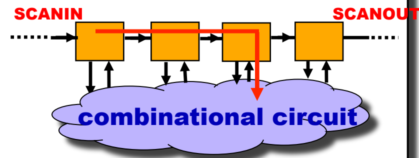
(A) Shift in 1 bit after scan in of V_1 in the following slow-clock cycle (TC=0)

(B) V_2 is the output of the comb. logic

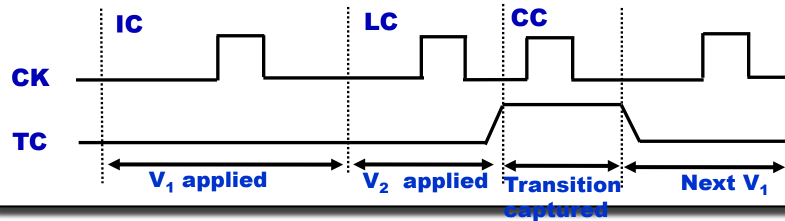


Launch-on-Shift (LOS)

- Transition launched in last shift cycle
- Scan enable must switch at-speed
- Launch path is scan path more controllable
- e.g. $V_1 = 01000101$
  $V_2 = 10100010$

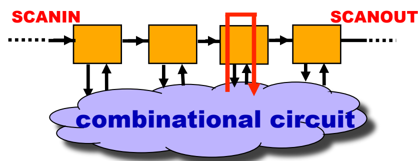


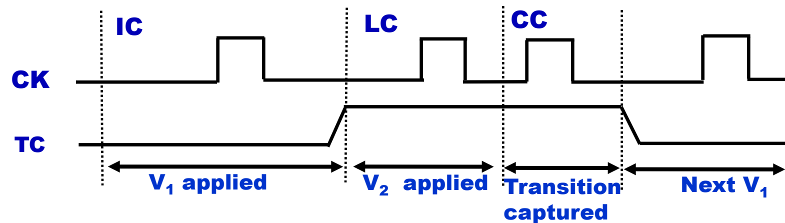
IC: Initialization cycle
LC: Launch cycle
CC: Capture cycle

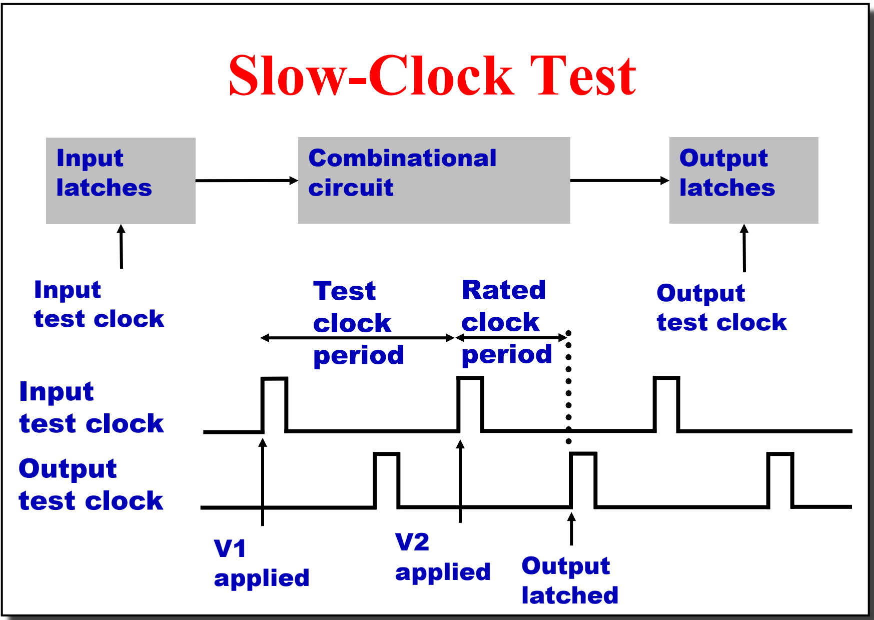


Launch-on-Capture (LOC)

- Transition launched from functional path
- Scan enable does not have to switch at-speed
- Functional launch path
  - Less controllable







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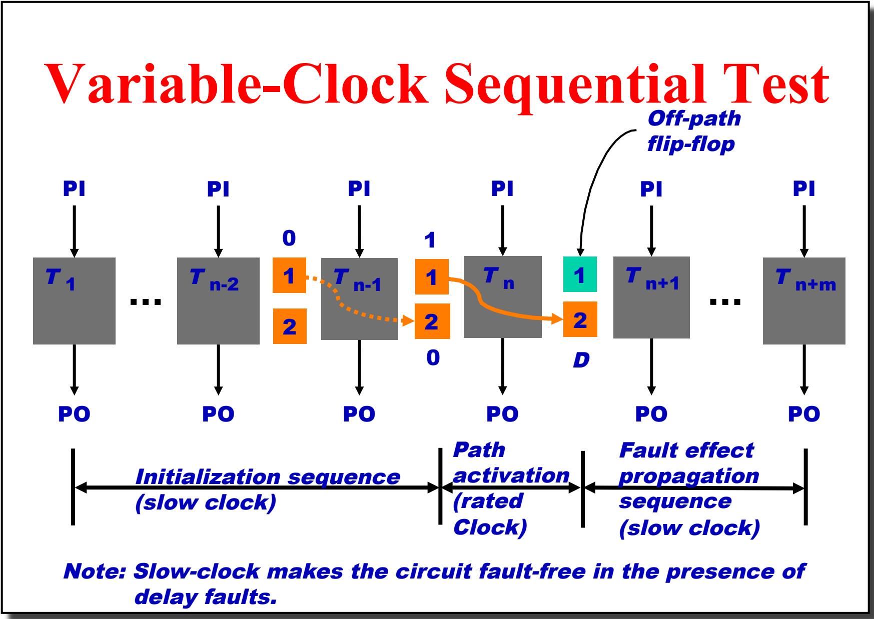

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