ECE 538

VLSI System Testing

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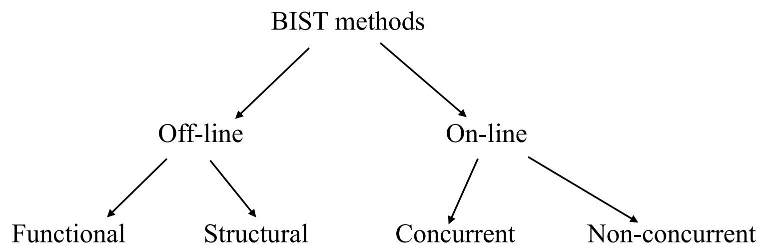
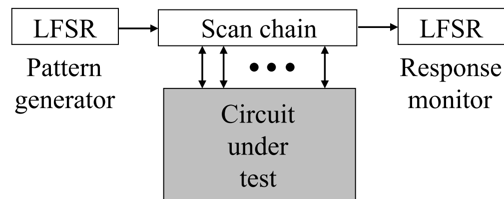
Built-In Self-Test (BIST): 2

Taxonomy

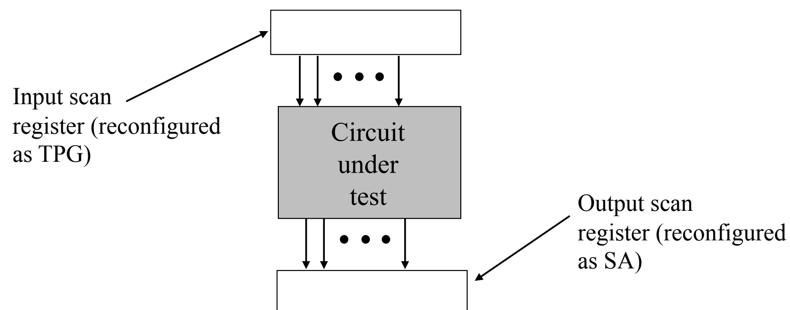


Test-Per-Scan BIST (Scan-BIST)



- High testing time (one pattern every n+1 cycles)
- At-speed testing not possible
- Low performance degradation (none beyond scan)
- Fairy low overhead

Test-Per-Clock BIST



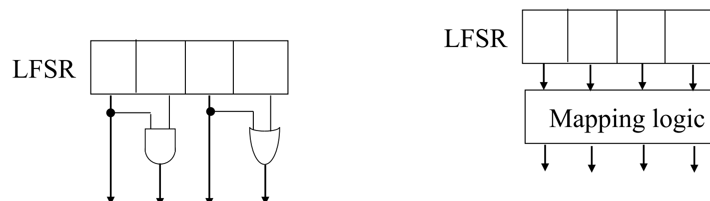
- Suitable for register-based designs
- Low testing time (one pattern every cycle)
- At-speed testing achieved
- Performance degradation (delay on functional paths)
- Overhead may be high

BIST Pattern Generators

- LFSRs are good pseudorandom pattern generators
  - Low cost, easy to implement
- Suitable for test-per-scan and test-per-clock
- LFSR-generated patterns exhibit high degree of randomness (can be measured through statistical correlation tests)

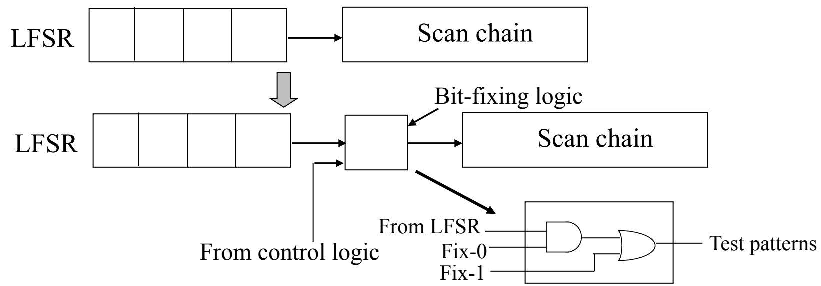
BIST Pattern Generators

- For test-per-clock BIST, non-random patterns are often needed, especially for random-pattern-resistant faults
- Test length with pseudorandom patterns only is excessive
- How to generate non-random patterns?
  - Use weighted random patterns
  - Use mapping logic

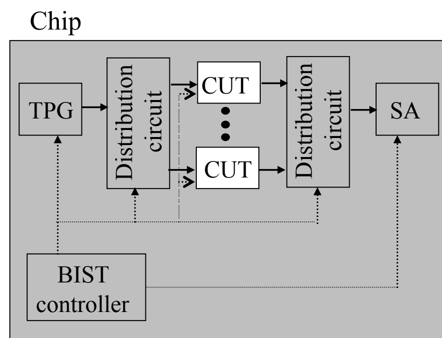


BIST Pattern Generators

- For scan-BIST, the bits in the LFSR sequence should have low linear correlation and sequence length should be large
  - Use primitive polynomials
  - Use longer LFSRs
  - Use bit-fixing logic



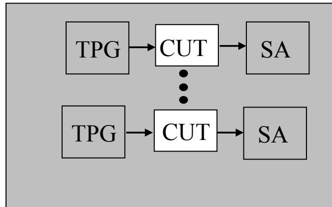
BIST Architectures



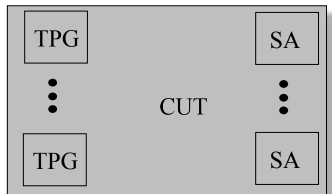
- Centralized and separate BIST
  - Lower overhead
  - Lower fault coverage and high testing time
  - Easy to control and implement

BIST Architectures

Chip



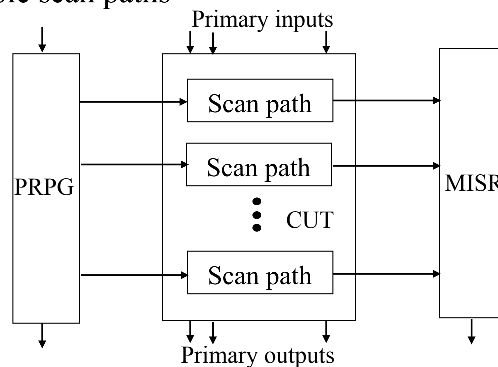
Chip



- Distributed and separate BIST
  - Higher overhead
  - Low testing time (parallelism)
  - Higher fault coverage
- Distributed and embedded BIST
  - Lower overhead
  - Difficult to control
  - In-system reconfiguration employed

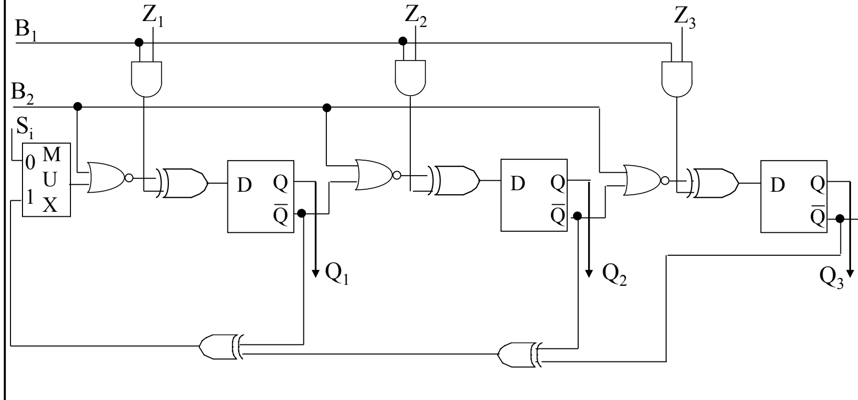
STUMPS Architecture

- *Self-testing using MISR and PRPG*
- Centralized and separate BIST
- Multiple scan paths



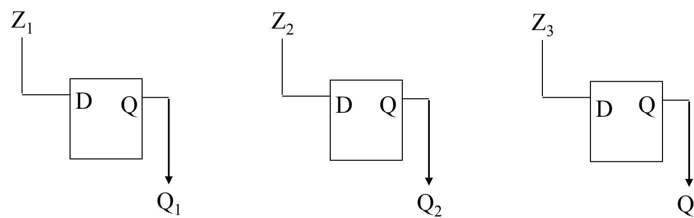
Built-in Logic Block Observer (BILBO)

- Reconfigure registers to act in four modes of operation: functional (parallel load), scan (serial), LFSRs and MISRs

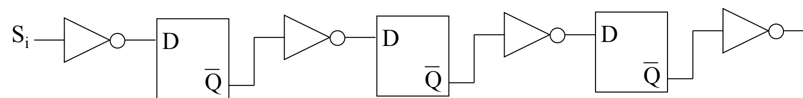


BILBO Operation Modes

$B_1 = B_2 = 1$ (normal mode)



$B_1 = B_2 = 0$ (shift register, scan mode)



$B_1 = 1$, $B_2 = 0$ (MISR, response mode), $B_1 = 0$, $B_2 = 1$ (LFSR mode),