

On the Quality of Accumulator-Based Compaction of Test Responses

Krishnendu Chakrabarty, *Member, IEEE*, and John P. Hayes, *Fellow, IEEE*

Abstract—The accumulator-based compaction (ABC) technique uses an accumulator to generate a composite fault signature for a circuit under test. The error coverage for this method has been previously analyzed using Markov chains. We describe an alternative technique for calculating the error coverage of ABC using the asymmetric error model. This technique relies on the central limit theorem of statistics and can be applied to other count-based compaction schemes. Our analysis shows that ABC provides very high coverage of asymmetric errors. Experiments on the actual fault coverage for the ISCAS 85 benchmark circuits show that extremely high postcompaction fault coverage (close to 100%) is obtained with ABC. They also indicate that the use of a rotate-carry adder does not always improve the fault coverage; in some cases, the fault coverage is actually reduced.

I. INTRODUCTION

BUILT-IN self-testing (BIST) schemes reduce the volume of test data by compressing the test response into a compact form called a signature. One such scheme, using a counter and an accumulator, was proposed for datapath circuits by Saxena and Robinson [11]. Recently, Rajski and Tyszer [9] have shown that a counter is not necessary to generate the fault signature. Their technique, termed accumulator-based compaction (ABC), uses only an accumulator to generate a composite signature from all of the test responses of the circuit under test, as shown in Fig. 1(a). Each “word” of the test response is added to the contents of the accumulator’s register R , and the result in R is, in turn, added to the next word of the test response. The final contents of R after all tests are applied is the signature of the test response.

The ABC technique offers the advantage that for datapaths that already contain an accumulator, the hardware overhead for testing is relatively small. However, like other compaction schemes, ABC can introduce aliasing, which occurs when a faulty response maps to the fault-free signature. This can be attributed to two reasons: 1) error cancellation, whereby errors produced by one test vector can be masked by the errors produced by another test vector, and 2) error leakage because of overflow in the adder. Error leakage can be eliminated for a k -output circuit and m test patterns if a $(k + \lceil \log_2 m \rceil)$ -bit accumulator is used. However, this may not be feasible

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K. Chakrabarty is with the Department of Electrical and Computer Engineering, Boston University, Boston, MA 02215 USA.

J. P. Hayes is with the Advanced Computer Architecture Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109-2122 USA.

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because of hardware overhead and the need to maintain compatibility with the datapath width. In order to reduce error leakage without increasing the overhead, Rajski and Tyszer propose: 1) the use of a 1’s-complement adder, in which the carry out from the most significant bit position is directly connected to the carry input of the adder [9], and 2) the use of a rotate-carry adder, in which the carry output is fed back to the adder through a 1-bit register [10]; see Fig. 1(b).

We analyze accumulator-based compaction with several objectives in mind.

- 1) To use a realistic error model, namely, the asymmetric error model proposed in [12].
- 2) To compute the error coverage accurately using the central limit theorem of statistics. This technique has recently been applied to compute the error coverage for other count-based compaction schemes [3], and our analysis here complements the Markov chain analysis method developed in [9] and [10]. The central limit theorem helps us to determine the error coverage accurately even for short test lengths. Although short test sequences in BIST may not provide adequate coverage of nonmodeled faults, they simplify the test generation problem using many proposed methods such as ROM storage and multiple reseeding of LFSR’s.
- 3) To determine the actual fault coverage obtained with ABC for the ISCAS 85 benchmark circuits [2].
- 4) To evaluate the effect of carry feedback (rotate-carry) on fault coverage.

We begin by analyzing accumulator-based compaction in which the carry output is not fed back to the adder, and then extend our analysis to compaction using rotate-carry adders. We do not investigate the case where 1’s-complement addition is performed, i.e., the carry-out line is directly connected to the carry input.

II. ERROR DETECTION

Consider the use of ABC to compress the responses produced by applying a set of m test patterns to a k -output combinational circuit C . The test response is a sequence of k -bit words W_1, W_2, \dots, W_m , which are interpreted as unsigned integers. The response word W_j is made up of bits $b_1^j, b_2^j, \dots, b_k^j$ where the most significant bit is b_k^j . If b_i^j changes from 0 to 1 (1 to 0) with the other bits of W_j remaining the same, then the numerical value of W_j increases (decreases) by 2^{i-1} .

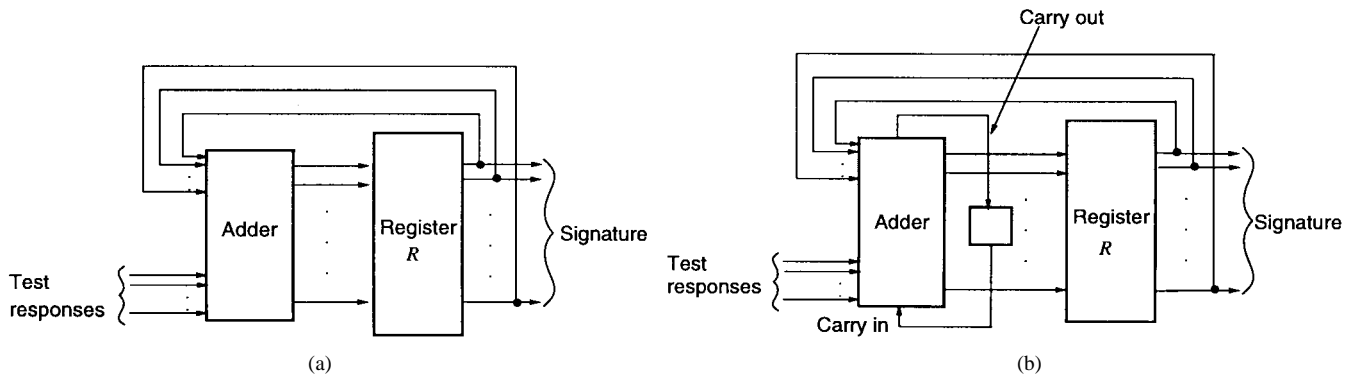
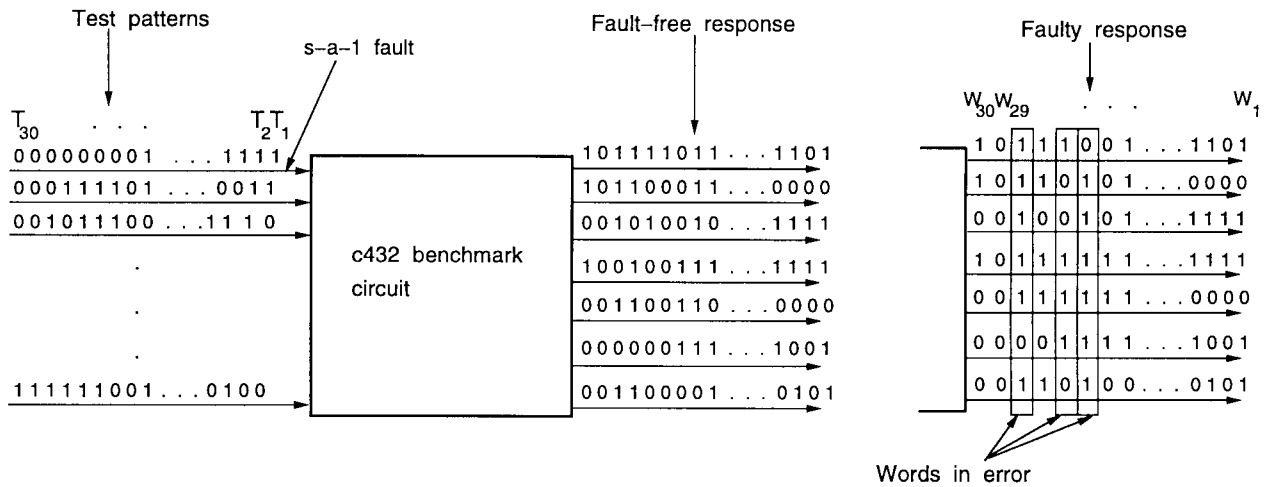


Fig. 1. Accumulator-based compaction (ABC) scheme: (a) without carry feedback, (b) with carry feedback (rotate-carry adder).



<i>i</i>	<i>j</i>										
	$x_{j,i}, v(b_i^j)$	1	...	23	24	25	26	27	28	29	30
1	0,1	...	0,1	0,0	1,0	0,1	0,1	0,1	0,0	0,1	
2	0,0	...	0,1	0,0	1,1	0,0	0,1	0,1	0,0	0,1	
3	0,1	...	0,1	0,0	1,1	1,0	0,0	0,1	0,0	0,0	
4	0,1	...	0,1	0,1	1,1	1,1	0,1	1,1	0,0	0,1	
5	0,0	...	0,1	0,1	1,1	1,1	0,1	0,1	0,0	0,0	
6	0,1	...	0,1	0,1	1,1	1,1	0,0	0,0	0,0	0,0	
7	0,1	...	0,0	0,0	1,1	0,0	0,1	0,1	0,0	0,0	

Fig. 2. Illustration of the notation used to analyze error detection in ABC.

A fault in C affects one or more words of the test response sequence, and each erroneous word contains one or more erroneous bits. Let $x_{j,i}$ be a binary variable defined as follows: $x_{j,i} = 1$ if bit i of W_j is in error, and $x_{j,i} = 0$ otherwise. The following theorem provides a necessary and sufficient condition for error detection.

Theorem 1: Let the number of test patterns applied to a k -output circuit under test be m . An error is not detected by ABC if and only if $\sum_{j=1}^m \sum_{i=1}^k x_{j,i} (-1)^{v(b_i^j)} 2^{i-1} = 0$, where $v(b_i^j)$ is the fault-free binary value and $x_{j,i}$ is 1 if bit i of word W_j is in error and 0 otherwise.

Proof: An error is not detected by ABC if and only if the weight difference δS between the fault-free and faulty signatures is zero. If $x_{j,i} = 1$, then the error in bit i of word

j contributes $(-1)^{v(b_i^j)} 2^{i-1}$ to this difference. If $x_{j,i} = 0$, then this bit is error free and does not affect δS . The final value of δS is obtained by summing over all the bits of every word of the test response. This implies that $\delta S = \sum_{j=1}^m \sum_{i=1}^k x_{j,i} (-1)^{v(b_i^j)} 2^{i-1}$, and the error is not detected if and only if $\sum_{j=1}^m \sum_{i=1}^k x_{j,i} (-1)^{v(b_i^j)} 2^{i-1} = 0$. \square

In Fig. 2, we apply a complete SSL test set of 30 patterns [5] to the c432 circuit with an SSL fault affecting the top input line. From Theorem 1, $\sum_{j=1}^m \sum_{i=1}^k x_{j,i} (-1)^{v(b_i^j)} 2^{i-1} = -17 \not\equiv 0 \pmod{2^8}$. Therefore, the error is detected by an ABC compaction circuit employing an 8-bit adder.

Theorem 1 is the key result that we use later to calculate the error coverage. If a k -bit adder is used, the error is undetected if and only if $\sum_{j=1}^m \sum_{i=1}^k x_{j,i} (-1)^{v(b_i^j)} 2^{i-1} = 0$

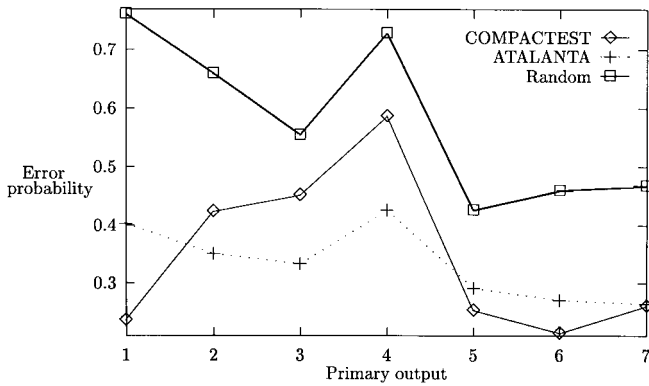


Fig. 3. Error probability at every primary output of the c432 circuit.

(mod 2^k). For compaction with a rotate-carry adder, we have the following result on the necessary and sufficient condition for error masking.

Corollary 1: For compaction with a rotate-carry adder, a fault remains undetected if and only if $\sum_{j=1}^m \sum_{i=1}^k x_{j,i} \{(-1)^{v(b_i^j)} 2^{i-1} + \delta c_{i-1}\} = 0$, where $\delta c_i = c_i - c_i^f$ and c_i (c_i^f) is the carry from the most significant bit position for the i th test pattern in the fault-free (faulty) circuit.

Proof: With a rotate-carry adder, the weight difference δS depends on the carry from the most significant bit position; in fact, $\delta S = \sum_{j=1}^m \sum_{i=1}^k x_{j,i} \{(-1)^{v(b_i^j)} 2^{i-1} + \delta c_{i-1}\}$, from which the result immediately follows. \square

III. ERROR COVERAGE

An error model makes specific assumptions about the probability of occurrence of errors at the output of a faulty circuit that is exercised by test patterns. We employ the asymmetric error model [12], which assumes that the probability of an error depends on the fault-free response. Given a particular SSL fault, an output value can change from 0 to 1 for some input patterns, from 1 to 0 for other patterns, and not change at all for others. The number of 1-to-0 changes generally does not equal the number of 0-to-1 changes, and therefore the probability of the response bit being in error depends on the value of the fault-free function. Experimental results provided in [12] for the 74 181 ALU and the c432 ISCAS benchmark circuit support this model. We carried out an independent set of experiments to study the distribution of error patterns for the c432 circuit.

We first calculated the probability of error at each output for different complete test sets. Reduced test sets for all SSL faults were generated using the COMPACTEST [8] and ATALANTA test generation programs, while pseudorandom patterns were generated using the FSIM fault simulation program [6]. We found, not surprisingly, that the error probability at a circuit output varies from almost 0 to 0.8. Fig. 3 demonstrates that the equiprobable error model, which implies an error probability of 0.5, is not accurate. We next determined the probabilities of 0-to-1 and 1-to-0 errors. Fig. 4 shows that there is a significant discrepancy between these two probabilities; hence, our emphasis on the asymmetric error model.

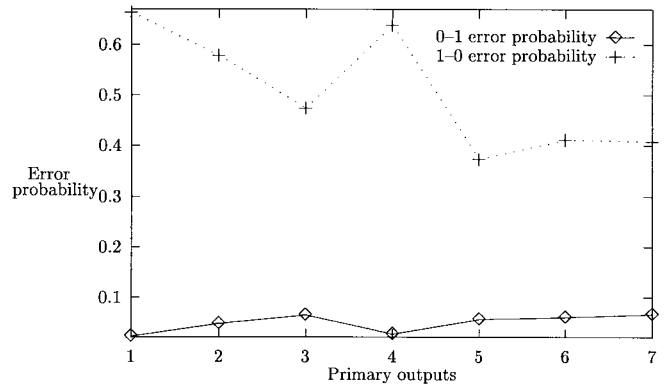


Fig. 4. The 0-to-1 and 1-to-0 error probabilities for the different primary outputs of c432 for pseudorandom patterns.

Let θ_0 (θ_1) be the probability that a response bit is in error given that its fault-free value is 0 (1). We can also assign different error probabilities $\theta_{0,1}, \theta_{0,2}, \dots, \theta_{0,k}$ ($\theta_{1,1}, \theta_{1,2}, \dots, \theta_{1,k}$) to the various outputs z_1, z_2, \dots, z_k of the circuit under test. In order to simplify analysis, however, we first assume that $\theta_{0,1} = \theta_{0,2} = \dots = \theta_{0,k} = \theta_0$ and $\theta_{1,1} = \theta_{1,2} = \dots = \theta_{1,k} = \theta_1$. Later, we briefly explain how our analysis can be extended to the more general case.

Let \mathcal{E} be the event that the fault-free signature equals the fault signature, i.e., $\delta S_m = 0$. The aliasing probability of ABC is the probability of occurrence of the event \mathcal{E} . Therefore, the error coverage of ABC is $1 - P[\mathcal{E}]$. For each W_j ($1 \leq j \leq m$), we define a random variable $X_j = \sum_{i=1}^k x_{j,i} (-1)^{v(b_i^j)} 2^{i-1}$. We are interested in the distribution of the sum $X = \sum_{j=1}^m X_j$ of these random variables since for an adder of size at least $k + \lceil \log_2 m \rceil$, $P[\mathcal{E}] = P[X = 0]$ from Theorem 1. For an adder of size k , as assumed in [9], [10], $P[\mathcal{E}] = P[(X = 0) \cup (X = 2^k) \cup (X = 2^{k+1}) \cup \dots]$.

The asymmetric error model assumes that the test responses are uncorrelated in time, a reasonable assumption for combinational circuits. Thus, it follows from the error model that the X_j 's are independent. Moreover, the X_j 's are bounded in value. Therefore, we can apply the central limit theorem of statistics [4], stated below, to study the distribution of X .

Theorem 2 (Central Limit Theorem [4]): If X_1, X_2, \dots, X_m are independent random variables, where X_j ($1 \leq j \leq m$) has mean μ_j and variance σ_j^2 , then under certain regularity conditions, the limiting distribution of $X = \sum_{j=1}^m X_j$ is normal with mean $\sum_{j=1}^m \mu_j$ and variance $\sum_{j=1}^m \sigma_j^2$.

The regularity conditions in the theorem statement are satisfied by the fact that the X_j 's are bounded in value. Experimental results in [3] show that X can be approximated by the normal distribution for values of m as small as 10. The approximation is even better for larger values of m . Hence, we can accurately determine the error coverage of ABC for short test lengths. We next describe a technique for calculating the mean μ and variance σ^2 of X_j under the asymmetric error model. For a k -output circuit, X_j can take values from the set $\{-(2^k - 1), -(2^k - 2), \dots, 0, \dots, 2^k - 1\}$. Let $\mathcal{P}[u, k]$ be the probability that X_j is u , given that the circuit under test has k outputs. In other words, $\mathcal{P}[u, k]$ is the probability that $\sum_{i=1}^k x_{j,i} (-1)^{v(b_i^j)} 2^{i-1} = u$. First, consider the most significant

TABLE I
MEAN AND VARIANCE OF X_j FOR ABC (a) WITHOUT AND (b) WITH CARRY FEEDBACK

k	θ_0	θ_1	μ_j	σ_j^2
8	0.1	0.2	-25.500	6335.057
	0.3	0.1	50.999	7864.203
	0.4	0.6	-50.999	20971.207
9	0.1	0.2	-51.100	25340.480
	0.3	0.1	102.199	31457.162
	0.4	0.6	-102.200	83885.757
10	0.1	0.2	-102.300	101362.344
	0.3	0.1	204.599	125829.156
	0.4	0.6	-204.599	335544.031
11	0.1	0.2	-204.700	405448.438
	0.3	0.1	409.400	503316.406
	0.4	0.6	-409.399	1342175.6250
12	0.1	0.2	-409.499	1621794.125
	0.3	0.1	818.999	2013266.625
13	0.1	0.2	-819.104	6487184.000
	0.3	0.1	1638.199	8053080.000

(a)

k	θ_0	θ_1	c_1	c_{-1}	μ_j	σ_j^2
8	0.1	0.2	0.1	0.2	-25.599	6335.318
	0.3	0.1	0.1	0.2	50.898	7864.226
	0.4	0.6	0.1	0.2	-50.257	20832.521
9	0.1	0.2	0.1	0.2	-51.199	25340.744
	0.3	0.1	0.1	0.2	102.099	31457.143
	0.4	0.6	0.1	0.2	-101.282	83558.156
10	0.1	0.2	0.1	0.2	-102.399	101362.718
	0.3	0.1	0.1	0.2	204.499	125828.992
	0.4	0.6	0.1	0.2	-203.473	334766.343
11	0.1	0.2	0.1	0.2	-204.800	405449.625
	0.3	0.1	0.1	0.2	409.299	503315.844
	0.4	0.6	0.1	0.2	-408.024	1340322.375
12	0.1	0.2	0.1	0.2	-409.601	1621797.875
	0.3	0.1	0.1	0.2	818.900	2013265.750
	0.4	0.6	0.1	0.2	-817.323	5364264.500

k	θ_0	θ_1	c_1	c_{-1}	μ_j	σ_j^2
8	0.1	0.2	0.5	0.4	-25.399	6335.884
	0.3	0.1	0.5	0.4	51.091	7863.798
	0.4	0.6	0.5	0.4	-49.264	20674.166
9	0.1	0.2	0.5	0.4	-50.999	25341.836
	0.3	0.1	0.5	0.4	102.294	31456.504
	0.4	0.6	0.5	0.4	-100.103	83199.179
10	0.1	0.2	0.5	0.4	-102.199	101363.156
	0.3	0.1	0.5	0.4	204.697	125828.070
	0.4	0.6	0.5	0.4	-202.077	333939.218
11	0.1	0.2	0.5	0.4	-204.599	405450.250
	0.3	0.1	0.5	0.4	409.498	503314.343
	0.4	0.6	0.5	0.4	-406.370	1338392.3750
12	0.1	0.2	0.5	0.4	-409.399	1621801.500
	0.3	0.1	0.5	0.4	819.099	2013260.000
	0.4	0.6	0.5	0.4	-815.367	5359723.500

(b)

bit. If its fault-free value is 0 (1) and it is in error, then it contributes a value of 2^{k-1} (-2^{k-1}) to the value of X_j . The probability of this event is θ_0 (θ_1). Thus, we have the following recurrence relation for $\mathcal{P}[u, k]$:

$$\mathcal{P}[u, k] = \theta_0 \mathcal{P}[u - 2^{k-1}, k - 1] + \theta_1 \mathcal{P}[u + 2^{k-1}, k - 1] + (1 - \theta_0 - \theta_1) \mathcal{P}[u, k - 1].$$

The boundary conditions for this recurrence are as follows:

$$\begin{aligned} \mathcal{P}[1, 1] &= \theta_0 \\ \mathcal{P}[-1, 1] &= \theta_1 \\ \mathcal{P}[0, 1] &= 1 - \theta_0 - \theta_1. \end{aligned}$$

Also, $\mathcal{P}[x, y] = 0$, if $x \geq 2^y$. The mean and variance of X_j are now given by the following equations:

$$\begin{aligned} \mu_j &= \sum_{i=-(2^k-1)}^{2^k-1} i \mathcal{P}[i, k] \\ \sigma_j^2 &= \sum_{i=-(2^k-1)}^{2^k-1} i^2 \mathcal{P}[i, k] - \mu_j^2. \end{aligned}$$

The recurrence relation for $\mathcal{P}[u, k]$ can be used to compute the mean and variance given k, θ_0 , and θ_1 . We have done

this for a number of different values of these parameters; the results are listed in Table I.

If different error probabilities are assigned to the various outputs, the recurrence relation for $\mathcal{P}[u, k]$ has to be slightly modified. Let $\theta_{0,i}$ ($\theta_{1,i}$) be the probability of a 1-to-0 (0-to-1) error on output z_i . The following recurrence relation for $\mathcal{P}[u, k]$ follows directly:

$$\mathcal{P}[u, k] = \theta_{0,k} \mathcal{P}[u - 2^{k-1}, k - 1] + \theta_{1,k} \mathcal{P}[u + 2^{k-1}, k - 1] + (1 - \theta_{0,k} - \theta_{1,k}) \mathcal{P}[u, k - 1].$$

The boundary conditions for this recurrence are as follows:

$$\begin{aligned} \mathcal{P}[1, 1] &= \theta_{0,1} \\ \mathcal{P}[-1, 1] &= \theta_{1,1} \\ \mathcal{P}[0, 1] &= 1 - \theta_{0,1} - \theta_{1,1}. \end{aligned}$$

Also, as before, $\mathcal{P}[x, y] = 0$, if $x \geq 2^y$.

We next calculate μ_j and σ_j^2 for compaction using a rotate-carry adder. Let δc_j be the difference between the carry out of the most significant bit position for the fault-free circuit and that for the faulty circuit. Let c_1 (c_{-1}) be the probability that $\delta c_j = 1$ (-1). To simplify analysis, we assume that the probability of δc_j being 1 is independent of j . Let $\mathcal{P}'[u, k]$ be the probability that X_j is u given that there are k outputs in

TABLE II
ERROR COVERAGE OF ABC FOR SMALL VALUES OF c_1 AND c_{-1} , THE PROBABILITIES OF ERROR PROPAGATION THROUGH THE CARRY OUTPUT

θ_0	θ_1	c_1	c_{-1}	Number of outputs k	Number of tests m	Percentage error coverage						
						Size $k + \lceil \log_2 m \rceil$	Size k	Rotate-carry				
0.1	0.2	0.1	0.2	10	20	99.980	99.818	99.817				
					30	99.990	99.854	99.831				
					40	99.995	99.857	99.843				
					100	99.999	99.923	99.887				
				12	20	99.995	99.953	99.855				
					30	99.998	99.963	99.868				
					40	99.999	99.965	99.871				
					100	99.999	99.974	99.930				
				0.3	0.1	0.1	0.2	10	20	99.998	99.824	99.843
									30	99.999	99.864	99.840
									40	99.999	99.877	99.853
									100	99.999	99.896	99.898
12	20	99.999	99.999					99.956				
	30	99.999	99.999					99.970				
	40	99.999	99.999					99.982				
	100	99.999	99.999					99.987				

the circuit under test. Assuming $c_1 + c_{-1} < 1$, we have the following recurrence relation for \mathcal{P}' :

$$\mathcal{P}'[u, k] = c_1 \mathcal{P}'[u - 1, k] + c_{-1} \mathcal{P}'[u + 1, k] + (1 - c_1 - c_{-1}) \mathcal{P}'[u, k].$$

X_j can now take values from the set $\{-2^k, -(2^k - 1), \dots, 0, \dots, 2^k\}$. Therefore, the mean and variance are given by the following equations:

$$\mu_j = \sum_{i=-2^k}^{2^k} i \mathcal{P}'[i, k]$$

$$\sigma_j^2 = \sum_{i=-2^k}^{2^k} i^2 \mathcal{P}'[i, k] - \mu_j^2.$$

For a continuous random variable, the probability associated with an event $[X = c]$ is zero. However, the underlying random variable in this case is discrete, therefore, we can approximate $P[\mathcal{E}] = P[X = 0]$ by the probability $P[-1 \leq X \leq 1]$, i.e.,

$$P[\mathcal{E}] \approx \int_{-1}^1 \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right) dx$$

where $\mu = m\mu_j$ and $\sigma^2 = m\sigma_j^2$. For an accumulator of size k , we need to calculate the probability $P[X = 0(\text{mod } 2^k)]$, which can be approximated by $\sum_{i=0}^{\infty} (P[i2^k - 1 \leq X \leq i2^k + 1] + P[-i2^k - 1 \leq X \leq -i2^k + 1])$. Therefore

$$P[\mathcal{E}] \approx \sum_{i=0}^{\infty} \int_{i2^k-1}^{i2^k+1} \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right) dx + \sum_{i=0}^{\infty} \int_{-i2^k-1}^{-i2^k+1} \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right) dx.$$

We used Maple to obtain the error coverage for different values of θ_0 , θ_1 , and k . The results are listed in Table II. From the error coverage values, we make the following observations.

- 1) For fixed θ_0 , θ_1 , and k , the error coverage increases with m .

TABLE III
ERROR COVERAGE OF ABC WITH ROTATE-CARRY ADDER FOR HIGHER VALUES OF c_1 AND c_{-1}

θ_0	θ_1	c_1	c_{-1}	Number of outputs k	Number of tests m	Percentage error coverage				
0.1	0.2	0.5	0.4	10	20	99.986				
					30	99.990				
					40	99.994				
					100	99.999				
				12	20	99.991				
					30	99.998				
					40	99.999				
					100	99.999				
				0.3	0.1	0.5	0.4	10	20	99.999
									30	99.999
								12	20	99.999
									30	99.999

- 2) For fixed θ_0 , θ_1 , and m , the error coverage increases with k .
- 3) For small values of c_1 and c_{-1} (e.g., $c_1 = 0.1$ and $c_{-1} = 0.2$ in Table II), the carry feedback in the rotate-carry adder has little impact on the error coverage. This becomes more evident in the following section, where we consider the actual fault coverage for benchmark circuits. However, if c_1 and c_{-1} have higher values as in Table III ($c_1 = 0.5$ and $c_{-1} = 0.4$), the use of a rotate-carry adder increases the error coverage.

IV. FAULT COVERAGE

In order to investigate the effectiveness of ABC, we performed extensive simulations to determine the postcompaction SSL fault coverage for the ISCAS 85 benchmark circuits. These benchmarks include a number of typical datapath circuits that are likely to be used with accumulators [5]. Similar fault simulation results have recently been reported in the literature [1] and [7]; we independently investigated the fault coverage achieved with ABC for the ISCAS 85 circuits. We first performed the fault coverage experiments with reduced sets of test patterns generated by COMPACTEST. The experiments were carried out using a fault-dictionary-based simulation program that explicitly computes fault signatures. A fault is detected if its signature differs from the fault-free

TABLE IV
FAULT COVERAGE OF ABC FOR THE ISCAS 85 CIRCUITS WITH
REDUCED TEST SETS AND ACCUMULATOR OF SIZE $k + \lceil \log_2 m \rceil$

ISCAS benchmark circuit	Number of test patterns	Number of detectable faults	Number of faults detected	Percentage fault coverage
c432	48	520	518	99.62
c499	59	750	750	100
c880	30	942	942	100
c1355	95	1566	1566	100
c1908	129	1870	1868	99.89
c2670	75	2628	2620	99.69
c3540	113	3291	3286	99.97
c5315	59	5291	5291	100
c6288	16	7710	7670	99.48
c7552	88	7419	7418	99.99

TABLE V
FAULT COVERAGE OF ABC FOR SOME ISCAS 85 CIRCUITS WITH
PSEUDORANDOM TEST PATTERNS AND ACCUMULATOR OF SIZE $k + \lceil \log_2 m \rceil$

ISCAS benchmark circuit	Number of test patterns	Number of detectable faults	Number of faults detected	Percentage fault coverage
c432	480	520	518	99.62
c499	2016	750	750	100
c880	2600	936	935	99.89
c6288	128	7710	7672	99.51

signature. Table IV shows the fault coverage obtained with an accumulator of size $k + \lceil \log_2 m \rceil$. The fault coverage of ABC is 100% in four cases, and over 99% for the other six circuits. With a smaller k -bit accumulator, the fault coverage decreases to 94% for the c3540 circuit; for the other circuits, it remains the same.

We also obtained the fault coverage with pseudorandom testing for some of the ISCAS circuits (Table V). The pseudorandom test patterns were generated using FSIM. For these experiments, we considered the c432, c499, c880, and c6288 benchmark circuits. In each case, we obtained nearly 100% coverage of the detectable faults after compaction. The fault coverage remained unchanged with a smaller k -bit accumulator. We were unable to perform the experiments with pseudorandom patterns for the other ISCAS circuits because of the excessive memory required to construct the fault dictionaries. The above experimental results strongly suggest that ABC introduces very little aliasing. They also indicate that if a k -bit accumulator is used for a k -output circuit, then the loss of fault coverage due to error leakage is usually negligible.

In order to evaluate rotate-carry ABC and to compare it with compaction without rotate-carry, we repeated the above experiments by simulating a compaction circuit where the carry out of the most significant bit is fed back to the adder. The results for reduced and pseudorandom test patterns are given in Tables VI and VII, respectively. The last column of these tables indicates an increase (+) or decrease (−) in fault coverage compared to compaction without carry feedback using an accumulator of the same size. We see that the carry feedback does not always lead to an increase in fault coverage. In fact, for some of the circuits, it decreases the fault coverage. An explanation for this is that while the carry feedback reduces error leakage, it increases the likelihood of error cancellation.

TABLE VI
FAULT COVERAGE OF ROTATE-CARRY ABC FOR THE
ISCAS 85 CIRCUITS WITH REDUCED TEST SETS

ISCAS benchmark circuit	Number of test patterns	Number of detectable faults	Number of faults detected	Percentage fault coverage	Increase (+) or decrease (−) in fault coverage
c432	48	520	515	99.04	−
c499	59	750	742	98.93	−
c880	30	942	942	100	0
c1355	95	1566	1557	99.42	−
c1908	129	1870	1863	99.63	−
c2670	75	2628	2628	100	+
c3540	113	3291	3181	96.66	+
c5315	59	5291	5268	99.56	−
c6288	16	7710	7672	99.50	+
c7552	88	7419	7413	99.91	−

TABLE VII
FAULT COVERAGE OF ROTATE-CARRY ABC FOR SOME
ISCAS 85 CIRCUITS WITH PSEUDORANDOM TEST PATTERNS

ISCAS benchmark circuit	Number of test patterns	Number of detectable faults	Number of faults detected	Percentage fault coverage	Increase (+) or decrease (−) in fault coverage
c432	480	520	511	98.27	−
c499	2016	750	742	98.93	−
c880	2600	936	936	100	+
c6288	128	7710	7672	99.51	0

These results also indicate that error cancellation is more likely to cause aliasing, and that error leakage has little impact on fault coverage for these circuits.

We also carried out a set of experiments with the ISCAS 85 benchmarks to determine the impact of faults occurring in the accumulator itself. We found that almost all such faults were covered, and that they caused little or no increase in aliasing, thus confirming other recent results on accumulator faults [1], [7], [9].

V. CONCLUSIONS

Accumulator-based compaction provides extremely high fault coverage with low hardware overhead. The error coverage can be analyzed for the asymmetric error model using the central limit theorem of statistics. We demonstrate that exceptionally high error coverage is obtained for asymmetric errors. Our analysis also shows that aliasing is caused more often by error cancellation than by error leakage. Experimental results show that very high postcompaction fault coverage is obtained for the ISCAS 85 benchmark circuits. Furthermore, the use of a rotate-carry adder does not improve the fault coverage significantly for these circuits; in fact, it sometimes reduces the fault coverage because of an increase in error cancellation.

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Krishnendu Chakrabarty (S'92–M'96) received the B.Tech. degree from the Indian Institute of Technology, Kharagpur, in 1990, and the M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1992 and 1995, respectively, all in computer science and engineering.

While at the University of Michigan, he was a Research Assistant at the Advanced Computer Architecture Laboratory in the Department of Electrical Engineering and Computer Science. Since 1995, he has been an Assistant Professor of Electrical and Computer Engineering at Boston University, Boston, MA. His research interests are in computer-aided design of VLSI circuits and systems, testing, design verification, and fault-tolerant computing.

Dr. Chakrabarty is a member of Sigma Xi.



John P. Hayes (S'67–M'70–SM'81–F'85) received the B.E. degree from the National University of Ireland, Dublin, in 1965, and the M.S. and Ph.D. degrees from the University of Illinois, Urbana–Champaign, in 1967 and 1970, respectively, all in electrical engineering.

While at the University of Illinois, he participated in the design of the ILLIAC III computer. In 1970, he joined the Operations Research Group at the Shell Benelux Computing Center, The Hague, where he worked on mathematical programming.

From 1972 to 1982, he was a Faculty Member of the Departments of Electrical Engineering–Systems and Computer Science of the University of Southern California, Los Angeles. Since 1982, he has been a Professor in the Electrical Engineering and Computer Science Department of the University of Michigan, Ann Arbor. He was the Founding Director of the University of Michigan's Advanced Computer Architecture Laboratory. He was Technical Program Chairman of the 1977 International Conference on Fault-Tolerant Computing, Los Angeles, and the 1991 International Computer Architecture Symposium, Toronto. He is the author of more than 150 technical papers and five books, including *Computer Architecture and Organization* (New York: McGraw-Hill, 1998, 3rd ed.), *Layout Minimization for CMOS Cells* (Norwell, MA: Kluwer, 1992; coauthored with R. L. Maziasz), and *Introduction to Digital Logic Design* (Reading, MA: Addison-Wesley, 1993). His current research interests are in the areas of computer architecture, computer-aided design, verification, and testing, VLSI design, and fault-tolerant embedded systems.

Dr. Hayes is a member of the Association for Computing Machinery and Sigma Xi. He has served as editor of various technical journals, including the IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS and the *Journal of Electronic Testing*.