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Wafer-Level Defect Screening for "Big-D/Small-A" Mixed-Signal SoCs

Sudarshan Bahukudumbi, Sule Ozev, Krishnendu Chakrabarty, and Vikram Iyengar

***Abstract*—Product cost is a key driver in the consumer electronics market, which is characterized by low profit margins and the use of a variety of "big-D/small-A" mixed-signal system-on-chip (SoC) designs. Packaging cost has recently emerged as a major contributor to the product cost for such SoCs. Wafer-level testing can be used to screen defective dies, thereby reducing packaging cost. We propose a new correlation-based signature analysis technique that is especially suitable for mixed-signal test at the wafer-level using low-cost digital testers. The proposed method overcomes the limitations of measurement inaccuracies at the wafer-level. A generic cost model is used to evaluate the effectiveness of wafer-level testing of analog and digital cores in a mixed-signal SoC, and to study its impact on test escapes, yield loss, and packaging costs. Experimental results are presented for a typical mixed-signal "big-D/small-A" SoC, which contains a large section of flattened digital logic and several large mixed-signal cores.**

***Index Terms*—Cost model, defect screening, mixed-signal, signature analysis, system-on-chip (SoC) test, wafer sort.**

I. INTRODUCTION

RAPID advances in the semiconductor industry and in design tools have led to the integration of digital and analog cores in mixed-signal system-on-chip (SoC) integrated circuits. The fraction of die area taken up by analog circuits can range from 5% to 30% for a typical mixed-signal SoC [1]. The DragonBall-MX1 SoC, details for which are presented in [2], is an example of a "big-D/small-A" mixed-signal SoC. Most "big-D/small-A" SoCs comprise of at least a pair of complementary data converters, a significant amount of digital logic and a phase locked loop (PLL) [2], [3]. In the SoC described in [2], the mixed-signal components constitute up to 10% of the overall die area. The applications of "big-D/small-A" SoCs to the consumer market are numerous, ranging from medical monitoring devices to audio products and handheld devices [2], [3]. The consumer electronics market is also characterized by low profit margins and rising packaging costs [4], [5]. Test and packaging costs are therefore of increasing importance for such SoCs.

The test cost for a mixed-signal SoC is significantly higher than that for a digital SoC [6]. This is due to the capital cost associated with expensive mixed-signal automatic test equipment (ATE), as well as the high test times for analog cores. Test methods for analog circuits that rely on low-cost digital testers are therefore especially desirable; a number of such methods have recently been developed [7]–[9].

It is well-known that wafer-level testing leads to early defect screening, thereby reducing packaging and production cost [10], [11]. As highlighted in [4] and [5], packaging cost accounts for a significant part of the overall production cost. Current packaging costs for a cost-sensitive, yet performance-driven IC can vary between \$3.60 to \$20.50, depending on the number of pins in the IC [4]. These costs are further increased for high-performance ICs. It has also been reported that the packaging cost per pin exceeds the cost of silicon per square millimeter, and the number of pins per die can easily exceed the number of square millimeters per die [4], [5]. These trends highlight the need to minimize the cost associated with the packaging of faulty dies by effective testing at the wafer-level. The impact of packaging cost on the overall production cost provides a major motivation for the work presented in this paper.

Despite the numerous benefits of testing at the wafer level, industry practitioners have reported that mixed-signal test is seldom carried out at the wafer level [3], [12]. Measurement inaccuracies are common when analog cores are tested in a mixed-signal test environment based on digital signal processing [9]. This problem is exacerbated by noisy dc power supply lines, improper grounding of the wafer probe, and lack of proper noise shielding of the wafer probe station [13]. The previous problems make test and characterization at the wafer-level especially difficult, and they can lead to high yield loss during wafer sort. Moreover, since test time is a major practical constraint for wafer sort, even more so than for package test, not all scan-based tests can be applied to the digital cores under test [14].

In this paper, we present a new correlation-based signature analysis technique for mixed-signal cores, which facilitates defect screening at the wafer-level. The proposed technique is motivated by popular outlier analysis techniques for IDD-quiescent (IDDQ) testing [15]. Outlier identification using IDDQ during wafer sort is difficult for deep-submicrometer processes [15]. This problem has been addressed using statistical post-processing techniques that utilize the test response data from the ATE [15]. We propose a similar classification technique that allows us to make a pass/fail decision under non-ideal ambient conditions and using imprecise measurements. We present a wafer-scale analog test method based on the use of low-cost digital testers, and with reduced dependence on mixed-signal testers. To the best of our knowledge, this is the first attempt to use low-cost digital testers at the wafer level for mixed-signal SoCs, without any on-chip overhead. Experimental results are presented for an industrial mixed-signal SoC.

II. WAFER-LEVEL DEFECT SCREENING: MIXED-SIGNAL CORES

Test procedures for data converters can be classified as being based on either spectral-based tests or code density tests. Spectral-based test methods [16] usually involve the use of a suitable transform, such as

Manuscript received July 24, 2007; revised December 27, 2007. First published February 24, 2009; current version published March 18, 2009. This work was supported in part by the Semiconductor Research Corporation under Contract 2004-TJ1174. A preliminary version of this paper appeared in Proc. Asia and South Pacific Design Automation Conference, 2007, pp. 823–828.

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Digital Object Identifier 10.1109/TVLSI.2008.2006075

the Fourier Transform, to analyze the output. These methods are used to determine the dynamic test parameters of the data converter. On the other hand, code density tests are based on the constructions of histograms of the individual code counts [17]. The code counts of the data converter-under-test are then analyzed and compared with the expected code counts to determine its static parameters. Recent work in mixed-signal testing has focused on spectral-based frequency domain tests, due to the inherent advantage of test time over the code density tests. In [16], a test flow process is described, that uses only the dynamic tests. A case study on sample data converters presented in [16] claims that 96% of faults involving both static and dynamic specifications can be detected without using the code density test technique. It is important to note that the procedure described in [16] is aimed at production testing. In [18], it has been shown that frequency-domain-based signature analysis helps in suppressing non-idealities associated with the test data, and it serves as a robust mechanism for enhancing fault coverage and reducing false alarms.

A mixed-signal path can be sandwiched between a pair of complementary data converters to generate a virtual mixed-signal core driven by digital inputs and outputs [9]. Testing this mixed-signal path, which is a basic building block in most "big-D/small-A" SoC designs, holds key to cost effective testing using low cost digital testers. The inadequacy of analog tests and their lack of effectiveness at wafer sort to accurately measure test parameters and identify faulty dies have been highlighted in [3] and [12]. A new defect screening technique for mixed-signal cores at wafer sort is needed for the following reasons.

- Time-domain signature analysis techniques have extremely low tolerance to noise, since the measured signature can be incorrect even for single bit errors [19].
- Noisy signals and imprecise test clocks at wafer sort lead to distortion in the value of the dynamic parameters of such a signal-to-noise ratio (SNR), which directly affect the effective number of bits for the data converter. The lower-order bits of the data converter, in the presence of noise, convert noise rather than the signal itself. In such circumstances, the comparison of the data converter with a prespecified signature inevitably leads to increased yield loss.
- Test signals which are more linear than the linearity of the device under test (DUT), are prescribed as a requirement for successful testing of data converters [20]. This cannot be guaranteed in "big-D/small-A" SoC designs, as the digital-to-analog converters (DACs) are used to provide test stimuli to the analog-to-digital converters (ADCs), when configured in a loop-back mode.

Measurement inaccuracies associated with a mixed-signal test and measurement environment are described in [9] and [13]. These problems can lead to a degradation in the quality of the measurements made; these effects are more pronounced at wafer sort [12], [13]. As a result, yield loss and test escape are more likely at the wafer-level.

Test procedures examine the output response of the circuit and compare it to a predetermined "acceptable" signature. In light of all the possible error sources during wafer sort, a reliable acceptable signature is hard to derive because it requires the modeling of all possible errors. To address the previous problems, outlier analysis has been extensively used in IDDQ testing of digital circuits [15]. We employ a similar pass/fail criterion in the proposed wafer-level testing approach. To perform such an analysis, we first require a measurable parameter for each core. In IDDQ testing, this data comes in the form of supply current information. However, in spectral analysis, the information obtained as a signature is spread over multiple data points, where each data point represents the power associated with the corresponding frequency bin. It is therefore necessary to encode this information as a single parameter corresponding to each individual core. We propose two correlation-based test methods to achieve this goal. These methods are referred to as the *mean-signature-* and *golden-signature*-based correlation techniques. Two complementary data converters connected in a loopback configuration in the test mode can be applied with a digital test stimuli (usually a multi-tone sinusoidal signal) at the DAC input interface; this results in a digital signature (test response) at the output interface of the ADC.

The contribution of this paper lies in the use of a suitable correlation-based signature analysis technique (mean- or golden-signature) to identify faulty die in a sample population. In a typical "big-D/small-A" SoC, there is at least one pair of data converters that can be used for measurements. Our defect screening technique does not have any specific requirement on the resolution of the data converters. The defect screening technique also needs only digital test stimuli and generates purely digital test signatures. Due to the non-idealities at wafer sort [12], [13], complete and accurate characterization of the devices is not possible. Our methodology does not involve any specification-based testing. Accurate specification-based testing (involving accurate spectral analysis, power measurement, etc.) will necessitate modification of the on-chip test infrastructure (e.g., increasing the bit resolution of the data converters). Since our work does not require any of the above, it is strictly limited to wafer sort testing of "big-D/small-A" SoCs, where the objective is to screen as many defective die as possible while keeping yield losses to a minimum.

A. Signature Analysis: Mean-Signature-Based-Correlation (MSBC)

In [18], Acar and Ozev use the correlation between a reference spectrum and the spectrum of the circuit under test as a pass/fail criterion. The reference spectrum serves as an acceptable signature, and is used for comparison with the spectrum of the circuit under test. Such a reference signature is called an Eigen signature [18]. The sensitivities to changes in the shape of the spectrum of the device-under-test from the Eigen signature can be quantified by means of a correlation parameter. The correlation is a fraction that lies between 0 and 1, and it serves as a single measurable parameter for each individual die.

The characteristic spectrum X_i of the ith core-under-test in a batch of m identical cores is obtained using a P-point fast Fourier transform (FFT) and is defined as: $X_i = \{x_{i1}, x_{i2}, \ldots, x_{iP}\}$, $1 \leq i \leq m$. The elements $x_{i1}, x_{i2}, \ldots, x_{iP}$ in the previous spectrum denote the power associated with the corresponding frequency bin. Ideally, the spectrum of each die should be correlated to a set of averages of the spectra of m dies tested under similar ambient operating conditions. The Eigen signature E is determined as the set of averages of the spectra of m identical cores-under-test and can be defined as: $E = \{(\sum_{i=1}^{m} x_{i1})/m, (\sum_{i=1}^{m} x_{i2})/m, \ldots, (\sum_{i=1}^{m} x_{iP})/m\}$. In particular, if the number of good dies is appreciably larger than the number of defective ones, the Eigen signature contains the information needed to classify the good dies from the defective ones. Since both X_i and E are random variables, let $\overline{X}_i$ and $\overline{E}$ represent the mean of X_i and E, respectively. The correlation between the Eigen spectrum and that of the circuit under test can now be defined using (1) as

$$\mathrm{corr}(X_i, E) = \frac{\sum_{j=1}^{P} (x_{ij} - \overline{X}_i)\left(\frac{\sum_{i=1}^{m} x_{ij}}{m} - \overline{E}\right)}{\left[\sum_{j=1}^{P} (x_{ij} - \overline{X}_i)^2 \sum_{j=1}^{P} \left(\frac{\sum_{i=1}^{m} x_{ij}}{m} - \overline{E}\right)^2\right]^{1/2}}. \quad (1)$$

B. Signature Analysis: Golden-Signature-Based-Correlation (GSBC)

For the MSBC technique, the collection of spectral signatures requires the storage of spectral information of a number of dies before a pass/fail decision can be made. While this information does not have to reside in the main memory of the tester, storing and handling such a large amount of data may be inconvenient. It may be desirable to use a predefined *golden-signature* for correlation during wafer sort. It is important to note that the use of a predefined spectrum as the *golden*

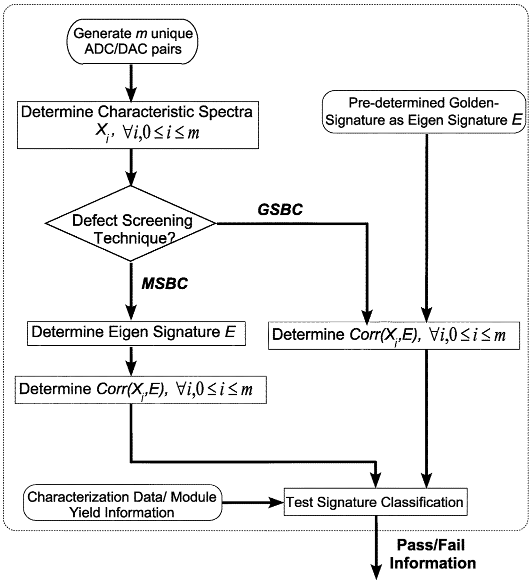

Fig. 1. Flowchart depicting the mixed-signal test process for wafer-level fault detection.

TABLE I

WAFER-LEVEL DEFECT SCREENING: EXPERIMENTAL RESULTS FOR AN 8-BIT FLASH ADC

Correlation Technique	FFT: No. of Sample Points-Yield Type	YL (%)	OTE (%)	TE_{MaF} (%)	TE_{MoF} (%)	TE_{GF} (%)	k
Mean Signature	1024-LY	0.8176	46.66	89.25	33.21	3.53	5
	1024-MY	0.25	67.7	97.11	66.19	0	7
	1024-HY	0.9	49	95.23	54	7.4	7
	4096-LY	0.06	47	77.1	7.95	0	10
	4096-MY	0.08	27.43	58.65	12.67	0	10
	4096-HY	0	25	95.23	10	0	10
Golden Signature	1024-LY	1.006	75.71	98.59	73.7	42.47	5
	1024-MY	0.0375	68.75	96.15	67.6	5	7
	1024-HY	1.1	74	100	76	55.55	5
	4096-LY	0.18	29.78	88.31	7.95	0.88	8
	4096-MY	0.16	43.36	96.15	15.49	0	10
	4096-HY	0.1	2.5	100	8	0	10

$\mathrm{YL} \rightarrow \mathrm{Yield\ loss;\ OTE} \rightarrow \mathrm{Overall\ test\ escapes;\ TE}_{MaF}$; TE_{MoF} and TE_{GF} → Test escapes for marginal; moderate and grossly faulty dies, respectively.

signature does not hamper outlier analysis. The *golden-signature* spectrum is obtained *a priori*, by assuming ideal and fault-free operating conditions for the circuit under test. The correlation parameter can still be used to identify the possible faulty dies. The correlation parameters are estimated in the same way as in Section II-A. The only difference here lies in the use of a *golden signature* as the Eigen signature. The test flow for both methods is described in Fig. 1.

The next step in signature analysis is to set a threshold to determine the pass/fail criterion for each die. As explained previously, due to all the non-idealities in the measurements, a predetermined threshold is of little use. However, during wafer sort, characterization data on mixed-signal components is already available. The characterization data provides information on the approximate percentage of dies that are expected to pass the final test. Modular testing of SoCs can also provide information on the approximate yield per module/core in an SoC [21]. Characterization information, in conjunction with the module yield data, can be used to estimate *a priori*, the approximate number of dies that will pass the test. The yield loss due to this indirect testing method should be minimized, since yield loss affects overall cost by increasing the effective cost of silicon per unit die. The number of passing dies can be estimated by using the expected yield $(Y_{\%})$ information from the characterization data. We set the fraction of the number of dies passing the test to be $Y_{\%} + ((100 - Y_{\%})/k)$. The constant k determines the number of die that pass the test during wafer sort. The value of k in our work is chosen based on the type of signature analysis technique; the choice of k is made appropriately to minimize the yield loss (at the cost of increased test escapes) during wafer sort. The values of k used in our experiments are reported in Table I.

C. Experimental Results

The effectiveness of the proposed methods can be established by determining the resultant yield loss and test escapes. If G represents the number of good circuits and G_{fail} the number of good circuits failing the test, then the yield loss can be estimated to be G_{fail}/G. The number of faulty circuits that pass the test (F_{pass}) can be used to calculate the test escapes as $F_{\mathrm{pass}}/(N - G)$.

To evaluate the previous performance metrics, we develop a behavioral model of a flash-type ADC [10] in MATLAB. We generate 1500 unique circuit instances of the ADC by inducing parametric variations in the associated components and also by injecting certain hard and soft failure types. The hard failure type corresponds to catastrophic failures and the soft failure type corresponds to parametric variations that result in undesirable circuit operation. The hard faults are generated for 100 data converters by forcing resistive opens and broken lines in the comparator network. We then vary the component parameters; the values of resistors; and the offset voltages of the comparators, to generate three sets of data converters. We modify the standard deviations of resistor values and offset voltages to randomly inject the soft faults. The three sets of data converters correspond to high yield (HY-90%), moderate yield (MY-75%), and low yield (LY-60%). Correlation parameters for each unique ADC are obtained for both the proposed methods and by using a 1024-point and a 4096-point FFT. In this experiment, the specification that determines the good/faulty dies is the differential-nonlinearity (DNL) parameter. The acceptable range of DNL for the ADC is set to be $0 \le \mathrm{DNL} \le 0.5$. Based on the random fault injection scheme, we have a number of marginally faulty dies $(0.5 \le \mathrm{DNL} \le 1)$, moderately faulty dies $(1 \le \mathrm{DNL} \le 2)$ and grossly faulty dies $(\mathrm{DNL} > 2)$. The percentages of marginal, moderate and grossly faulty data converters in the overall population are 44%, 37%, and 19%, respectively.

We present experimental results for the 8-bit flash ADC model in Table I. It is clear that the MSBC technique outperforms the GSBC technique in most cases, both in terms yield loss (YL) and overall test escapes (OTE). Table I lists the percentage of test escapes for marginal $(\mathrm{TE}_{\mathrm{MaF}})$, moderate $(\mathrm{TE}_{\mathrm{MoF}})$, and grossly $(\mathrm{TE}_{\mathrm{GF}})$ faulty dies. The percentages are given in terms of the number of faulty dies in each group). Columns 5–7 list the relevant data separately for each fail type. As a result, the rows of the table for these three columns do not add up to 100%. This analysis is performed in order to evaluate the effectiveness of our proposed signature analysis techniques over different failure regions. A significant percentage of marginal failures result in test escapes. This shows that the proposed signature analysis technique is not effective for screening marginal failures. On the other hand, 33%–92% and 26%–92% of the moderately faulty dies are screened in the case of the MSBC technique and GSBC technique, respectively. Thus, our technique is effective for screening moderate and gross failures, which is typically the objective in wafer-level testing. Marginal failures are best detected at package test, where the chip can be tested in a more comprehensive manner.

III. COST MODEL: QUANTITATIVE ANALYSIS

In [22], a cost model to evaluate wafer-level testing for a generic mixed-signal SoC was presented. The cost model in [22] modeled the precise relationship between yield loss, test escape and the overall product cost. The effects of yield loss and test escape for both the digital and mixed-signal cores in an SoC were also considered in [22].

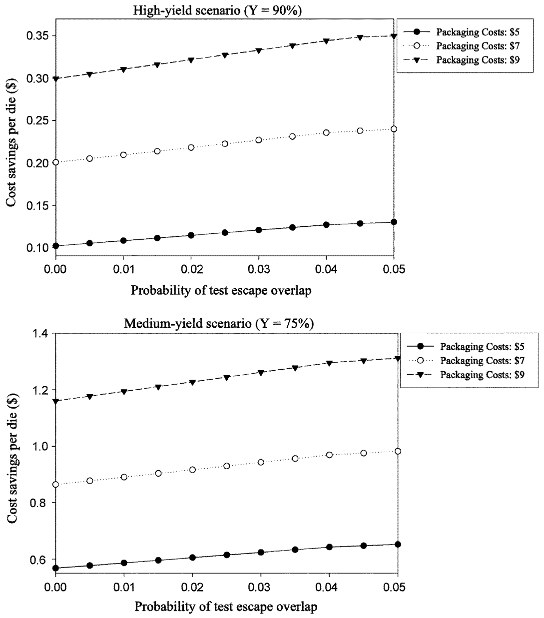

Fig. 2. Distribution of cost savings for a large die with packaging costs of (a) \$5, (b) \$7, and (c) \$9 when test escapes between digital and analog parts are correlated.

In this section, we use the model to validate the importance of wafer-testing from a cost perspective. In order to use the cost model, we need realistic values of the cost components used in the model. For this purpose, we model the section of flattened digital logic (as in [22]) as a single core, and use relevant information from a commercial mixed-signal SoC, Chip U.[1] The mixed-signal SoC includes a pair of complementary data converters of identical bit-resolution. The data converters can be configured in such a way that each DAC is routed through the ADC for purposes of test (as explained in Section II). It is appropriate to assume that the ADC and the DACs are tested as pairs because a single point of failure is a sufficient criterion to reject the IC as being faulty.

We model the test escapes by assuming that the digital portion application-specific integrated-circuit (ASIC) Chip K is tested with 4046 test patterns, and for which the test escape correction factor is determined from [22]. The analog test time is modeled by assuming that the data converter pair is tested with a 4096-point FFT. The test escape of the mixed-signal portion of the chip is assumed to be 50%; this is significantly higher than the average value of overall test escape rate presented in Table I.

The work in [22] illustrated the distribution in cost savings for small, medium and large die with varying packaging costs. However, in [22] the results did not consider the impact of failures due to both the digital and mixed-signal cores. In a typical "big-D/small-A" SoC, the digital and mixed-signal portion of the die are placed close to one another. A defect that causes a fail in the digital portion of the die is likely to cause a defect in the mixed-signal portion of the die; depending on the size and nature of the defect. The impact of the distribution of the mixed-signal fail types (percentage of marginal, moderate and gross failures) on cost savings were also not considered in [22].

A. Cost Savings: Results Considering Failures Due to Both Digital and Mixed-Signal Cores

We now evaluate the cost savings when the digital and the analog fails are correlated. Let A denote the event of a mixed-signal test escape and B denote the event of a digital test escape. A test escape in either the mixed-signal portion of the die, or in the digital portion of the die will result in the part being packaged. The probability that the test process results in at least one test escape can be given as $P(A \cup B)$; this probability can be represented using the following equation:

$$P(A \cup B) = P(A) + P(B) - P(A \cap B). \qquad (2)$$

TABLE II
EXPERIMENTAL RESULTS FOR COST SAVINGS CONSIDERING FAILURE TYPE DISTRIBUTIONS FOR MIXED-SIGNAL CORES

Yield Type	Distribution: {Marginal, Moderate, Gross} Failures (%)	FFT: No. of Sample Points	TE_{MSBC} (%)	CS_{MSBC} (in \$)	TE_{GSBC} (%)	CS_{MSBC} (in \$)
Low Yield (60%)	{33.33,33.33,33.33}	1024	42.79	1.6867	72.01	0.702
		4096	29.3	2.1333	32.99	2.009
	{70,15,15}	1024	68.42	0.8227	86.65	0.2084
		4096	55.78	1.24	63.65	0.9744
	{15,70,15}	1024	38.02	1.8472	73.26	0.6597
		4096	18.27	2.5057	20.45	2.4454
	{15,15,70}	1024	21.92	2.3898	56.21	1.2343
		4096	13.95	2.6513	16.26	2.5733
Medium Yield (75%)	{33.33,33.33,33.33}	1024	55	0.3867	56.79	36.86
		4096	24.82	0.685	38.04	0.5509
	{70,15,15}	1024	78.21	0.1519	78.49	0.149
		4096	43.74	0.4932	70.04	0.2265
	{15,70,15}	1024	61.44	0.3216	63.01	0.3051
		4096	18.79	0.746	26.29	0.67
	{15,15,70}	1024	25.53	0.6848	29.05	0.6492
		4096	11.92	0.8157	17.89	0.7552
High Yield (90%)	{33.33,33.33,33.33}	1024	52.81	0.0258	76.73	-0.0011
		4096	35.93	0.0381	59.96	0.018
	{70,15,15}	1024	76.2	-0.0005	89.87	-0.0159
		4096	68.6	0.001	82.25	-0.0145
	{15,70,15}	1024	53.84	0.0247	76.85	-0.0013
		4096	22.36	0.0535	71.4	-0.0021
	{15,15,70}	1024	28.56	0.0532	65.76	0.0113
		4096	16.94	0.0596	28	0.0471

TE_{MSBC} and TE_{GSBC} → Overall test escape rate for the SoC using MSBC and GSBC; $\text{CS}_{\text{MSBC}}$and CS_{GSBC} → Cost savings per die using MSBC and GSBC.

Prior work [22] considered a scenario where the test escapes occurring in the different sections of the die were independent. The product of the individual test escape probabilities were therefore used to determines the resultant test escape. We now consider a scenario where test escapes occur in both parts of the die simultaneously, i.e., when a test results in a test escape in the digital portion of the die, the mixed-signal test also results in a test escape. This is given by the probability $P(A \cap B)$. In our experiments, we consider test escape values by varying $P(A \cap B)$ between 0 and $\min\{P(A), P(B)\}$ to determine the test escape probability from (2). The values of $P(A)$, $P(B)$, and the various costs associated with the test and packaging process considered here are the same as in [22]. The purpose of this experiment is to determine the impact, on the overall cost savings, of test escapes that occur in both the digital and mixed-signal portions of the die.

We now present experimental results for a large die under two different yield scenarios: high yield [see Fig. 2(a)] where the yield is 90% and medium yield [see Fig. 2(b)] where the yield is 75%. The x-axis denotes the probability of test escape overlap; the overlap in test escape is varied from 0 to the test escape probability of digital cores (0.05 for Chip U). It is observed from Fig. 2 that our defect screening technique results in cost savings despite the overlap in test escapes in the digital and mixed-signal cores. The cost savings are minimum when there is no overlap in test escapes between the digital and mixed-signal cores, and vice-versa. Similar results are obtained for small and medium dies.

B. Cost Model: Results Considering Failure Distributions

The results in [22] did not consider the breakdown between the various mixed-signal fail types. The percentage of marginal, moderate and gross failures can be determined via statistical binning of failure information for a given batch of dies being manufactured. Unfortunately, such failure data is not easily available in the literature; companies are reluctant to disclose this information. Therefore, we con-

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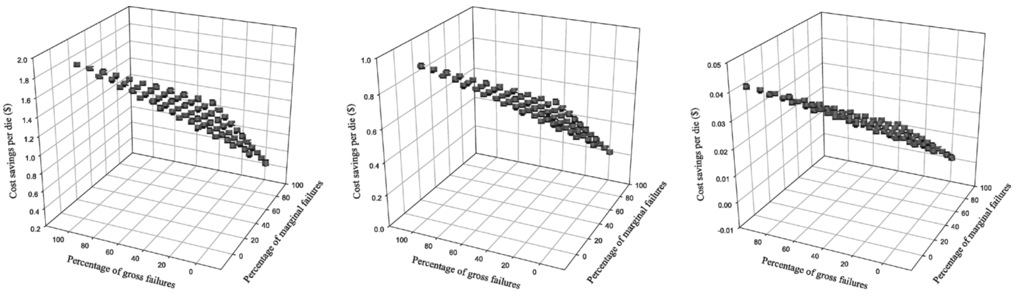
[1] ASICs Test Methodology, IBM Microelectronics, Essex Jct, VT 05452.



(a) (b) (c)

Fig. 3. Variation in cost savings considering the impact of mixed-signal fail types. (a) Low-yield scenario. (b) Medium-yield scenario. (c) High-yield scenario.

sider different scenarios and a range of values for the percentages corresponding to the different failure types. Let x_1, x_2, and x_3 represent the percentage of failures corresponding to marginal, moderate and gross fail types, and TE_1, TE_2, and TE_3 be their corresponding test escape rates. The test escape for the analog cores can now be calculated as: $(\mathrm{TE}_1 \cdot x_1 + \mathrm{TE}_2 \cdot x_2 + \mathrm{TE}_3 \cdot x_3)/(x_1 + x_2 + x_3)$.

We first consider the following cases: 1) all the fail types are equally distributed; 2) the marginal fail type dominates the sample fail population; 3) the moderate fail type dominates the sample fail population; 4) the gross fail type dominates the sample fail population. In the case of a particular fail type dominating the sample fail population, we assume that the other two fail types make equal contributions to the number of failing dies. Table II illustrates the previous four cases; it is assumed here that the digital core in the SoC is tested with 4046 digital test patterns. The packaging costs are chosen according to the yield type considered. We consider a packaging cost of $5 for the low yield case, since the low yield case nominally corresponds to large dies. Similarly, we consider packaging costs of $3 and $1 for the medium and high yield cases respectively. The die areas considered are, 10, 40, and 120 mm^2, corresponding to low, medium, and high yield. A constant yield loss of 1% for all test cases is considered. The percentage test escapes corresponding to failure type, are obtained using behavioral simulations (see Table I) for all yield cases. The choices of packaging costs reflect the lower bounds from the values considered in Section III-A. We assume here that the digital and mixed-signal fails are uncorrelated, due to the lack of representative information. In practice, as discussed in Section III-B, the correlation information can be easily incorporated in the cost model if it is available for failing dies.

Table II presents results obtained using the cost model for the different cases described above. We present results for both the MSBC- and the GSBC-based techniques. The purpose of this experiment is to relate the importance of the proposed wafer-level defect screening techniques to the dominance of a particular fail type. It is obvious that a sample population with a high marginal fail type will result in a high overall test escape rate for the SoC ($\mathrm{TE}_{\mathrm{MSBC}}$ and $\mathrm{TE}_{\mathrm{GSBC}}$). On the other hand, the test escape rate will be low for the gross fail type. Table II shows that irrespective of the distribution of fail types, wafer-level testing reduces cost in most cases. The use of the MSBC-based technique results in greater cost savings ($\mathrm{CS}_{\mathrm{MSBC}}$), compared to the GSBC technique ($\mathrm{CS}_{\mathrm{GSBC}}$). For a process known to have high yield, wafer-level testing does not always reduce test and packaging costs. The negative entries in Table II provide a reality check on the extent to which wafer-level tests should be applied. These results help us to judiciously determine the extent of wafer testing for different scenarios. The GSBC technique is inefficient for testing in a high-yield production environment, which typically corresponds to the manufacture of small dies. It is more suitable for low- and medium-yield dies.

We next vary x_1, x_2, and x_3, each between 0 and 100, under the constraint that $x_1 + x_2 + x_3 = 100$. The resulting cost savings are shown in Fig. 3. The three axes in Fig. 3 denote the percentage of marginal failures (x_1), the percentage of gross failures (x_3), and the cost savings per die, respectively. (The percentage of moderate failures, x_2, is derived from x_1, and x_3.) Results are presented for three different yield scenarios: low, medium, and high yield; MSBC is used as the defect-screening technique for the results presented in Fig. 3. It is observed that cost savings are the least when marginal failures dominate the fail population. Similarly, a fail population with significant gross failures result in high cost savings per die. As expected, the cost savings for moderate failures lies between the cost savings for marginal and gross failures. Similar results are observed when GSBC is used instead of MSBC.

IV. CONCLUSION

We have proposed a wafer-level defect screening technique for core-based mixed-signal SoCs. Two new correlation-based signature analysis methods have been presented for wafer-level testing of analog cores. We use the cost model presented in [22] to quantify the savings that result from wafer-level testing. Test escape, yield loss, and packaging have been incorporated in this production cost model. We have used an industrial mixed-signal SoC to evaluate the proposed wafer-level test method. The proposed method uses a low-cost digital tester for wafer-level mixed-signal test, which further reduces test cost.

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