JOURNAL OF ELECTRONIC TESTING: Theory and Applications 20, 611–622, 2004
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A Signature Analysis Technique for the Identification of Failing Vectors with Application to Scan-BIST*

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Received March 27, 2003; Revised February 28, 2004

Editor: S.N. Demidenko

Abstract. We present a new technique for uniquely identifying a single failing vector in an interval of test vectors. This technique is applicable to combinational circuits and for scan-BIST in sequential circuits with multiple scan chains. The proposed method relies on the linearity properties of the MISR and on the use of two test sequences, which are both applied to the circuit under test. The second test sequence is derived from the first in a straightforward manner and the same test pattern source is used for both test sequences. If an interval contains only a single failing vector, the algebraic analysis is guaranteed to identify it. We also show analytically that if an interval contains two failing vectors, the probability that this case is interpreted as one failing vector is very low. We present experimental results for the ISCAS benchmark circuits to demonstrate the use of the proposed method for identifying failing test vectors.

Keywords: algebraic analysis, fault diagnosis, intervals of test vectors, linearity, MISR

1. Introduction

As feature sizes of integrated circuits (ICs) shrink and designs increase in complexity, built-in self-test (BIST) and scan design are being increasingly accepted as industry-wide test solutions [6]. The combination of scan design and BIST, commonly referred to as scan-BIST, is now especially common. A scan-BIST

*This research was supported in part by the AZTEKE project of the BMFB, Germany. The work of K. Chakrabarty was also supported in part by a fellowship from the Alexander von Humboldt Foundation, Germany. A preliminary and abridged version of this paper appeared in *Proc. 6th International Workshop on Design and Diagnostics of Electronic Circuits and Systems*, pp. 81–86, Poznan, Poland, April 14–16, 2003.

technique typically applies a large number of pseudo-random patterns to the circuit under test via internal scan chains. The responses are then captured by the scan chains and compacted to a short signature in a multiple-input signature register (MISR) [3]. The properties of MISRs and their effectiveness for response compaction have been studied extensively in the literature [12, 18, 21, 25, 28]. However, a drawback of this approach is that the compact signature provided by the MISR provides only limited information for fault diagnosis, either to determine (failing) test vectors that produce errors on observable outputs or to identify error-capturing (failing) scan cells.

Fault diagnosis is essential not only for the identification of manufacturing defects, but also for yield learning. In addition, fault diagnosis during silicon debugs is useful for design error detection. The cost of diagnosis is usually determined by the total time required for test application, identification of failing vectors and scan cells, fault localization, and failure analysis. For a scan-BIST scheme involving millions of vectors and tens of thousands of scan cells, the diagnosis and failure analysis time can be extremely high. Due to the large numbers of test vectors and scan cells, it is often difficult to determine a small set of failing vectors and failing scan cells that can be used for failure analysis. The diagnostic accuracy provided by a typical scan-BIST scheme is therefore too low to be useful in practice [26]. Hence, there is a need for scan-BIST schemes that offer high diagnostic accuracy, i.e., they provide a small set of failing vectors and failing scan cells, without requiring excessive test application time, processing time, and additional on-chip hardware.

Diagnosis in a scan-BIST environment can be broadly classified as either time diagnosis or space diagnosis. *Time diagnosis* refers to the identification of the set of failing testing vectors in a BIST session. *Space diagnosis* refers to the identification of failing (error-capturing) scan cells. A number of space diagnosis techniques have been proposed in the literature [4, 5, 23, 29]. These techniques provide a small set of candidate failing scan cells out of the tens of thousands of scan cells in large ICs.

A more difficult problem in scan-BIST diagnosis is that of identifying the set of failing vectors. This is because the number of test vectors applied to the circuit under test in a typically BIST scheme is usually much larger than the length of a scan chain. As a result, even fewer practical techniques are available today for rapidly identifying a small set of candidate failing vectors. Early work on failing vector identification was based on the analysis of LFSR sequences [20], and the use of cycling registers [24] and error-correcting codes [11, 17]. An alternative approach that does not require intermediate signatures was presented in [1]. These techniques suffer from several drawbacks, including limitations on error multiplicity and restriction to a single-bit response stream [20], diagnostic aliasing [11, 17, 24], and high overhead [1, 11]. A promising matrix-based approach for identifying failing vectors is presented in [7]. However, it makes several simplistic assumptions, e.g., it limits the number of erroneous channels driving the MISR and the number of errors per MISR channel. Recently, a method based on the combination of cycling registers and pruning techniques was proposed for failing vector identification [15]. While this approach is useful for narrowing down the set of candidate failing vectors, it suffers from the drawback that it cannot identify all failing vectors.

An elegant analytical technique for identifying failing vectors is described in [13]. This method takes advantage of the availability of efficient public-domain numerical software tools; the computation time for this method can be reduced through the use of appropriately-chosen signature register polynomials. A potential drawback of this approach however is that it may identify a large number of candidate failing vectors. The principle of superposition is first used in [8, 9] for identifying failing vectors. Failing vector identification is also the focus of [14], where a MISR and a second device consisting of T-flip-flops are together used to determine the location of a single error vector in a stream of n response vectors of m bits each, as well as the m-bit error vector. While the MISR generates a signature based on signature analyis, the second output compactor consists of T-flip-flops that are not connected to each other. Since only a single test vector is assumed to fail, the modulo-2 difference between the signatures of the T-flip-flops for the correct test response and the erroneous response is equal to the error vector E corresponding to the test response sequence. To determine the position of the failing vector in the test sequence, the initial state of the m-bit MISR is chosen to be the state that is reached after the test response stream of n m-bit vectors is compacted, followed by a sequence of $2^m - 1 - n$ m-dimensional all-0 vectors provided as input to the MISR. With this initial state, the state E is reached after N cycles of the all-0 vector is applied to the MISR, where N denotes the position of the failing vector in the test sequence.

In other related prior work, erroneous frames of scan cells can be identified [30], where the ith frame consists of the ith scan cells of all N scan chains. The scan chains are connected to two MISRs, one of which is programmable, and in every repetition of the test set, the programmable MISR has to implement a different primitive polynomial. In order to identify up to t erroneous frames, $2t$ signatures for the complete test set are needed. In addition, to localize the failing scan cells, every scan chain must be considered separately. For a large number of scan chains, this approach imposes time overhead, as well as area overhead due to the need to modify the scan-BIST architecture.

A recent technique for failing vector identification relies on the use of overlapping intervals of test vectors [19]. An interval is a set of consecutive test vectors. A separate BIST signature is determined for each interval to determine is pass/fail status. An advantage of this approach is that all failing vectors are included in a reduced set of candidate vectors for failure analysis. The overlap allows effective pruning the set of candidate failing vectors with low hardware overhead. An interval that does not contain a failing vector can be omitted from the set of candidate failing vectors. Despite these advantages, the interval-based approach of [19] suffers from the drawback that a larger number of non-failing vectors are often included in the set of candidate failing vectors.

In this paper, we present a new technique for uniquely identifying a single failing vector in an interval for combinational circuits and for sequential circuits with multiple scan chains. As in [14], this approach is based on an algebraic analysis of the signatures captured in the MISR during a BIST session. The algebraic analyis is based on the well-known theory of shift-register sequences as described in detail in the literature [3, 16, 27, 31–33]. Instead of demonstrating how to apply this methodology in practical situations, the emphasis of this paper is on the theory underlying the method. The analysis relies on the linearity properties of the MISR, and on the use of two test sequences, where the second test sequence is derived from the first in a straightforward manner. The same test pattern source is used for both test sequences. If an interval contains only a single failing vector, the algebraic analysis is guaranteed to identify it. In addition, we show that if the interval contains two (or more) failing vectors, the probability that this pair of failing vectors is misinterpreted as a single failing vector is extremely low. The proposed method can be used with a standard STUMPS-like BIST architecture.

The proposed approach is based on a classification of faults on the basis of their ease of detection using pseudorandom patterns. This approach is not intended for the "easy faults" that are detected by a large number of test patterns. The benefit of the proposed approach for such faults is limited because they require very short intervals. The focus here is on faults that cause only a few failing vectors within an interval. The identification of these failing vectors and the underlying faults imposes an onerous burden on the failure analysis engineer. We show through simulation experiments that the ISCAS benchmark circuits contain a large number of such single stuck-at faults, therefore the proposed analysis technique for identifying single failing vectors within an interval can reduce diagnosis time significantly. Once a failing interval is identified, the test vectors in the interval can be either applied from the tester or from a BIST pattern source. A set of appropriate interval lengths can be determined through preprocessing on the set of faults that are targeted by this approach. In addition to facilitating effect-cause analysis, the proposed approach can also benefit cause effect analysis [10]. For example, the knowledge of candidate failing vectors can improve the resolution provided by a compact fault dictionary [22].

An inefficient approach to identify a failing test vector in a failing interval is to apply the vectors in that interval, and bypass the MISR and download all the test responses captured in the scan chains. To see what this entails, consider a design with 500 scan chains and 200 scan cells per scan chain. If the interval contains 200 test vectors, the total volume of test response that must be used to identify a failing test vector is as large as 20 Mbits. Even though diagnosis is done off-line, this amount of test data volume for a typical design imposes a severe burden on ATE memory for on-tester diagnosis, and workstation memory for off-tester diagnosis. In the proposed method, the failing vector is identified by examining only the MISR signature at the end of the test session, and even though the test patterns are applied twice (as explained in the next section), the volume of test response data is only 1 Kbits.

The organization of the paper is as follows. In Section 2, we describe the algebraic technique for identifying failing vectors in an interval for combinational circuits. In Section 3, we extend the algebraic analysis to a full-scan BIST environment with multiple scan chains. In Section 4, experimental results are provided

for the ISCAS-85 and the ISCAS-89 benchmark circuits. Finally, Section 5 presents conclusions.

2. Failing Vector Identification Using MISR Signatures

In this section, we describe the algebraic analysis technique that allows us to determine the failing vector in an interval from the signature generated by the MISR. We consider combinational circuits here, and extend the analysis to full-scan designs in the next section.

Suppose a sequence of test vectors $t^1, t^2, \ldots t^n$ is applied to the circuit under test; see Fig. 1. (The masking logic is described later.) We refer to this sequence of k-bit vectors as an interval of length n. Let the corresponding sequence of m-bit test response vectors be $y_1, y_2, \ldots y_n$, and let the MISR signature for this response sequence be denoted by $S(y_1, y_2, \ldots y_n) = S(1 \rightarrow n)$. Let the initial state of the MISR be $\underline{0}$, the all-zero vector.

Next, suppose that a fault φ in the circuit under test changes the fault-free response y_i to the faulty response $y_i \oplus e_i$, where e_i is the error vector. Since we are assuming that only one test vector fails in an interval, all the other test response vectors are fault-free, i.e. $e_j = \underline{0}, j \neq i$. The erroneous signature corresponding to an error for the ith test vector, denoted $S(1 \rightarrow n, i, e_i)$ is given by

$$\begin{aligned} &S(1 \rightarrow n, i, e_i) \\ &\quad = S(y_1, y_2, \ldots y_{i-1}, y_i \oplus e_i, y_{i+1}, \ldots, y_n) \\ &\quad = S(y_1, y_2, \ldots, y_{i-1}, y_i, y_{i+1}, \ldots, y_n) \\ &\qquad \oplus S(\underline{0}, \ldots, \underline{0}, e_i, \underline{0}, \ldots, \underline{0}) \\ &\quad = S(1 \rightarrow n) \oplus \Delta S_1(i, e_i) \end{aligned}$$

where $\Delta S_1(i, e_i)$ is the difference between the MISR signature obtained for the fault-free circuit and the MISR signature for the faulty circuit with the test sequence $t^1 t^2 \ldots t^n$.

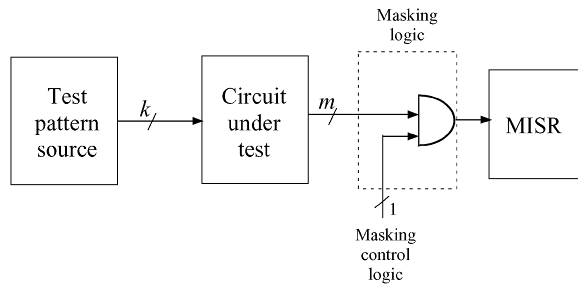

Fig. 1. Signature analysis for a combinational circuit.

Let the state transition matrix of the m-bit MISR be A. For the simplicity of presentation, we assume here that the MISR has a primitive feedback polynomial and that the inverse $\mathbf{A}^{-1}$ of the state transition matrix A exists. The next-state equation of the MISR, as described in [3, 16], is given in general terms by

$$z(t+1) = \mathbf{A}z(t) \oplus y(t) \tag{1}$$

where $z(t)$, $z(t+1)$ and $y(t)$ are m-bit vectors. Note that for notational convenience, we are using both $y(t)$ and y_t to refer to the m-bit test response vector at time instant t. Therefore, we have

$$\begin{aligned} \Delta S_1(i, e_i) &= S(\underline{0}, \ldots, \underline{0}, e_i, \underline{0}, \ldots, \underline{0}) \\ &= \mathbf{A}^{n-i} e_i, i \in \{1, 2, \ldots, n\} \end{aligned} \tag{2}$$

Next we apply every test pattern twice to the circuit under test, i.e., the test sequence is now $t^1 t^1 t^2 t^2, \ldots, t^n t 1^n$. This can be implemented by clocking the circuit twice as fast as the test pattern source. The mask control signal generates the alternating sequence 1010...1010. For this repeated sequence of test vectors, the fault-free response of the circuit under test is $y_1 y_1 y_2 y_2 \ldots y_n y_n$, and the input sequence to the MISR is $y_1 0 y_2 0 \ldots y_n 0$. The corresponding MISR signature is $S(y_1 0 y_2 0 \ldots, y_n, 0) = S(10 \rightarrow n0)$.

If the test vector t^i fails due to a fault in the circuit, the test response of the circuit is $y_1 y_1 y_2 y_2 \ldots y_{i-1} y_{i-1} y_i \oplus e_i y_i \oplus e_i, y_{i+1}, y_{i+1}, \ldots, y_n y_n$, and the corresponding signature is

$$\begin{aligned} &S(y_1, 0, \ldots, y_{i-1}, 0, y_i \oplus e_i, 0, y_{i+1}, 0, \ldots, y_n, 0) \\ &\quad = S(10 \rightarrow n0) \oplus S(\underline{0}, \underline{0}, \ldots, \underline{0}, \underline{0}, e_i, \\ &\qquad \underline{0}, \underline{0}, \underline{0}, \ldots, \underline{0}, \underline{0}) \\ &\quad = S(10 \rightarrow n0) \oplus \Delta S_2(i, e_i) \end{aligned}$$

where $\Delta S_2(i, e_i)$ is the difference between the MISR signature obtained for the fault-free circuit and the MISR signature for the faulty circuit with the test sequence $t^1 t^1 t^2 t^2 \ldots t^n t^n$. It follows from the next-state function of the MISR, Eq. (1) in this section, that

$$\Delta S_2(i, e_i) = \mathbf{A}^{2n-2i+1} e_i \tag{3}$$

Combining Eqs. (2) and (3), we get

$$e_i = \mathbf{A}^{i-n}\Delta S_1(i, e_i)$$
$$e_i = \mathbf{A}^{2i-2n-1}\Delta S_2(i, e_i)$$

which implies that

$$\mathbf{A}^{i-n-1}\Delta S_2(i, e_i) = \Delta S_1(i, e_i), \quad i \in \{1, 2, \ldots, n\} \tag{4}$$

In Eq. (4) above, A is known for the MISR, and the observed differences in MISR signatures $\Delta S_1(i, e_i)$ and $\Delta S_2(i, e_i)$ for the two test sequences are also known. Thus the value of i can be easily determined from this equation. Once i is determined, it can be used to determine e_i. Note that under the assumption that the MISR has a primitive feedback polynomial, we can always use the state space of the MISR to determine for arbitrary values of $\Delta S_1(i, e_i)$ and $\Delta S_2(i, e_i)$ a value of i, $1 \leq i \leq 2^n - 1$, such that Eq. (4) is satisfied. However, here we restrict i to lie between 1 and n, i.e. $1 \leq i \leq n$, since we are interested in the failing vector within the interval that produced the error. If no solution exists, we conclude that the erroneous signature in this case cannot be attributed to the presence of exactly one failing vector in the test sequence. Instead, the erroneous signature in this case must have been produced by more than one failing vector. In this way, we not only determine the failing vector, i.e., the location of the error in the test response sequence, but we also identify the error e_i, i.e., the outputs of the circuit under test that are in error.

Equation (4) suggests that matrix multiplication and inversion operations are necessary to determine i and e_i. This is however not necessary, and the computation can be speeded up significantly if we utilize the next-state and previous-state functions of the MISR [3, 16]. From the feedback structure of the MISR, we can easily determine the next state and previous state for every flip-flop in the MISR. Next, we set $\Delta S_2(i, e_i)$ to be the initial state of the MISR, and depending on the value of the index $i-n-1$, we calculate an appropriate number of next states or previous states. For example, if $i = n$, we calculate the previous state; on the other hand, if $i = 1$, we calculate the nth previous state and check to see if it equals $\Delta S_1(i, e_i)$.

We now illustrate the failing vector identification procedure using a small example as shown in Fig. 2. The circuit under test has four inputs x_1, x_2, x_3, x_4 and three outputs y_1, y_2, y_3. The outputs are connected via

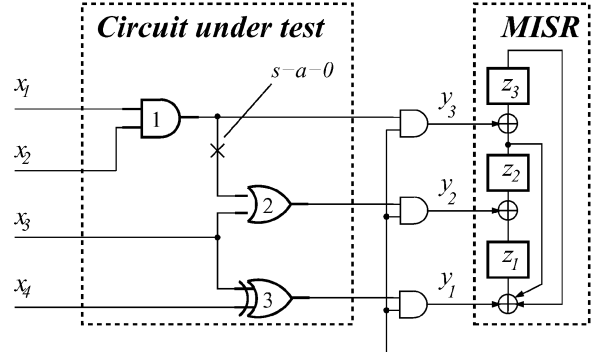

Fig. 2. Example to illustrate failing vector identification.

masking logic to the three parallel inputs of the MISR. The MISR has three stages and it has a primitive feedback polynomial. The circuit under test has three gates numbered 1 to 3.

Consider a stuck-at-0 fault on the line connecting the output of Gate 1 to an input of Gate 2. The original test sequence consists of the five (pseudorandom) test patterns $t^1 = 0010$, $t^2 = 1001$, $t^3 = 1100$, $t^4 = 0110$ and $t^5 = 1011$. The corresponding outputs y_{c1}, y_{c2}, y_{c3} and y_{f1}, y_{f2}, y_{f3} for the fault-free and the faulty circuit, respectively, as well as the accumulated signatures in the MISR are shown in Table 1. The accumulated signature for the correct circuit is 011 and the accumulated signature for the faulty circuit is 101. For the difference $\Delta S_1(i, e_i)$, we have $\Delta S_1(i, e_i) = 101 \oplus 011 = 110$.

The second test sequence consists of the ten test patterns $t^1, t^1, t^2, t^2, t^3, t^3, t^4, t^4, t^4, t^5, t^5$, where every test pattern of the original test sequence is applied twice. The control input of the masking logic is 1010101010 and in every second cycle, the input to the MISR is $\underline{0} = 000$. The corresponding test responses y_{c1}, y_{c2}, y_{c3} for the fault-free circuit under test, the test responses y_{f1}, y_{f2}, y_{f3} for the faulty circuit

Table 1. Circuit outputs and signatures for the original test sequence consisting of five patterns.

t	$t_1t_2t_3t_4$	$y_{c1}y_{c2}y_{c3}$	$y_{f1}y_{f2}y_{f3}$	$z_{c1}z_{c2}z_{c3}$	$z_{f1}z_{f2}z_{f3}$
t^1	0010	110	110	000	000
t^2	1001	100	100	110	110
t^3	1100	$\underline{011}$	$\underline{001}$	011	011
t^4	0110	110	110	010	000
t^5	1011	010	010	011	110
		$\Delta S_1 = 110$		011	101

Table 2. Circuit outputs and signatures for the derived test sequence consisting of ten patterns.

t	$t_1t_2t_3t_4$	$y_{c1}y_{c2}y_{c3}$	$y_{f1}y_{f2}y_{f3}$	$z_{c1}z_{c2}z_{c3}$	$z_{f1}z_{f2}z_{f3}$
t^1	0010	110	110	000	000
t^1	0010	000	000	110	110
t^2	1001	100	100	111	111
t^2	1001	000	000	111	111
t^3	1100	011	001	011	011
t^3	1100	000	000	010	000
t^4	0110	110	110	101	000
t^4	0110	000	000	000	110
t^5	1011	010	010	000	111
t^5	1011	000	000	010	001
		$\Delta S_2 = 001$		101	100

under test, as well as the accumulated signatures are shown in Table 2. The accumulated signature for the fault-free circuit is 101 and the accumulated signature for the faulty circuit is 100. We therefore obtain $\Delta S_2(i, e_i) = 101 \oplus 100 = 001$.

According to Eq. (4), the index i is determined with $n = 5$ as follows: $\Delta S_2(i, e_i) = (001)^T = \mathbf{A}^{n-i+1}\Delta S_1(i, e_i) = \mathbf{A}^{6-i}(110)^T$, where

$$\mathbf{A} = \begin{pmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix}$$

and $(001)^T$ and $(110)^T$ denote the transpose of (001) and (110), respectively.

Instead of multiplying the vector 011 repeatedly by A, we can use the simple shift register equations for the state components under input 0. The state successor equations are:

$$z_1(t+1) = z_2(t) \oplus z_3(t)$$
$$z_2(t+1) = z_1(t)$$
$$z_3(t+1) = z_2(t).$$

With the initial state (110), we easily compute the state sequence (110), 111, 011, 001 and for $6 - 3 = 3$, the states $(001)^T$ and $\mathbf{A}^{6-i}(110)^T$ are equal, and $i = 3$ is uniquely determined.

Next we compute the error vector e_3, which is determined as $e_3 = \mathbf{A}^{3-5}\Delta S_1(3, e_3) = \mathbf{A}^{-2}(110)^T$. Instead of matrix multiplication, we can again use the shift register equations for the state components of the MISR. The state predecessor equations are:

$$z_1(t) = z_2(t+1)$$
$$z_2(t) = z_3(t+1)$$
$$z_3(t) = z_1(t+1) \oplus z_3(t+1)$$

and with the initial state $\Delta S_1(3, e_3) = 110$, we have the predecessor state sequence 110, 101, 010 with the error vector $e_3 = \mathbf{A}^{-2}\Delta S_1(3, e_3) = 010$. It can be seen from Table 1 that indeed for the third input pattern $t^3 = 1100$, the outputs $y_{f1}, y_{f2}, y_{f3} = 001$ and $y_{c1}, y_{c2}, y_{c3} = 011$ differ by the error vector $e_3 = 001 \oplus 011 = 010$.

Recall that failing vector identification using the above procedure is guaranteed if a single test vector produces an error. We next determine the condition under which the case of two failing vectors is incorrectly diagnosed as a single failing vector. Suppose that for the test sequence $T = \{t^1, t^2, \ldots, t^n\}$, a fault causes test vectors t^i and t^j to fail, producing errors e_i and e_j, respectively. Let us assume that our diagnosis procedure interprets this pair of failing vectors as a single error e_k for the test vector t^k. This implies that $\mathbf{A}^{n-i}e_i \oplus \mathbf{A}^{n-j}e_j = \mathbf{A}^{n-k}e_k$ and $\mathbf{A}^{2n-2i+1}e_i \oplus \mathbf{A}^{2n-2j+1}e_j = \mathbf{A}^{2n-2k+1}e_k$, which leads to the following:

$$\mathbf{A}^{-i}e_i \oplus \mathbf{A}^{-j}e_j = \mathbf{A}^{-k}e_k$$
$$\mathbf{A}^{-2i}e_i \oplus \mathbf{A}^{-2j}e_j = \mathbf{A}^{-2k}e_k$$

Since k and e_k are known from the diagnosis procedure, we now determine e_i and e_j using the following equations:

$$e_i = \mathbf{A}^{i}(\mathbf{A}^{-k}e_k \oplus \mathbf{A}^{-j}e_j)$$
$$e_i = \mathbf{A}^{2i}(\mathbf{A}^{-2k}e_k \oplus \mathbf{A}^{-2j}e_j) \quad (5)$$
$$(\mathbf{A}^{i-2j} \oplus \mathbf{A}^{-j})e_j = (\mathbf{A}^{i-2k} \oplus A^{-k})e_k \quad (6)$$

Since the feedback polynomial of the MISR is assumed to be primitive, the matrix $\mathbf{A}^{i-2j} \oplus \mathbf{A}^{-j} = \mathbf{A}^{-j}(\mathbf{A}^{i-j} \oplus \mathrm{I})$ for $i - j \neq \pm 2^n - 1$ is invertible and for fixed i and j, the error e_j is determined uniquely from (6) and the error e_i is then determined uniquely from (5). For each of the $\binom{n-1}{2}$ pairs of i and j, $1 \leq i < j \leq n, i, j \neq k$, the corresponding error vectors e_j and e_i are uniquely determined by the Eqs. (6) and (5), respectively, and $\binom{n-1}{2}$ two-positional errors can be interpreted as a one-positional vector e_k in position k. The total number

of errors caused by two failing vectors is $\binom{n}{2}(2^m - 1)(2^m - 1)$, where m denotes the number of outputs in the circuit under test. If all errors are equally likely, the probability $p_{2\to 1}$ that a pair of failing vectors is misinterpreted as a single failing vector is given by

$$p_{2\to 1} = \frac{\binom{n-1}{2}}{\binom{n}{2}(2^m - 1)(2^m - 1)} = \frac{n-2}{n} \cdot \frac{1}{2^{2m} - 2^{m+1} + 1} \approx \frac{1}{2^{2m}}. \quad (7)$$

Although the assumption that all possible errors are equally likely is not realistic in practice, we conclude that it is extremely unlikely that two failing vectors will be misinterpreted as a single failing vector using this technique. If a fault is easy to detect by pseudorandom inputs, then even in short intervals we can expect several failing vectors. Therefore, we apply the proposed methods only to faults that are not easy to detect using pseudorandom patterns.

To determine the failing test vectors, we consider R test intervals $t^{1,1}, t^{1,2}, \ldots, t^{1,l}; t^{2,1}, t^{2,2}, \ldots, t^{2,l}; \ldots, t^{R,1}, t^{R,2}, \ldots, t^{R,l}$ of length l with $R \cdot l \approx 1000$. For each of these intervals we compare the expected correct signature with the actually obtained signature. If a difference between the obtained and the expected (correct) signature occurs in the jth interval, $1 \leq j \leq R$, we use the proposed method to compute the failing test vector $t^j_{i_j}$ for this interval. If no solution is found to exist with $1 \leq i_j \leq l$, we ignore this interval and conclude that a higher-positional error occurred. If there is a solution with $1 \leq i_j \leq l$, we assume that a one-positional error occurred since the probability that a higher-positional error is misinterpreted as a one-positional error is extremely low.

3. Failing Vector Identification for Scan-BIST

In this section, we extend the analysis of Section 2 to scan-BIST. We assume that the circuit under test has L scan chains, each of length M, that drive an L-bit MISR; see Fig. 3. To fill the L scan chains of length M with a test pattern X_i, the test pattern generator TPG generates L pseudorandom sequences $x_i^j = (x_{i1}^j; \ldots, x_{iM}^j)$, $j = 1\ldots, L$, of length M, and these are shifted into the L scan-chains.

When the scan-chains are filled, the test pattern is applied and the test response Y_i is captured in the L scan-chains and shifted out. Simultaneously the next test pattern X_{i+1} is generated by the TPG and shifted into the scan-chains. The test response Y_i consists of L sequences $y_i^j = (y_{i1}^j, \ldots, y_{iM}^j)$, $1 \leq j \leq L$, which are captured in the L scan-chains and shifted out. Thus the test pattern X_i and the corresponding test response Y_i can be described in a matrix form as

$$X_i = \begin{pmatrix} x_i^1 \\ x_i^2 \\ \cdot \\ \cdot \\ \cdot \\ x_i^L \end{pmatrix} = \begin{pmatrix} x_{i1}^1 & x_{i2}^1 & \cdots & x_{iM}^1 \\ x_{i1}^2 & x_{i2}^2 & \cdots & x_{iM}^2 \\ & \cdot & & \\ & \cdot & & \\ & \cdot & & \\ x_{i1}^L & x_{i2}^L & \cdots & x_{iM}^L \end{pmatrix} \quad (8)$$

and

$$Y_i = \begin{pmatrix} y_i^1 \\ y_i^2 \\ \cdot \\ \cdot \\ \cdot \\ y_i^L \end{pmatrix} = \begin{pmatrix} y_{i1}^1 & y_{i2}^1 & \cdots & y_{iM}^1 \\ y_{i1}^2 & y_{i2}^2 & \cdots & y_{iM}^2 \\ & \cdot & & \\ & \cdot & & \\ & \cdot & & \\ y_{i1}^L & y_{i2}^L & \cdots & y_{iM}^L \end{pmatrix} \quad (9)$$

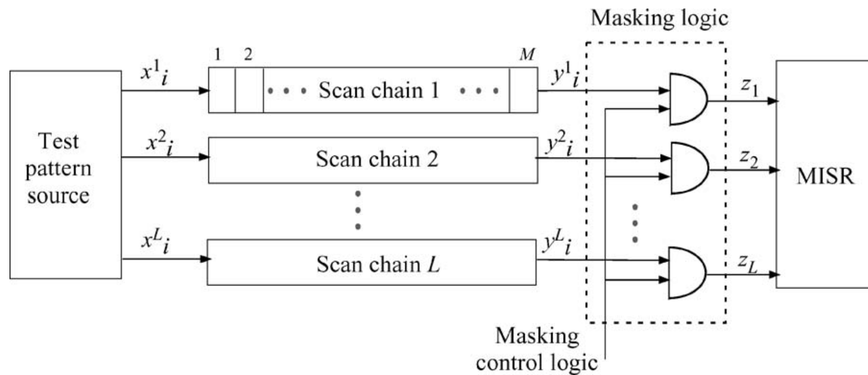

Fig. 3. Signature analysis for scan-BIST.

respectively. The state of the MISR is denoted by $z = z_1 z_2 \ldots z_L$. According to (8) and (9), the test patterns X_i and the test responses Y_i are $L \times M$ matrices consisting of M L-dimensional column vectors $(x_{i1}^1, x_{i1}^2, \ldots, x_{i1}^L)^T, \ldots, (x_{iM}^1, x_{iM}^2, \ldots, x_{iM}^L)^T$ and $(y_{i1}^1, y_{i1}^2, \ldots, y_{i1}^L)^T, \ldots, (y_{iM}^1, y_{iM}^2, \ldots, y_{iM}^L)^T$ respectively, where T denotes the transposition.

If a test sequence $X_1, X_2, \ldots, X_n$ is applied to a circuit under test with L scan-chains of length M, the test responses $Y_1, Y_2, \ldots, Y_n$ are captured in the L scan chains, given out in L data streams and compacted by the L-dimensional MISR with the linear state transition function (1) in $n \times M$ steps into a signature $S(Y_1, Y_2, \ldots, Y_n)$.

Now we assume that due a fault φ in the circuit under test, for the test input X_i an erroneous test response $Y_i \oplus E_i$ is captured in one or more of the L scan-chains, shifted out and compacted by the *MISR* into the signature $s(Y_1, \ldots, Y_{i-1}, Y_i \oplus E_i, Y_{i+1}, \ldots, Y_n)$.

Thereby we assume that only the test response $Y_i \oplus E_i$ under the test input X_i is erroneous. For all the other test inputs X_j, $j \neq i$, the corresponding test responses Y_j, $j \neq i$ are assumed to be correct. The error E_i, i.e., the difference in the test responses for the test pattern X_i can be represented in matrix form as follows:

$$E_i = \begin{pmatrix} e_i^1 \\ e_i^2 \\ \cdot \\ \cdot \\ \cdot \\ e_i^L \end{pmatrix} = \begin{pmatrix} e_{i1}^1 & e_{i2}^1 & \cdots & e_{iM}^1 \\ e_{i1}^2 & e_{i2}^2 & \cdots & e_{iM}^2 \\ & \cdot & & \\ & \cdot & & \\ & \cdot & & \\ e_{i1}^L & e_{i2}^L & \cdots & e_{iM}^L \end{pmatrix}$$

Since the MISR is a linear automaton with the linear state transition function (1) and with the initial state $\underline{0}$ we have:

$$\begin{aligned} &S(Y_1, \ldots, Y_{i-1}, Y_i \oplus E_i, Y_{i+1}, \ldots, Y_n) \\ &\quad = S(Y_1, Y_2, \ldots, Y_n) \oplus S(\mathbf{0}, \ldots, \mathbf{0}, E_i, \mathbf{0}, \ldots, \mathbf{0}) \end{aligned}$$

where 0 denotes an M by L matrix of all 0s.

Next, we apply a second, modified test sequence to the circuit under test, derived in a straightforward fashion from the first test sequence. The goal here is to provide an all-0 L dimensional column vector ($\underline{0}$) input to the MISR for one clock cycle immediately after each test response Y_i, $1 \leq i \leq n$, is shifted in M clock cycles into the MISR. The second test sequence can be easily generated by use of the same test pattern source as for the first test sequence. The masking logic is used to provide every M clock cycles an additional $\underline{0}$ input to the MISR and at the same time, freeze the scan clock using simple gating logic. This is done immediately after the capture cycle of the scan operation.

The signature of the MISR for the second test sequence is given by

$$\begin{aligned} &S(Y_1, \underline{0}, \ldots, Y_{i-1}, \underline{0}, Y_i \oplus E_i, \underline{0}, Y_{i+1}, 0, \ldots, Y_n, \underline{0}) \\ &\quad = S(Y_1, \underline{0}, Y_{i-1}, \underline{0}, Y_i, \underline{0}, Y_{i+1}, \underline{0}, \ldots, Y_n, \underline{0}) \\ &\quad \oplus S(\mathbf{0}, \underline{0}, \ldots, E_i, \underline{0}, \ldots, \mathbf{0}, \underline{0}). \end{aligned}$$

We now assume that if the input E_i is applied to the MISR with initial state $\underline{0}$, the MISR is driven to the state $z(E_i)$. This implies that the first test sequence give us $S(\mathbf{0}, \mathbf{0}, \ldots, E_i, \ldots, \mathbf{0}) = \mathbf{A}^{(n-i)M} z(E_i)$.
From the second test sequence, we get

$$S(\mathbf{0}, \underline{0}, \ldots, \mathbf{0}, \underline{0}, E_i, \underline{0}, \ldots, \mathbf{0}, \underline{0}) = \mathbf{A}^{(n-i)(M+1)+1} z(E_i).$$

Hence we conclude that

$$\begin{aligned} z(E_i) &= \mathbf{A}^{(i-n)M} S(\underline{0}, \ldots, \underline{0}, E_i \underline{0}, \ldots, \underline{0}) \\ z(E_i) &= \mathbf{A}^{(i-n)(M+1)-1} \\ &\qquad \times S(\mathbf{0}, \underline{0}, \ldots, \mathbf{0}, \underline{0}, E_i, \underline{0}, \mathbf{0}, \underline{0}, \ldots, \mathbf{0}, \underline{0}) \end{aligned}$$

and

$$\begin{aligned} &S(\underline{0}, \ldots, \underline{0}, E_i, \underline{0}, \ldots, \underline{0}) \\ &\quad = \mathbf{A}^{i-n-i} S(\mathbf{0}, \underline{0}, \ldots, \mathbf{0}, \underline{0}, E_i, \underline{0}, \mathbf{0}, \underline{0}, \ldots, \mathbf{0}, \underline{0}) \end{aligned} \tag{10}$$

From Eq. (10), we can easily determine i, i.e., the failing vector in the BIST sequence. An admissible value of i must lie between 1 and n. As in Section 2, it is not necessary here to carry out matrix multiplication and inversion in order to determine a value of i that satisfies this equation. Instead, we can use the next-state and previous-state functions to reduce the amount of computation. We consider the MISR with initial-state $S(\mathbf{0}, \underline{0}, \ldots, \mathbf{0}, \underline{0}, E_i, \underline{0}, \mathbf{0}, \underline{0}, \ldots, \mathbf{0}, \underline{0})$ and determine if the state $S(\underline{0}, \ldots, \underline{0}, E_i, \underline{0}, \ldots, \underline{0})$ can be reached for different values of i.

As in the case of a combinational circuit under test we next ask under what conditions can a fault φ in a full-scan sequential circuit, which is identified by the proposed method as a one-positional error under the test pattern X_i, is actually a two-positional error under the test patterns X_r and X_s.

If the two errors E_r and E_s under the test patterns X_r and X_s are erroneously interpreted as a single error E_i under the test pattern X_i then

$$S(\mathbf{0}, \ldots, \mathbf{0}, E_r, \mathbf{0}, \ldots, \mathbf{0}, E_s, \mathbf{0}, \ldots, 0) = S(\mathbf{0}, \ldots, \mathbf{0}, E_i, \mathbf{0}, \ldots, \mathbf{0}),$$

which implies that

$$\mathbf{A}^{(n-r)M} z(E_r) \oplus \mathbf{A}_{(n-r)M} z(E_s) = \mathbf{A}^{(n-i)M} z(E_i), \quad \text{and}$$
$$S(\mathbf{0}, \underline{0}, \ldots, \mathbf{0}, \underline{0}, E_r, \mathbf{0}, \underline{0}, \ldots, \mathbf{0}, E_s, \mathbf{0}, \underline{0}, \ldots, \mathbf{0}\underline{0}) = S(\mathbf{0}, \underline{0}, \ldots \mathbf{0}\underline{0}, E_i, \mathbf{0}, \ldots, \mathbf{0}, \underline{0}),$$

which implies that

$$\mathbf{A}^{(n-r)(M+1)+1} z(E_r) \oplus \mathbf{A}^{(n-r)(M+1)+1} z(E_s) = \mathbf{A}^{(n-i)(M+1)+1} z(E_i)$$

have to be valid. The error $z(E_i)$ and the error position i are determined by the proposed diagnosis method, and in the following discussion these values are assumed to be known.

We take into account the fact that for a MISR with a primitive feedback polynomial, the matrix $(\mathbf{I} \oplus \mathbf{A}^m)$, $1 \leq m \leq 2^L - 1$ here, is invertible. It is then easy to show that for every pair r, s, with $1 \leq r, s \leq n$, $z(E_r)$ and $z(E_s)$ are uniquely determined from $z(E_i)$ and i. Thus, if a one-positional error E_i under the ith test pattern X_i is identified by the proposed method, a total of $\binom{n-1}{2}$ two-positional errors can be erroneously interpreted as this one-positional error. The number of all possible two-positional errors is $\binom{n}{2}(2^{LM} - 1)^2$, where L is the number of scan chains and M is the number of scan cells in a scan chain.

If we assume that all the possible two-positional errors are equally likely then the probability $p_{2\to 1}$, that a pair of failing vectors is misinterpreted as a single failing vector is given by

$$p_{2\to 1} = \frac{\binom{n-1}{2}}{\binom{n}{2}(2^{LM})^2} = \frac{n-2}{n} \cdot \frac{1}{2^{2LM} - 2^{LM+1} + 1} \approx \frac{1}{2^{2LM}}$$

which is very small for realistic values of L and M.

In practice, the assumption that all the two-positional errors are equally likely is unrealistic. Nevertheless, we expect the the probability that a two-positional error is erroneously interpreted by the proposed method as a one-positional error to be extremely small. Based on these results, we are able to identify a failing vector for a fault φ in the circuit under test in the following way.

We consider R test intervalsn $X_1^1, \ldots, X_n^1, X_1^2, \ldots, X_n^2, \ldots, X_1^R, \ldots, X_n^R$ each of length n. For each of these R intervals, we compare the expected correct signatures of the MISR with the signatures obtained for the circuit under test. From the differences between these signatures, we use the proposed method to determine for the jth interval, $1 \leq j \leq R$, the value i_j of the corresponding failing test input X_i^j . If no solution is found for Eq. (10), $1 \leq i_j \leq n$, for the jth interval then we ignore these interval. On the other hand, if a solution is found, then X_i^j is taken to be a failing test pattern for the fault φ in the circuit under test. The test pattern X_i^j is uniquely determined if exactly one test pattern detects the fault in this interval. In the next section, we present experimental results for the ISCAS-85 and the ISCAS-89 circuits.

4. Experimental Results

We first present experimental results for the ISCAS-85 combinational benchmark circuits. We identified a set of faults for each circuit that are not easily detected by a small number of pseudorandom patterns. These faults are of interest to us and the proposed method is targeted toward them. In order to eliminate the easy to-detect faults that are not of interest to us, we applied 100 pseudorandom vectors to the circuit under test as a pre-processing step. We only retained those faults that were not detected by these patterns. We injected these faults into the circuits one at a time, and collected the MISR signatures in each case for various interval lengths, varying from 100 to 500, and for a total of 1000 pseudorandom patterns. The algebraic analysis technique was then applied to the differences in the MISR signatures. If a one-positional error occurs in at least one of the intervals, the corresponding failing test pattern (and the corresponding error vector in case of a combinational circuit) can be uniquely determined.

The results are shown in Table 3. Columns 1 and 2 list the name of the circuit and the number of faults that are not detected by the first 100 (pre-processing) pseudorandom test patterns. Columns 3, 4, 5, 6, 7 list the number of hard-to-detect faults (out of those listed in Column 2) that cause exactly one failing vector in at least one interval. These are the faults for which the

Table 3. Experimental results for the ISCAS-85 benchmark circuits.

Circuit	No of hard-to-detect faults considered	No of hard-to-detect faults diagnosed for different interval lengths				
		100	200	300	400	500
c432	26	25 (96.2%)	20 (76.9%)	19 (73.1%)	12 (46.2%)	11 (42.3%)
c499	42	42 (100%)	34 (80.0%)	27 (64.3%)	22 (52.4%)	12 (28.6%)
c880	61	61 (100%)	49 (80.3%)	43 (70.5%)	33 (54.1%)	30 (49.2%)
c1355	157	152 (96.8%)	141 (89.8%)	132 (84.1%)	121 (77.1%)	94 (59.9%)
c1908	255	243 (95.3%)	226 (88.6%)	208 (81.6%)	190 (74.5%)	148 (58.0%)
c2670	152	151 (99.3%)	140 (92.1%)	107 (70.4%)	90 (59.2%)	61 (40.1%)
c3540	563	532 (94.5%)	438 (77.8%)	396 (70.3%)	314 (55.8%)	223 (39.6%)
c5315	344	315 (91.6%)	226 (65.7%)	200 (58.1%)	130 (37.8%)	82 (23.8%)
c7552	480	447 (93.1%)	366 (76.3%)	297 (61.9%)	235 (49.0%)	155 (32.3%)

Table 4. Experimental results for the ISCAS-89 benchmark circuits.

Circuit	No of hard-to-detect faults considered	No of hard-to-detect faults diagnosed for different interval lengths				
		100	200	300	400	500
s1196	148	133 (89.9%)	118 (79.7%)	110 (74.3%)	97 (65.5%)	75 (50.8%)
s5378	454	438 (96.5%)	391 (86.1%)	367 (80.8%)	339 (74.7%)	266 (58.6%)
s9234.1	913	877 (96.1%)	829 (90.8%)	774 (84.8%)	676 (74.0%)	618 (67.7%)
s13207.1	1119	1093 (96.7%)	1036 (92.6%)	1022 (91.3%)	959 (85.7%)	781 (69.8%)
s15850.1	1464	1363 (93.1%)	1252 (85.5%)	1113 (76.0%)	1017 (69.5%)	812 (55.5%)
s38417	2207	2142 (97.0)	1948 (88.26)	1764 (79.92)	1615 (73.18)	1285 (58.22)
s38584.1	3881	3751 (96.65)	3337 (85.98)	3022 (77.87)	2538 (65.39)	1734 (44.68)

failing test vector and the corresponding error vector can be diagnosed by the proposed method. Also listed are the percentages of the hard-to-detect faults that are correctly diagnosed by the proposed method.

For an interval length of 100, we can uniquely identify the failing vector, which we refer to as the diagnosis of the corresponding fault, for over 90% of the hard-to-detect faults. In many cases, we can diagnose over 95% of these faults. This percentage drops as expected for longer intervals; nevertheless, we can diagnose a significant number of faults even for an interval length of 500.

The experimental results for the full-scan versions of the ISCAS-89 circuits are shown in Table 4. For these circuits, only the failing vector in an interval can be identified; the corresponding error vector cannot be obtained from the algebraic technique presented in Section 3.

In our experiments, we do not need to explicitly to model the scan chains. We apply a sequence of 1000 test patterns to the circuit under test. If the circuit is combinational, we apply these test patterns to the inputs of the circuit and we observe the outputs of the circuit. In the case of a sequential circuit with one or more scan chains, we apply the pseudorandom test patterns to the primary inputs and to the secondary inputs of the combinational part of the circuit, and we observe the corresponding primary and secondary outputs.

As discussed in Section 2, the proposed method requires very little hardware overhead. No modification is made here to the traditional STUMPSlike BIST architecture. The overhead is limited to m 2-input AND gates and a small finite-state machine that generates an alternating sequence.

5. Conclusions

We have presented a new technique for uniquely identifying a single failing vector in an interval of test vectors. This approach is based on an algebraic analysis of the signatures captured in the MISR during a BIST session, and it is aimed that faults that are not detected by a small number of pseudorandom test patterns. The analysis relies on the linearity properties of the MISR,

and on the use of two test sequences, where the second test sequence is derived from the first in a straightforward manner. The same test pattern source is used for both test sequences. We have shown algebraically that if an interval contains only a single failing vector, the analysis technique is guaranteed to identify it. In addition, we have shown through a probabilistic analysis that if an interval contains two failing vectors, the probability that this pair of failing vectors is misinterpreted as a single failing vector is extremely low. Experimental results for the ISCAS benchmark circuits show that the proposed approach can be efficiently used to uniquely identify failing vectors in a BIST environment.

Acknowledgment

The authors thank Prof. Serge Demidenko for valuable comments on this manuscript and for pointers to prior work in this area.

References

1. R.C. Aitken and V.K. Agarwal, "Diagnosis Method using Pseudo-Random Vectors Without Intermediate Signatures," in *Proc. Int. Conf. CAD*, 1989, pp. 574–580.
2. P.H. Bardell and W.H. McAnney, "Self-Testing of Multichip Logic Modules," in *Proc. International Test Conference*, 1982, pp. 200–204.
3. P.H. Bardell, W.H. McAnney, and J. Savir, *Built-in Test for VLSI: Pseudorandom Techniques*, New York: John Wiley, 1987.
4. I. Bayraktaroglu and A. Orailoglu, "Improved Fault Diagnosis in Scan-Based BIST via Superposition," in *Proc. Design Automation Conf.*, June 2000, pp. 55–58.
5. I. Bayraktaroglu and A. Orailoglu, "Diagnosis for Scan- Based BIST: Reaching Deep into the Signatures," in *Proc. Design, Automation and Test in Europe (DATE) Conf.*, March 2001, pp. 102–109.
6. M.L. Bushnell and V.D. Agrawal, *Essentials of Electronic Testing*, Norwell, MA: Kluwer Academic Publishers, 2000.
7. J.C. Chan and J.A. Abraham, "A Study of Faulty Signatures using a Matrix Formulation," in *Proc. International Test Conference*, 1990, pp. 553–561.
8. J.C. Chan and B.F. Womak, "Diagnostics Based on Faulty Signatures," in *Proc. International Test Conference*, p. 935, 1989.
9. J.C. Chan and B.F. Womak , "A Study of Faulty Signatures for Diagnostics," *Proc. Inte. Symp. Circuits and Systems*, 1990, pp. 2701–2704.
10. B. Chess and T. Larrabee, "Creating Small Fault Dictionaries," *IEEE Transactions on CAD*, vol. 18, pp. 346–356, March 1999.
11. T.R. Damarla, C.E. Stroud, and A. Sathaye, "Multiple Error Detection and Identification via Signature Analysis," *Journal of Electronic Testing: Theory and Applications*, vol. 7, pp. 193–207, 1995.
12. S. Demidenko, A. Ivanyukovich, L. Makhist, and V. Piuri, "On the Binary Sequences with Indistinguishable Signature for a Given Error Multiplicity in Electronic Testing," *Journal of the Institution of Engineers, Singapore*, vol. 35, pp. 63–66, Feb. 1995.
13. S. Demidenko and V. Piuri, "Signature Compression: a Generalized Description and its Applications," *Journal of Microelectronic Systems Integration*, vol. 3, pp. 19–33, 1995.
14. O.N. Diachenko and A.N. Tarasenko, "Modes of Diagnostic Information Separation from Signature," *Electronnoje Modelirowanie*, vol. 12, pp. 64–70, 1990 (in Russian).
15. J. Ghosh-Dastidar, D. Das, and N.A. Touba, "Fault Diagnosis in Scan-Based BIST using Both Time and Space Information," in *Proc. International Test Conference*, 1999, pp. 95–102.
16. M. Goessel, *Angewandte Automatentheorie II*, Berlin: Akademie-Verlag, 1971 (in German).
17. M.G. Karpovsky and S.M. Chaudhry, "Design of Self- Diagnosing Boards by Multiple Signature Analysis," *IEEE Transactions on Computers*, vol. 42, pp. 1035–1044, Sept. 1993.
18. M.G. Karpovsky and P. Nagvajara, "Optimal Time and Space Compression of Test Responses for VLSI Devices," in *Proc. 1987 Int. Test Conference*, 1987, pp. 523–529.
19. C. Liu, K. Chakrabarty, and M. Goessel, "An Interval-Based Diagnosis Scheme for Identifying Failing Vectors in a Scan-BIST Environment," in *Proc. Design, Automation and Test in Europe (DATE) Conference*, 2002, pp. 382–386.
20. W.H. McAnney and J. Savir, "There is Information in Faulty Signatures," in *Proc. Int. Test Conf.*, 1987, pp. 630–636.
21. D.K. Pradhan and S.K. Gupta, "A New Framework for Designing and Analyzing BIST Techniques and Zero Aliasing Compression," *IEEE Transactions on Computers*, vol. C-40, pp. 743–763, June 1991.
22. I. Pomeranz and S.M. Reddy, "On Dictionary-Based Fault Location in Digital Logic Circuits," *IEEE Transactions on Computers*, vol. 46, pp. 48–59, Jan. 1997.
23. J. Rajski and J. Tyszer, "Fault Diagnosis in Scan-Based BIST," in *Proc. Int. Test Conf.*, 1997, pp. 894–902.
24. J. Savir and W.H. McAnney, "Identification of Failing Tests with Cycling Registers," in *Proc. Int. Test Conf.*, 1988, pp. 322–328.
25. J.E. Smith, "Measures of Effectiveness of Fault Signature Analysis," *IEEE Transactions on Computers*, vol. C-29, pp. 510–514, June 1980.
26. P. Song, F. Motika, D.R. Knebel, R.F. Rizzolo, and M.P. Kusko, "S/390 G5 CMOS Microprocessor Diagnostics," in *Proc. International Test Conference*, 1999, pp. 1073–1082.
27. L. Voelkel and J. Pliquett, *Signaturanalyse*, Berlin: Springer-Verlag, 1988 (in German).
28. T.W. Williams, W. Daehn, M. Gruetzner, and C.W. Starke, "Aliasing Errors in Signature Analysis Registers," *IEEE Design and Test of Computers*, vol. 4, pp. 39–45, April 1987.
29. Y. Wu and S. Adham, "BIST Fault Diagnosis in Scan-Based VLSI Environment," in *Proc. Int. Test Conf.*, 1996, pp. 48–57.
30. Y. Wu and S. Adham, "Scan-Based BIST Fault Diagnosis," *IEEE Transactions on CAD*, vol. 18, pp. 203–211, Feb. 1999.
31. V.N. Yarmolik, *Fault Diagnostics of Digital Circuits*, Chichester, UK: John Wiley and Sons, 1990.
32. V.N. Yarmolik and S. Demidenko, *Generation and Application of Pseudorandom Sequences for Random Testing*, Chichester, UK: John Wiley and Sons, 1988.
33. V.N. Yarmolik and I.V. Kachan, *Self-Testing VLSI Design*, Amsterdam, The Netherlands: Elsevier, 1993.

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