Dual Ramp Analog/DC Converter (ADC)

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Outline

- The Design
- Classic Dual Slope Design
- Work Completed
- Final Estimations
- Questions
Design Objectives

Design ADC for Depth Gauge

- Our dual ramp ADC samples voltage values between .2v and 3.84 volts with a sample rate of over 300 samples per second.

- It's max power usage as determined by simulations is around 25 mW.

- Accuracy for this device fluctuates between 0.5% and 8.5% of the actual Vin value and is generally within .1V of the actual Vin sample.
Utilize PC’s clock and digital input/output capabilities to drive ADC.
**Classic Determination of Vin**

\[ T_2 = T_1 \times \frac{V_{in}}{V_{ref}} \]

\[ V_{in} = \frac{T_2}{T_1} \times V_{ref} \]

\[ V_{ref} = -5 \text{ V} \]

\[ T_1 \sim 1.8 \text{ to } 2.4 \text{ ms (TBD)} \]

\[ V_{th} = .34 \text{ mV} \]

Max 4 volts

Min 3.4 mV

Problems

- Maintaining a voltage drop of 5v across entire circuit
  - Settled for VDD of +4v & NVDD -1v
  - Modified Vin Determination Method
  - Designed Circuit and used values to determine calculation method.
S/H Output (Vin) is connected to the Comparator’s Reference input. Integrator is first ramped to 3.84V and then connected to NVDD (-1V) and allowed to ramp down. The comparator is triggered when the integrator output matches the input from the S/H circuit.
Early Indication of Slope Variation
Always Ramps to 3.84 V. However, slope of voltage drops are affected by input voltage.

Adjustment Factor 162 µs
Simulation (0.43v Capture)
Simulation (.79v Capture)

- Time (s):
  - 0.2M to 0.4M: 625 us
  - 0.4M to 0.6M: 0.79726
  - 0.6M to 1.0M: 1.25297
  - 1.0M to 1.2M: 3.84387
  - 1.2M to 1.4M: 3.91905
  - 1.4M to 1.6M: 5.00000
  - 1.6M to 1.8M: 5.00000
  - 1.8M to 2.0M: 2.00000
  - 2.0M to 2.2M: 5.00000
  - 2.2M to 2.4M: 5.00000

- Voltage (V):
  - 0.2M to 0.4M: 1.26364M (dx = 637.15133U)

- Time Labels:
  - 637 us
  - 162 us
Simulation (1.6v Capture)
Simulation (2.89v Capture)

162 us
## ADC Voltage Calculation

\[
Vin = \frac{(162.5 \text{ us} \times 3.84 \text{ V})}{(162.5 \text{ us} + T_{out})}
\]

<table>
<thead>
<tr>
<th>$V_{peak}$ (V)</th>
<th>Discharge Time (us)</th>
<th>Compare Time (us)</th>
<th>$V_{in}$ Known (V)</th>
<th>Trigger Time (us)</th>
<th>$V_{in}$ Calculate (V)</th>
<th>$V_{in}$ Adjust (V)</th>
<th>%error</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.84</td>
<td>1245</td>
<td>1063</td>
<td>0.52</td>
<td>161</td>
<td>0.496</td>
<td>0.50</td>
<td>2.98%</td>
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<tr>
<td>3.84</td>
<td>574</td>
<td>412</td>
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<td>162</td>
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<td>233</td>
<td>1.6</td>
<td>167</td>
<td>1.603</td>
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<tr>
<td>3.84</td>
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<td>149</td>
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<td>167</td>
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<td>65</td>
<td>2.78</td>
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<tr>
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<td>13</td>
<td>3.57</td>
<td>162</td>
<td>3.554</td>
<td>3.54</td>
<td>0.71%</td>
</tr>
</tbody>
</table>

Time Adjustment = 162.5

Range: 0.2 V to *3.84 V

*prefer values less than 3.84 since this will also represent values greater that 3.84.
Circuits

- Switches
Sample/Hold Circuit
Sample/Hold Layout
Integrator Circuit
Integrator Sub-Circuit
Integrator Circuit
Decided to produce voltage swing when a negative ramp voltage equals the Sampled Output Voltage
Comparator Circuit
Comparator Circuit
Dual Ramp ADC Circuit Complete
Work Completed

- End Product
  - Working HSPICE Simulations
  - DRC/LVS Clean Schematics

- Many Changes
  - Substrate Issues
  - Using GND with VDD of +4V and NVDD of -1V
  - “No battle plan ever survives contact with the enemy.” — Field Marshall Helmuth Carl Bernard von Moltke
Estimations

- **Power:**
  - Power estimate: 25mW (max achieved)

- **Area:**
  - $< .177 \text{ cm}^2 (5404 \text{ um} \times 3293 \text{ um})$
  - Off chip 20 nF capacitor approximately same size

- **Other**
  - Samples per Second: varies with Vin.
    - Smaller Vin results in longest time sample rates
    - $<1$ sample every 3ms or over 300 samples per second
Questions