4-bit ADC/DAC Design

Group Member: Yunfei Shen
Ming Gao
Tianyu Feng

Content

- Introduction
- DAC Implementation
- ADC Implementation

Introduction

- This design is divided into two devices: an **ADC** and a **DAC**.

- The **ADC** is composed of a comparator stage and an encoder stage.

  -The comparator stage discretizes an analog input voltage.

  -The encoder stage encodes the discrete values into a digital 4-bit binary word.

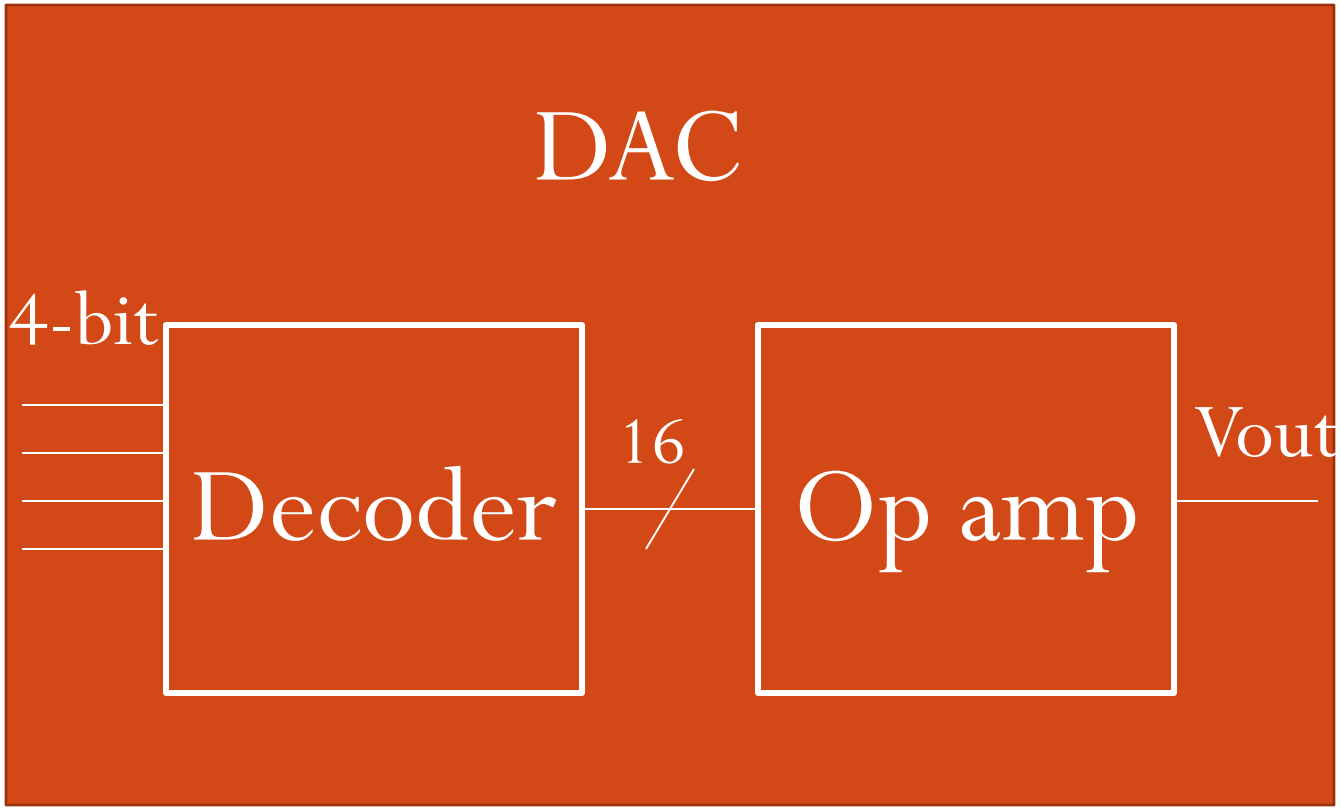
- The **DAC** is made up of decoder and operational amplifier.

  -The decoder is made up of 16 4-input NANDs.

  -The Op amp amplify the decoded signals and transfer them to the output.

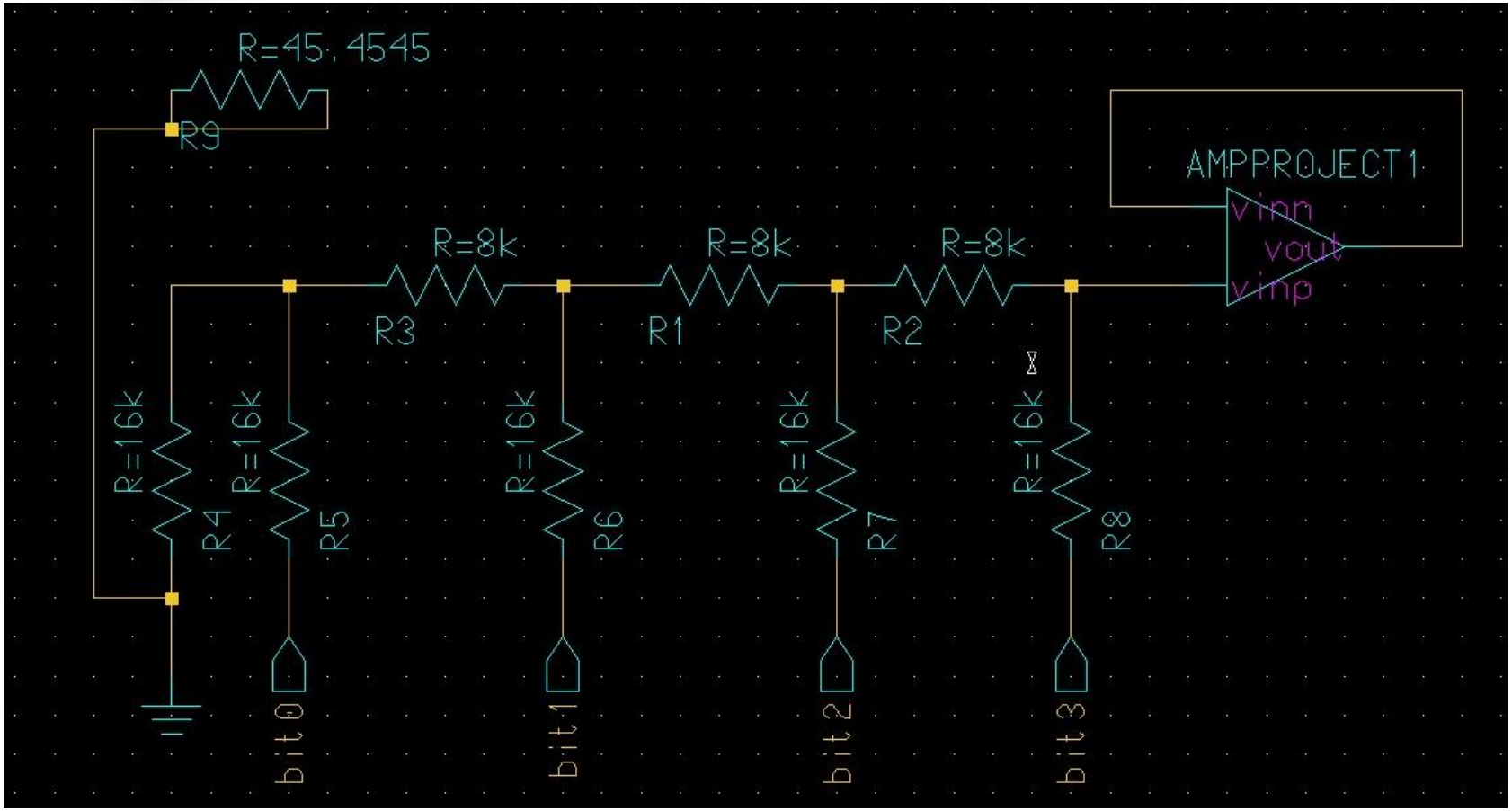
DAC Implementation

- Block Diagram



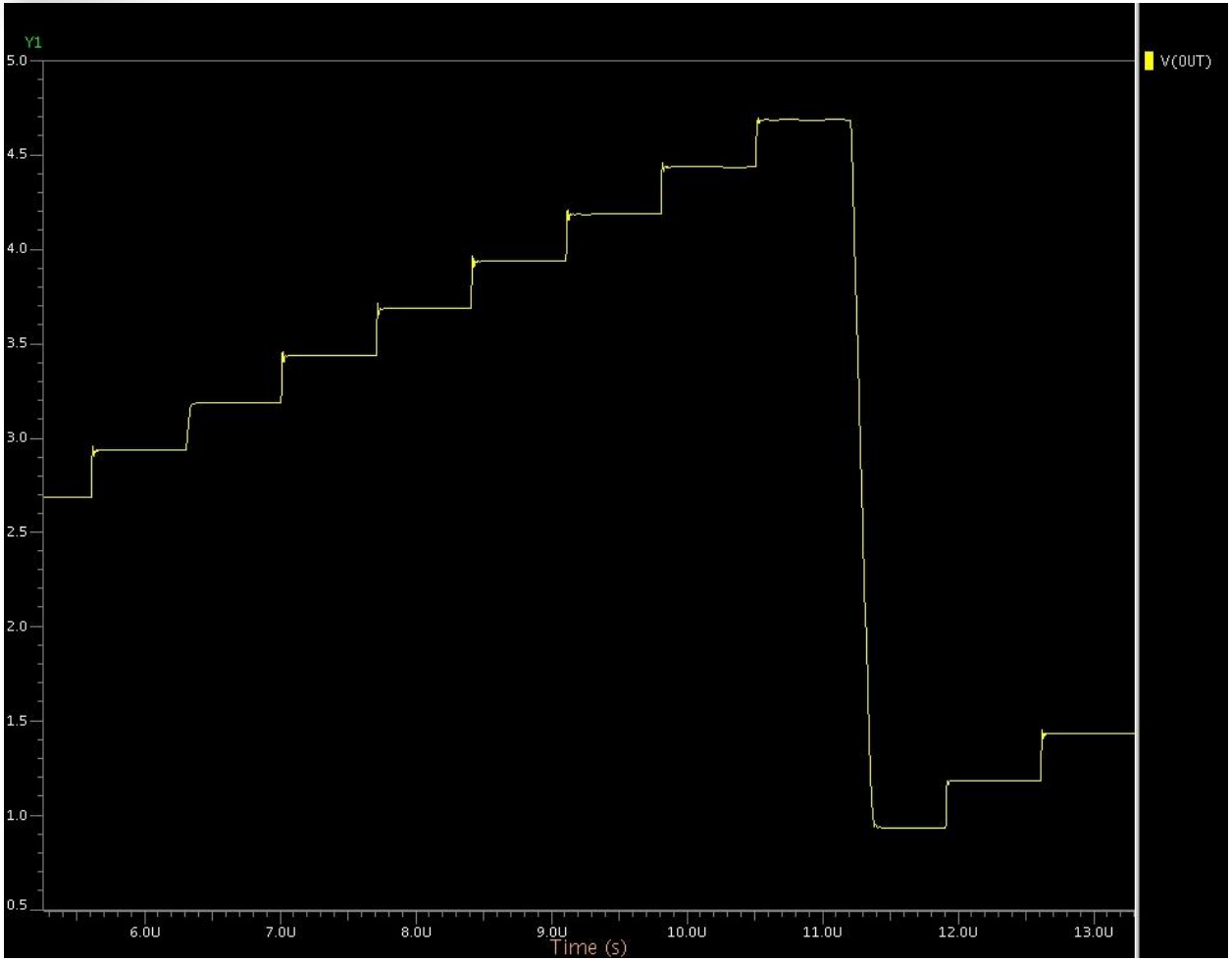
DAC Implementation

- R-2R DAC



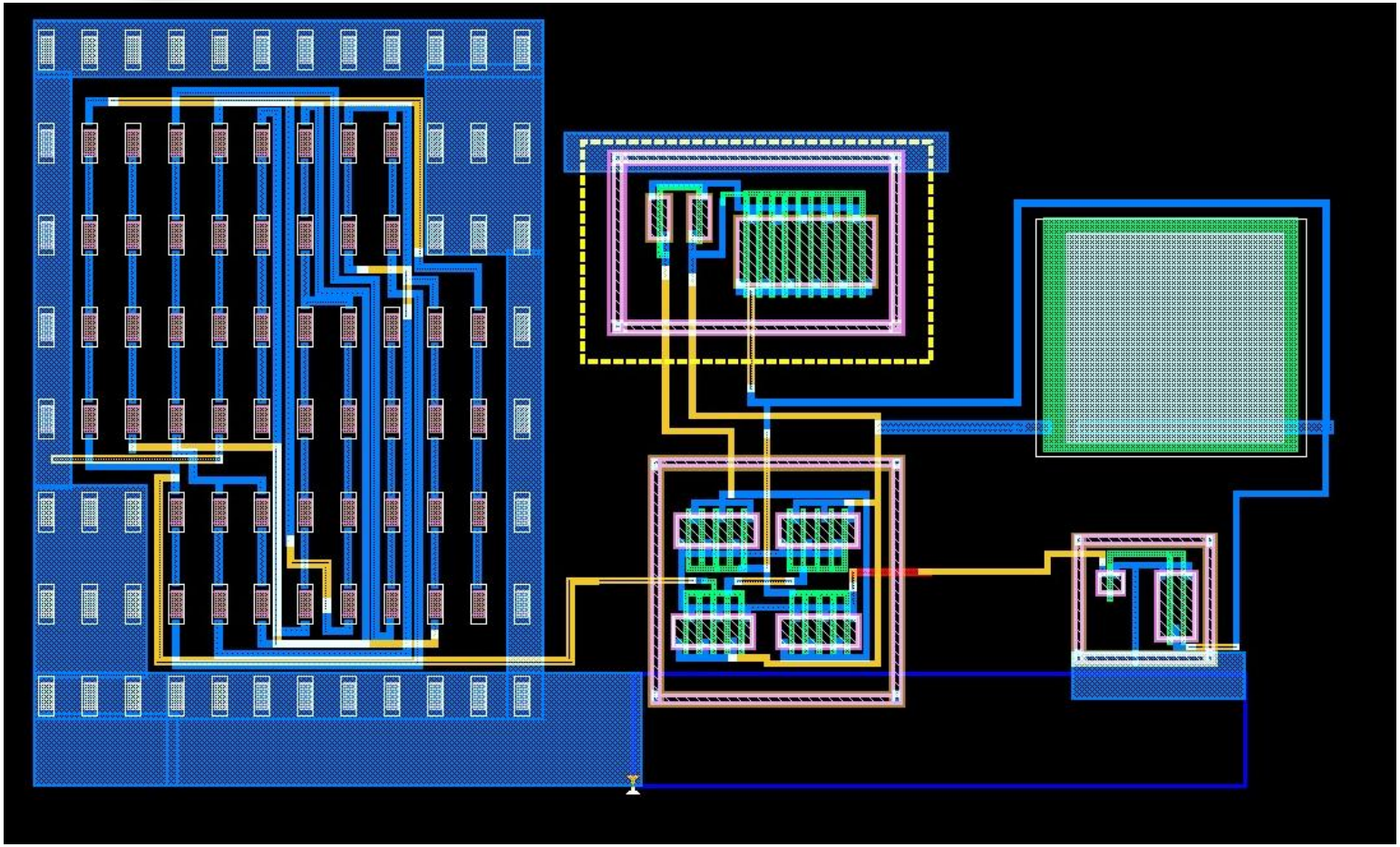
DAC Implementation

- R-2R DAC Simulation:



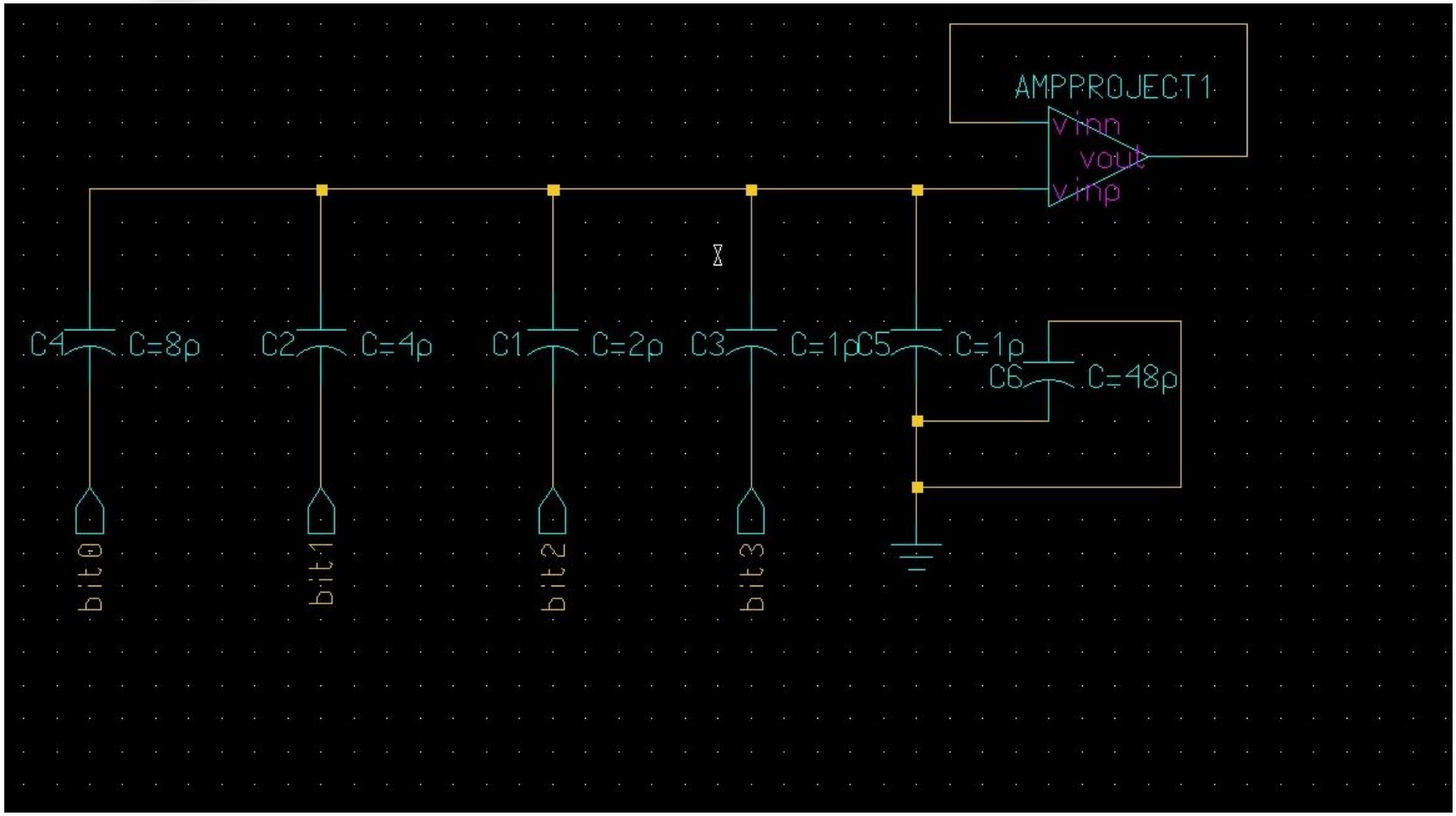
DAC Implementation

- R-2R DAC Layout:



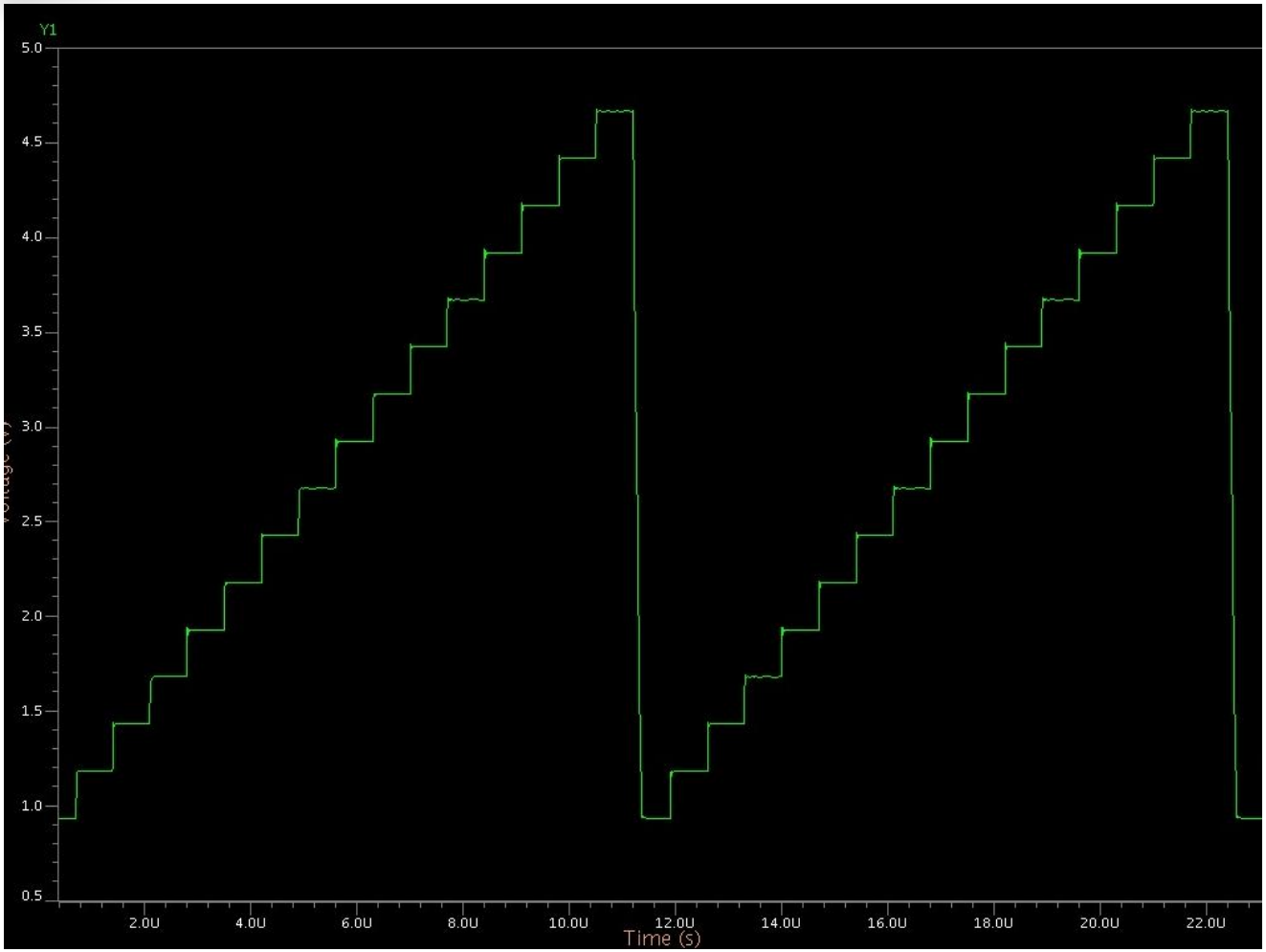
DAC Implementation

- Charge Scaling DAC



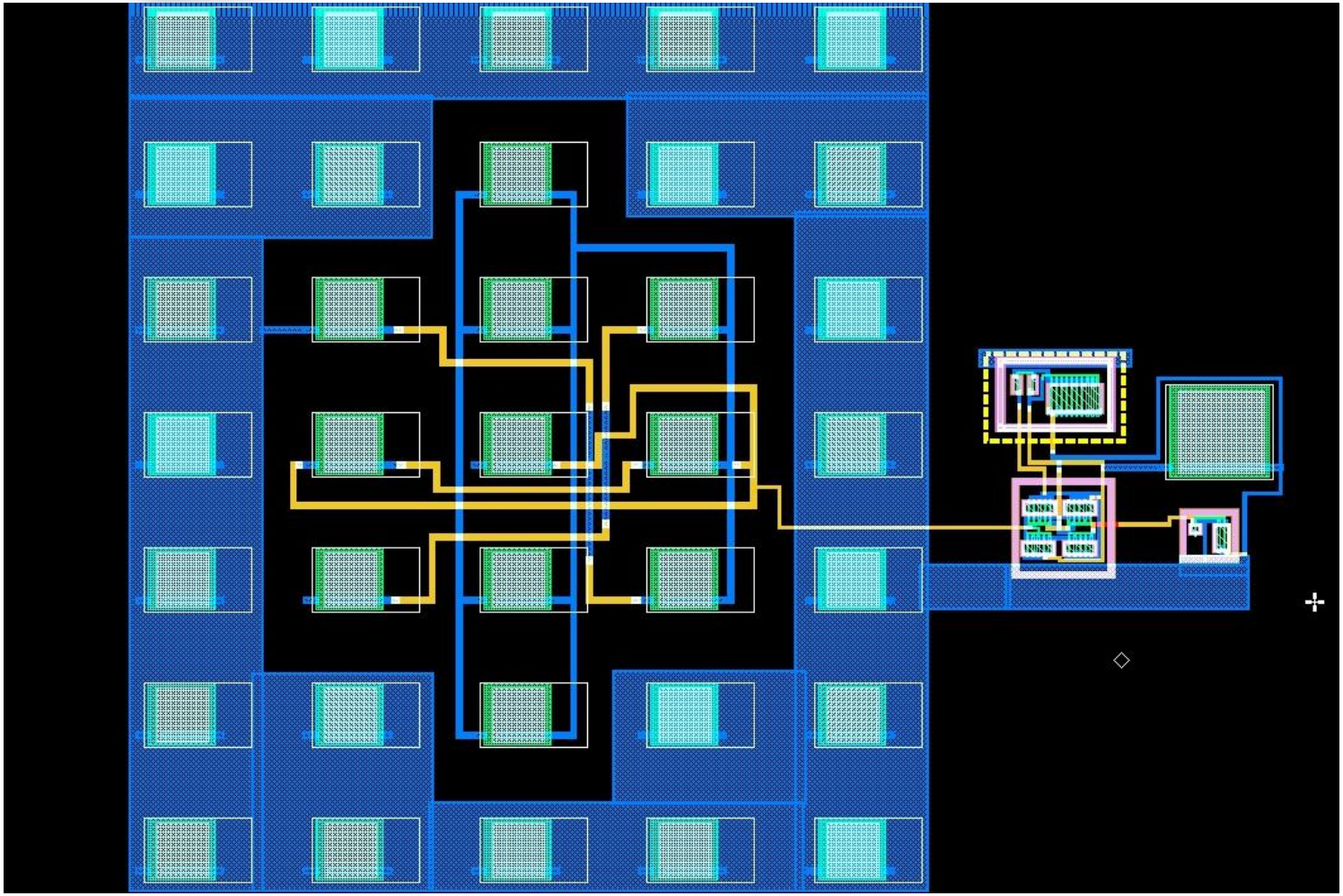
DAC Implementation

- Charge Scaling DAC Simulation:



DAC Implementation

- Charge Scaling DAC Layout:



DAC Implementation

- DAC Specification:

-- R-2R DAC:

---7 transistors

---10 resistors

---1 capacitor

--Area of layout = 300um*500um=0.15(mm)^2

-- Charge Scaling DAC:

---7 transistors

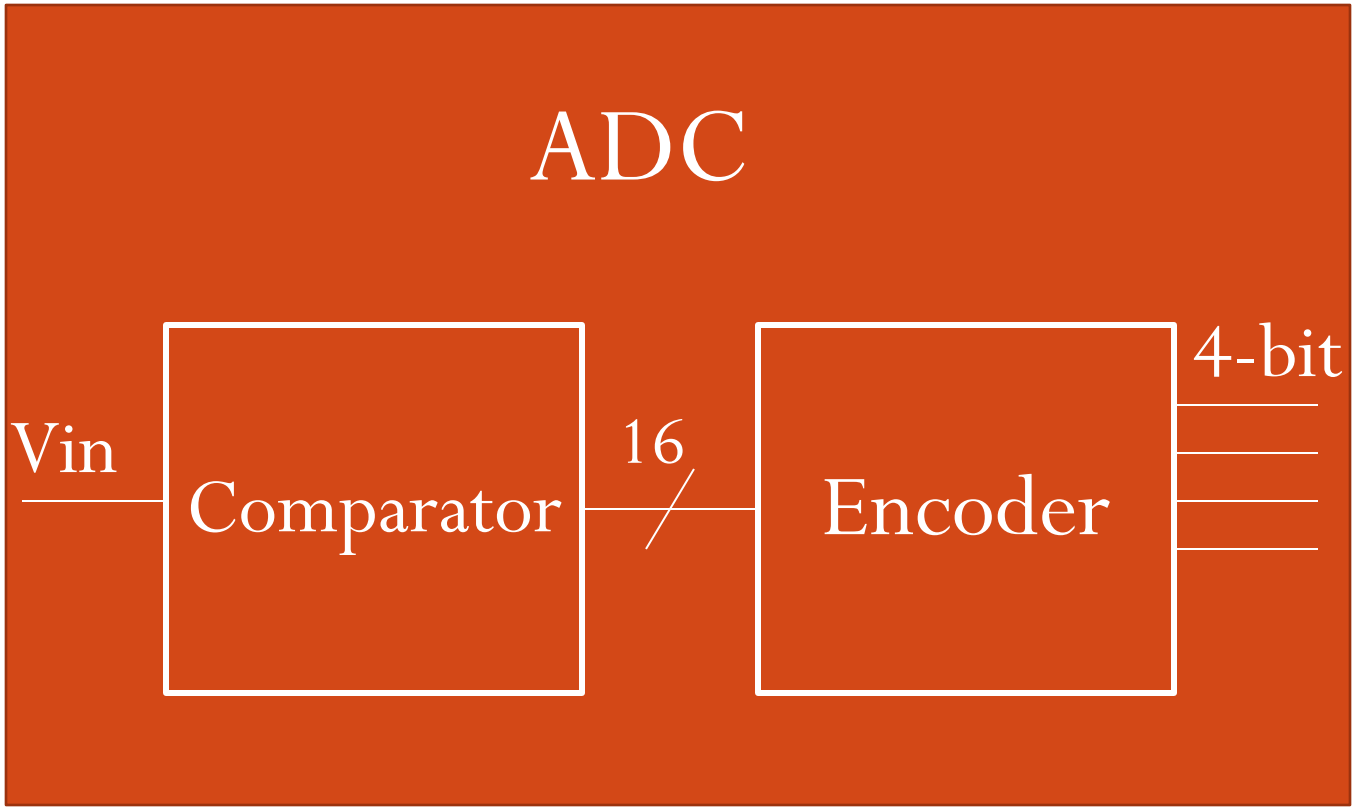
---1 resistor

---7 capacitors

--Area of layout = 1100um*840um=0.924(mm)^2

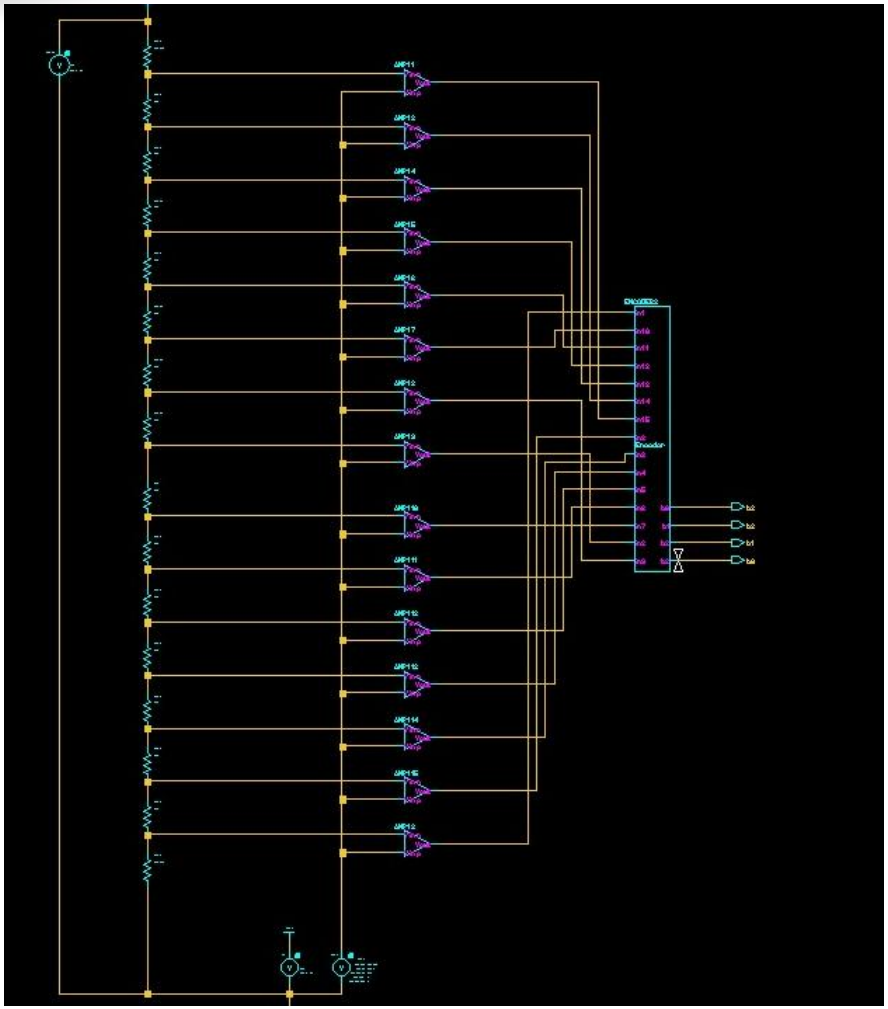
ADC Implementation

- Block Diagram



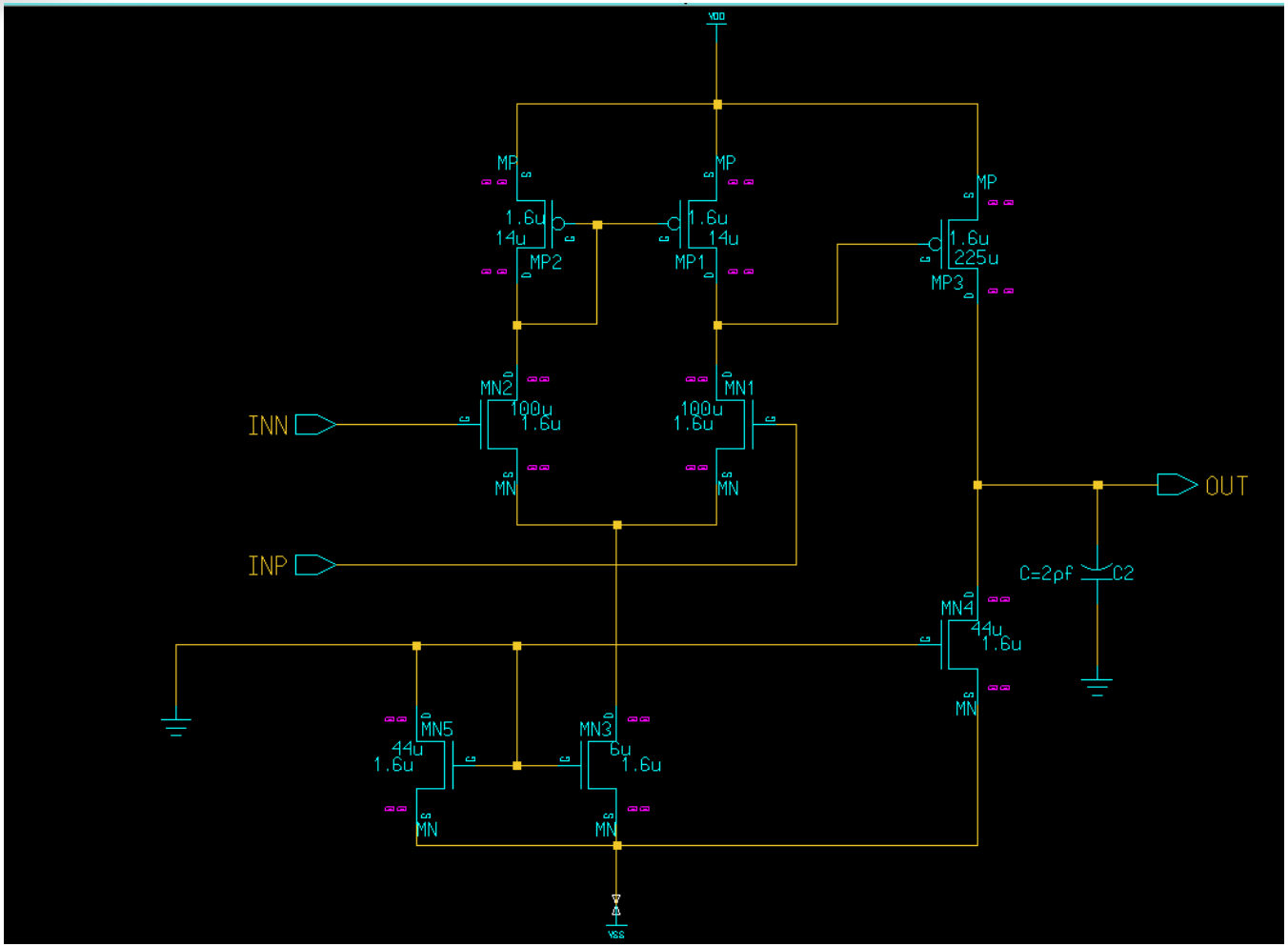
ADC Implementation

- Top View



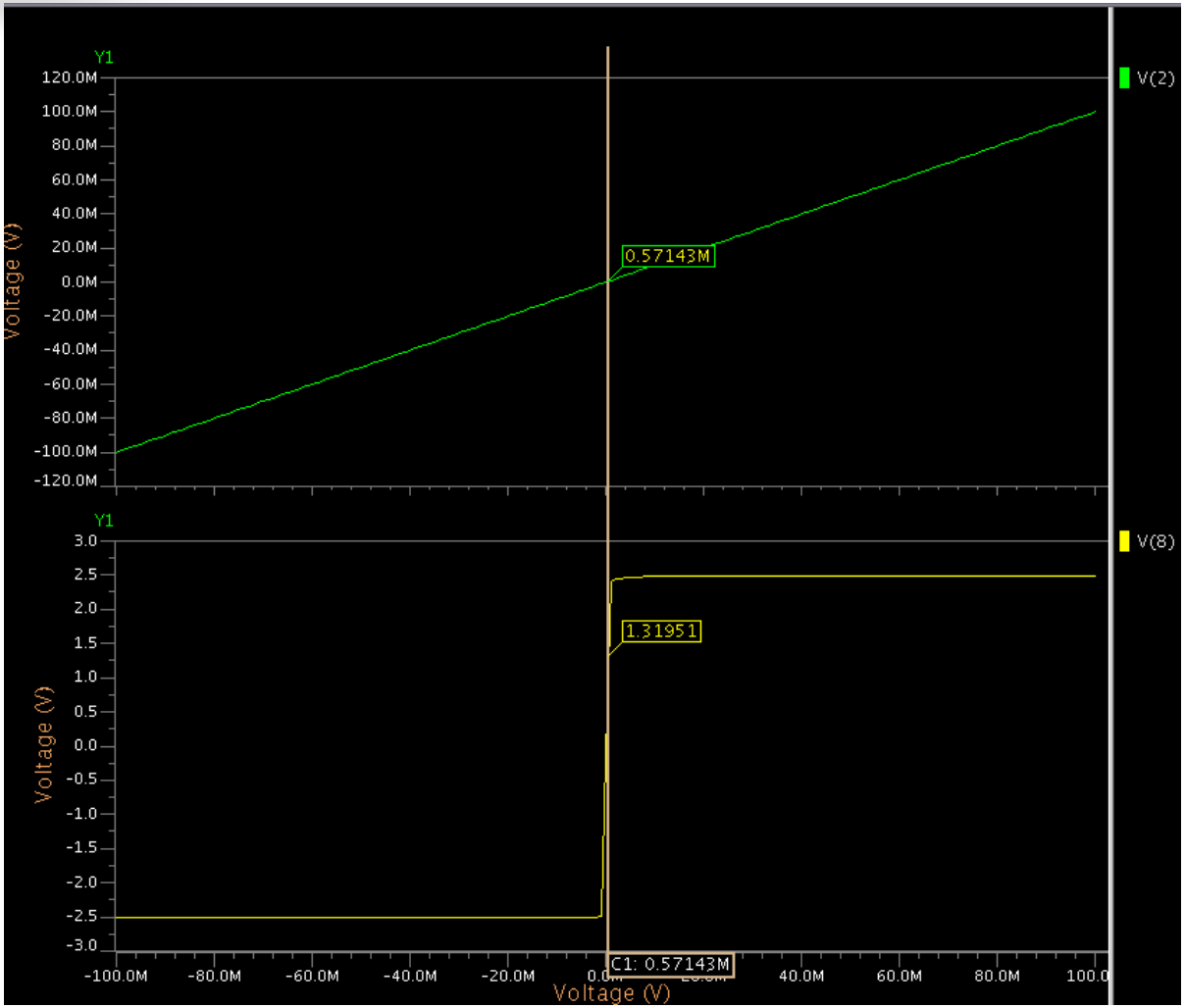
ADC Implementation

- op amp for ADC



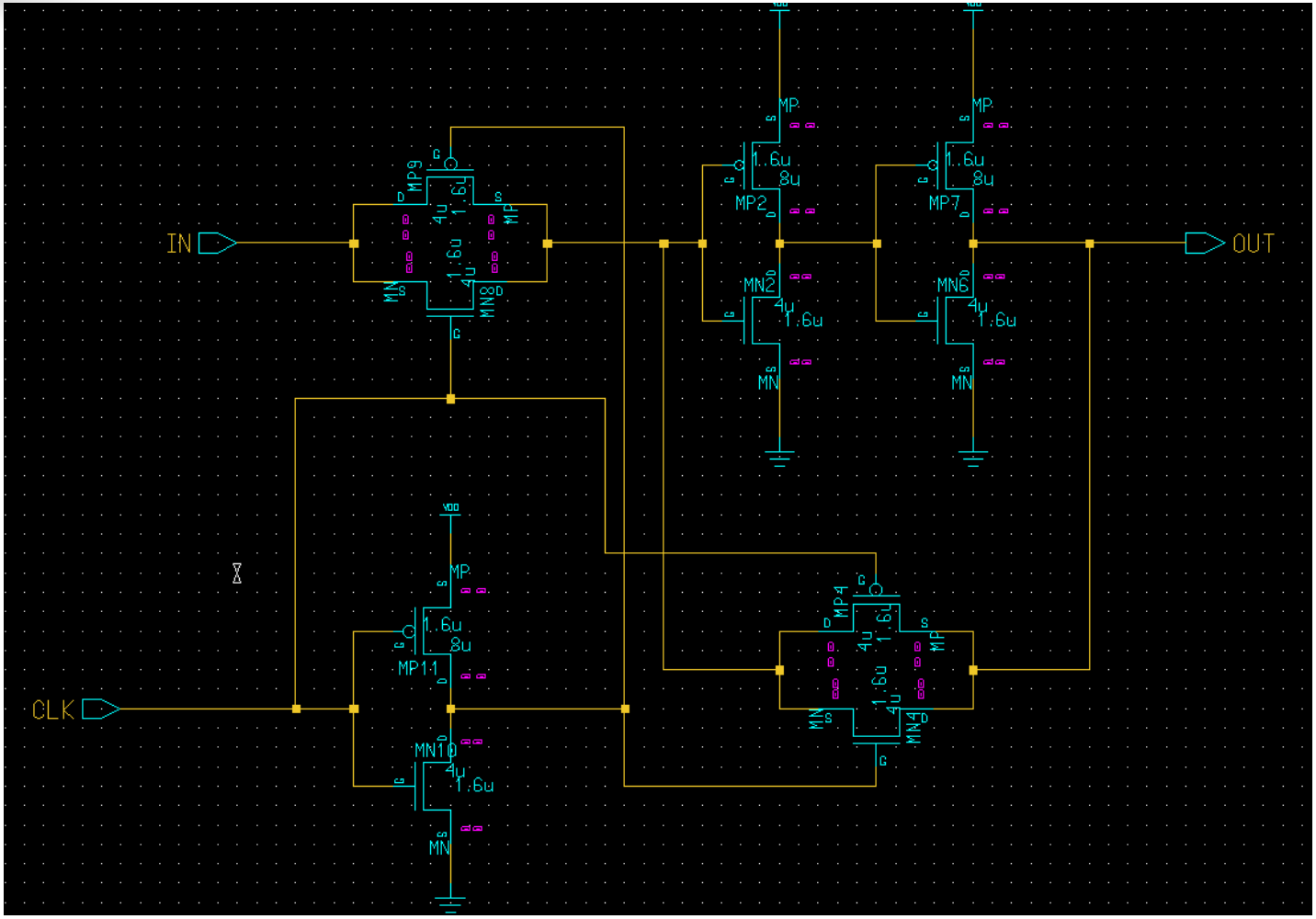
ADC Implementation

- Simulation: op amp



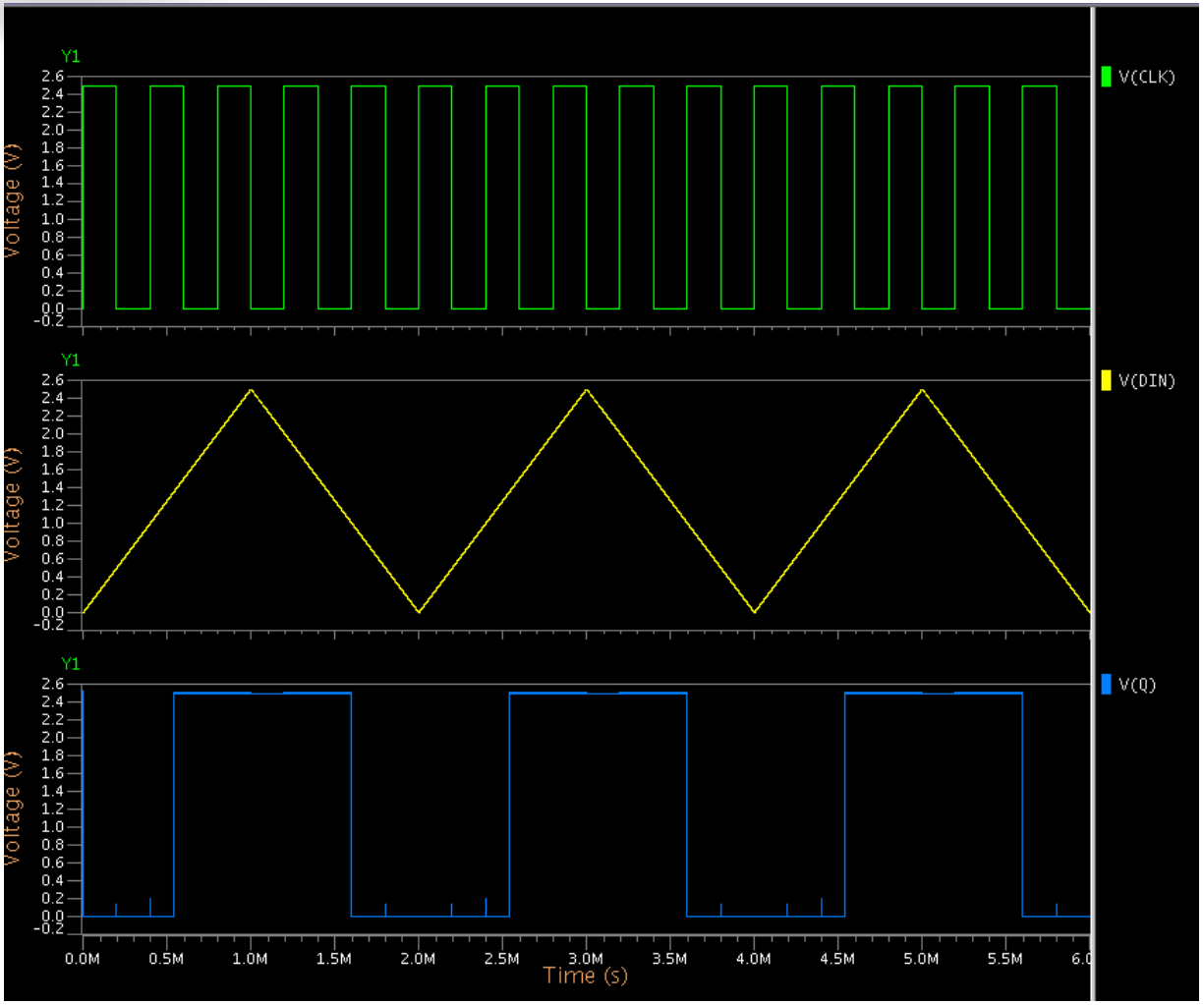
ADC Implementation

- Latch:



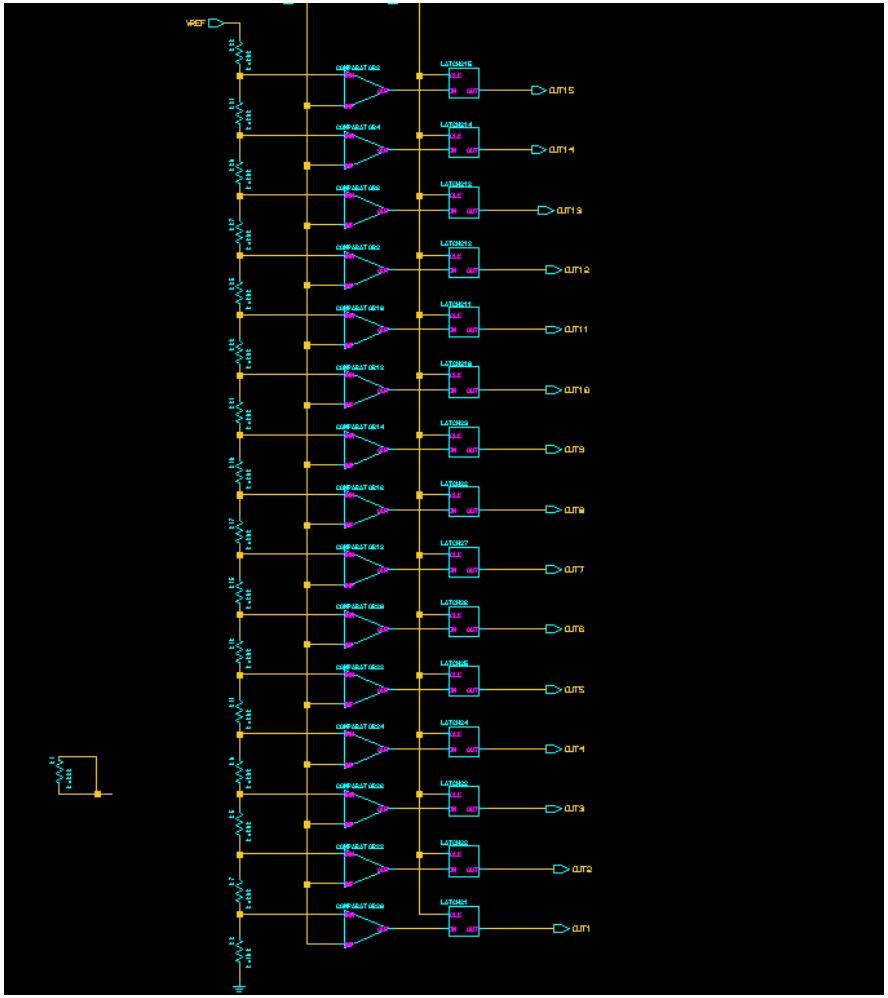
ADC Implementation

- Simulation: latch



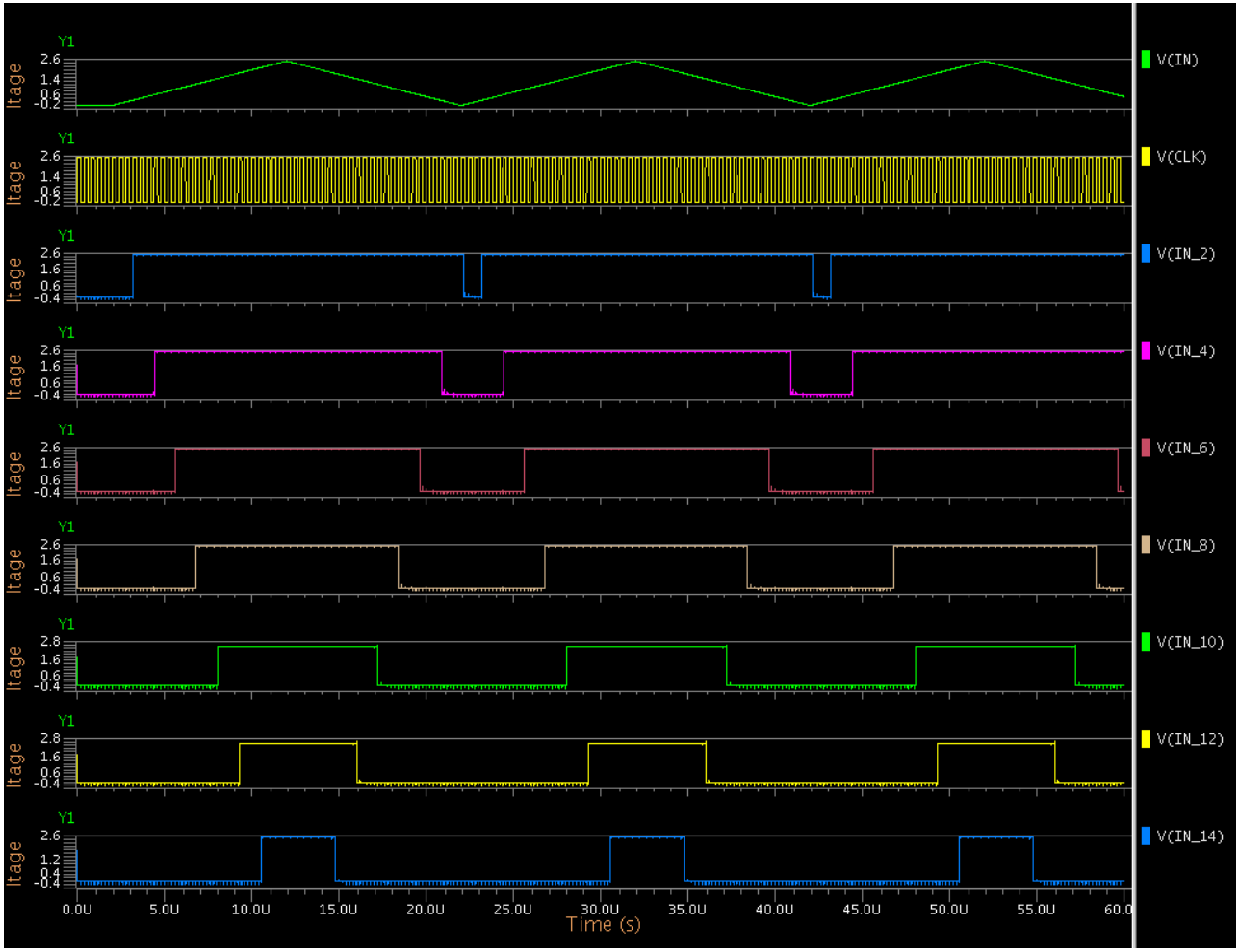
ADC Implementation

- Comparator: op amp + latch



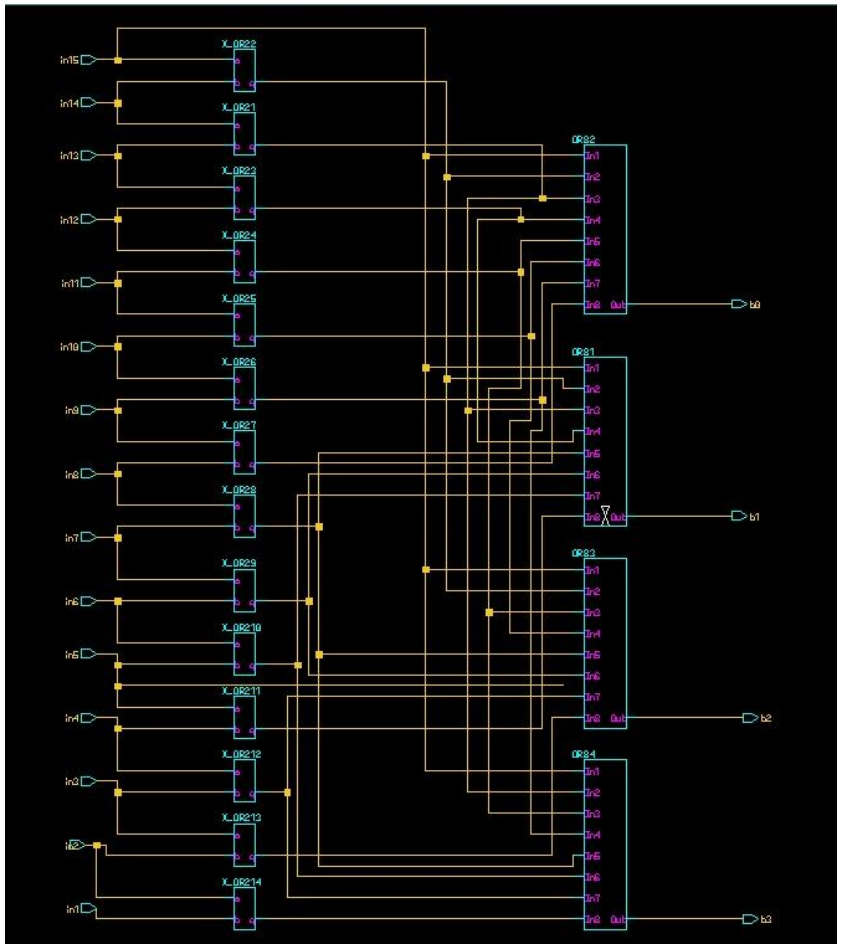
ADC Implementation

- Simulation: Comparator



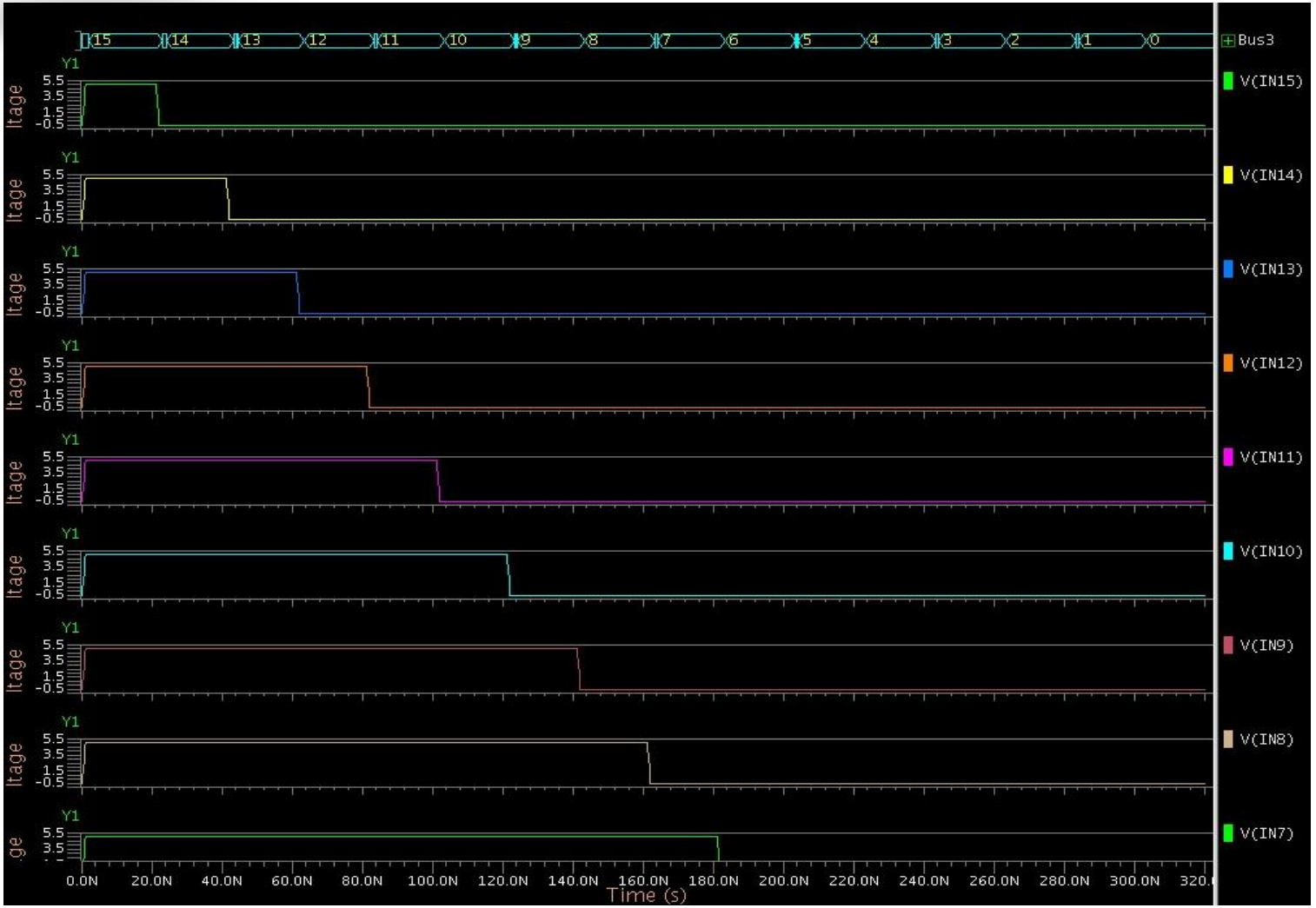
ADC Implementation

- Simulation: encoder



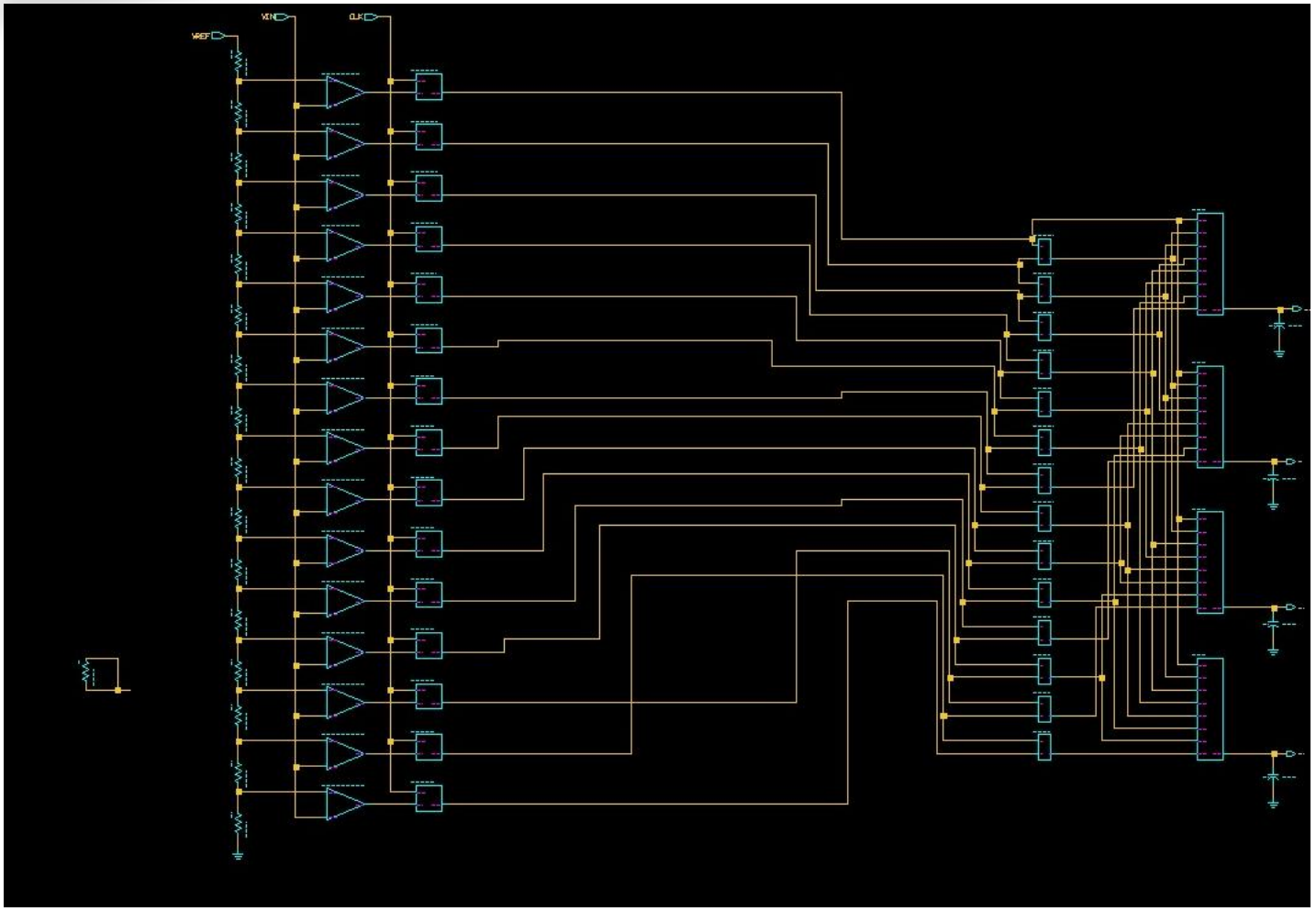
ADC Implementation

- Simulation: encoder



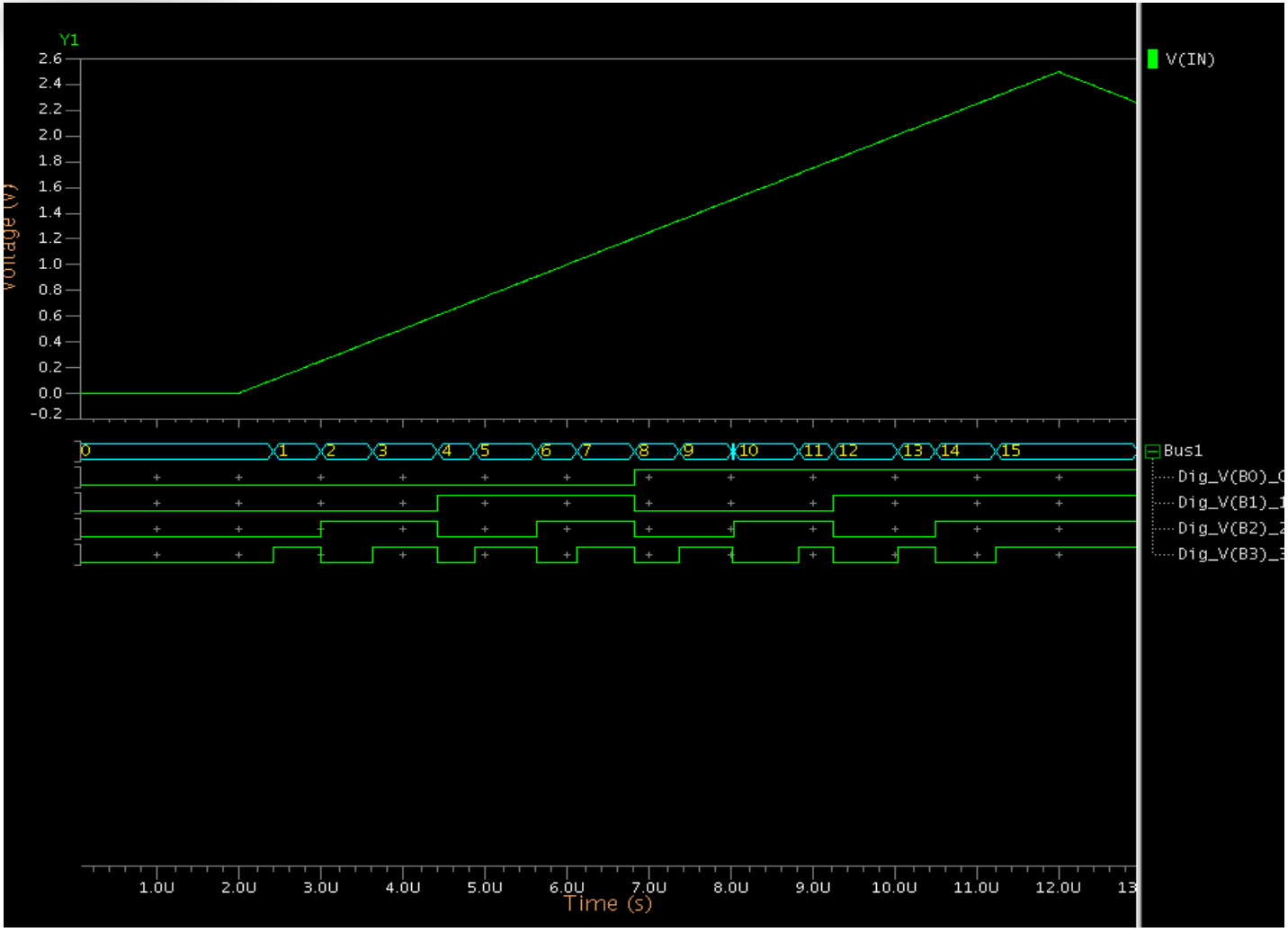
ADC Implementation

- 4-bit ADC



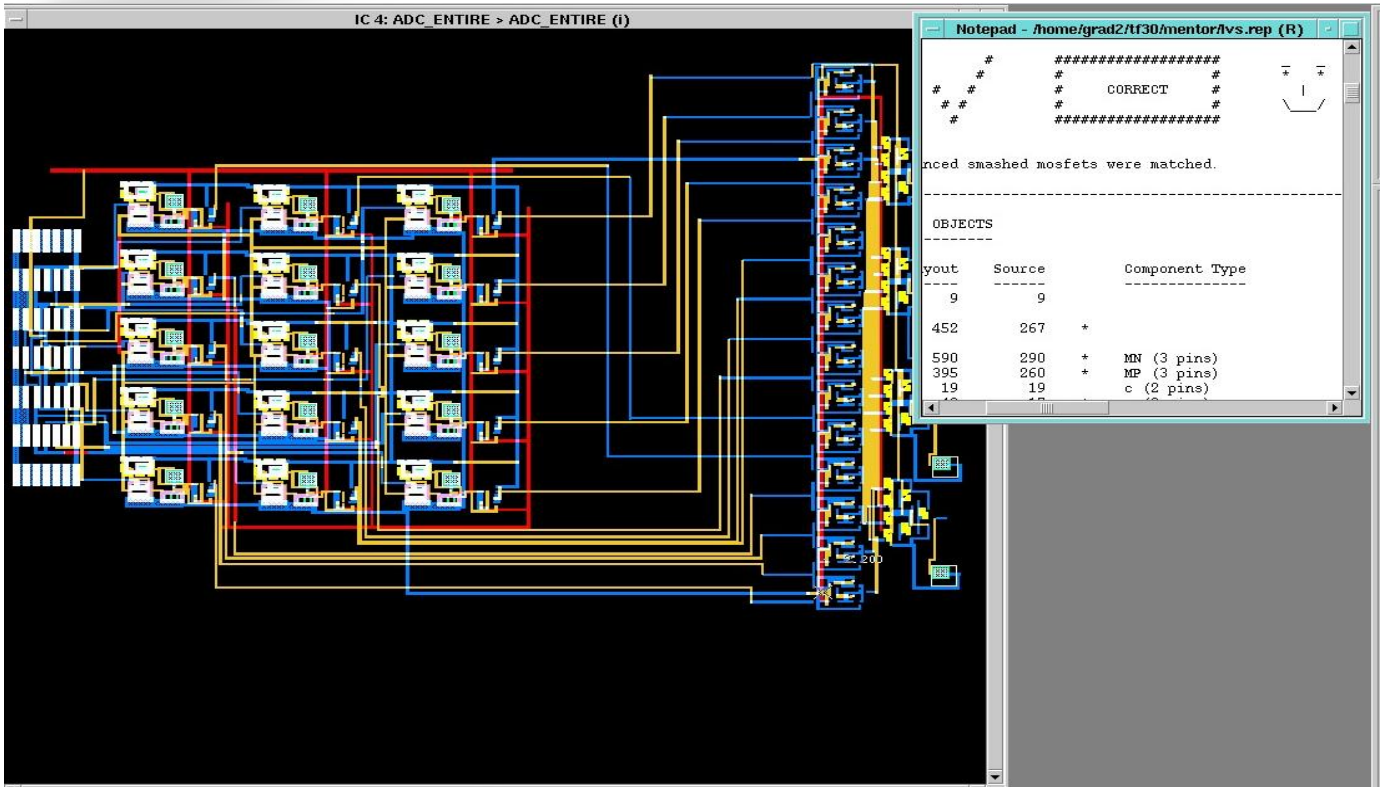
ADC Implementation

- 4-bit ADC Simulation:



ADC Implementation

- 4-bit ADC Layout:



Note : DRC RuleCheck DRC_OFGRID_POLY completed. Result count: 0.
Note : DRC RuleCheck DRC_OFFGRID_ELECTRODE completed. Result count: 0.
Note : DRC completed. Total RuleChecks: 120; Total Results: 0; Total Original Geometries: 56609; CPU Time: 0.84, REAL Time: 0.905858.

ADC Implementation

- ADC Specification:

-- Comparator-stage:

---8x15=120 transistors

---19 resistors

---15 capacitors

-- Latch: 8x15=120 transistors

-- Encoder-stage: 28x3+12x14=252 transistors

--ADC (total):

---492 transistors

---19 resistors

---15 capacitors

--Area of layout = 4.1mm*2.6mm=10.66(mm)^2


Thank you