

4-bit ADC/DAC Design

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Introduction

DAC Implementation

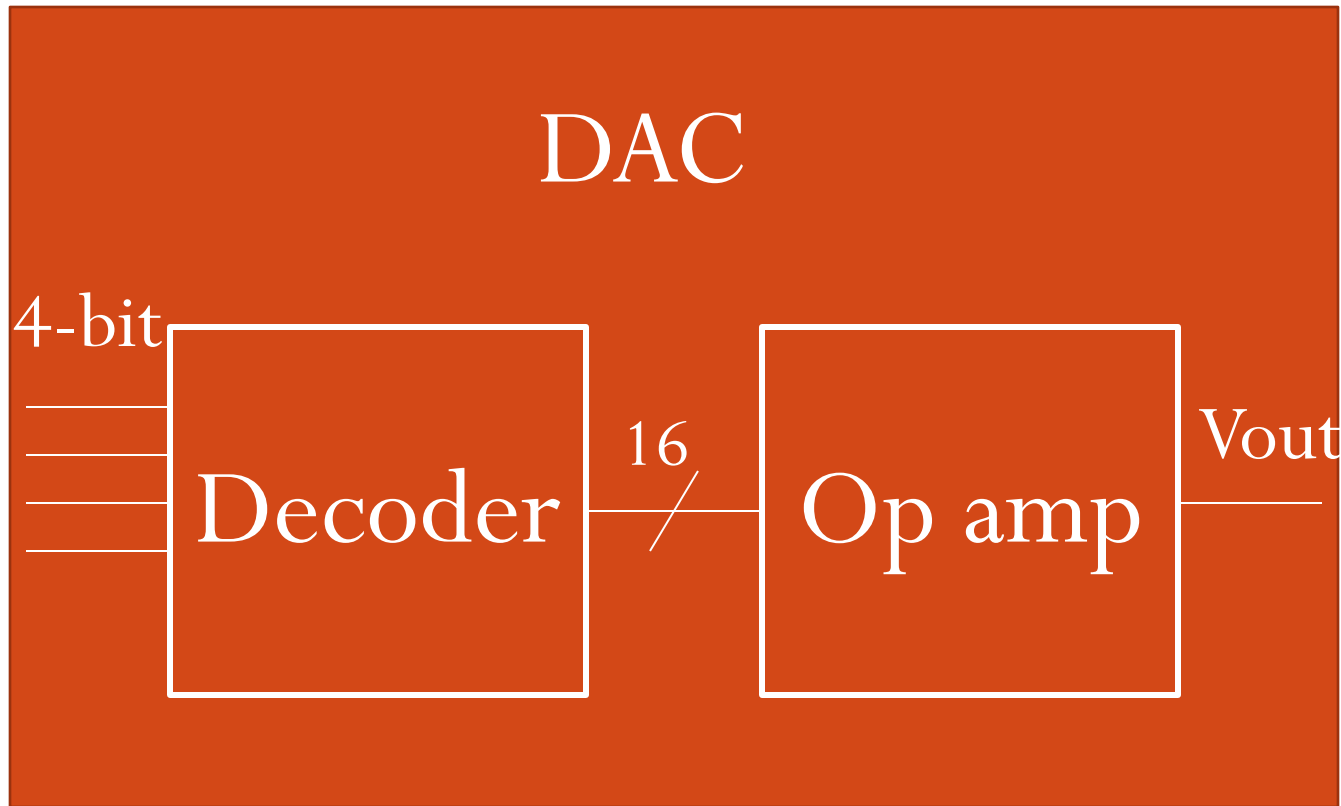
ADC Implementation

Introduction

- This design is divided into two devices: an **ADC** and a **DAC**.
- The **ADC** is composed of a comparator stage and an encoder stage.
 - The comparator stage discretizes an analog input voltage.
 - The encoder stage encodes the discrete values into a digital 4-bit binary word.
- The **DAC** is made up of decoder and operational amplifier.
 - The decoder is made up of 16 4-input NANDs.
 - The Op amp amplifies the decoded signals and transfers them to the output.

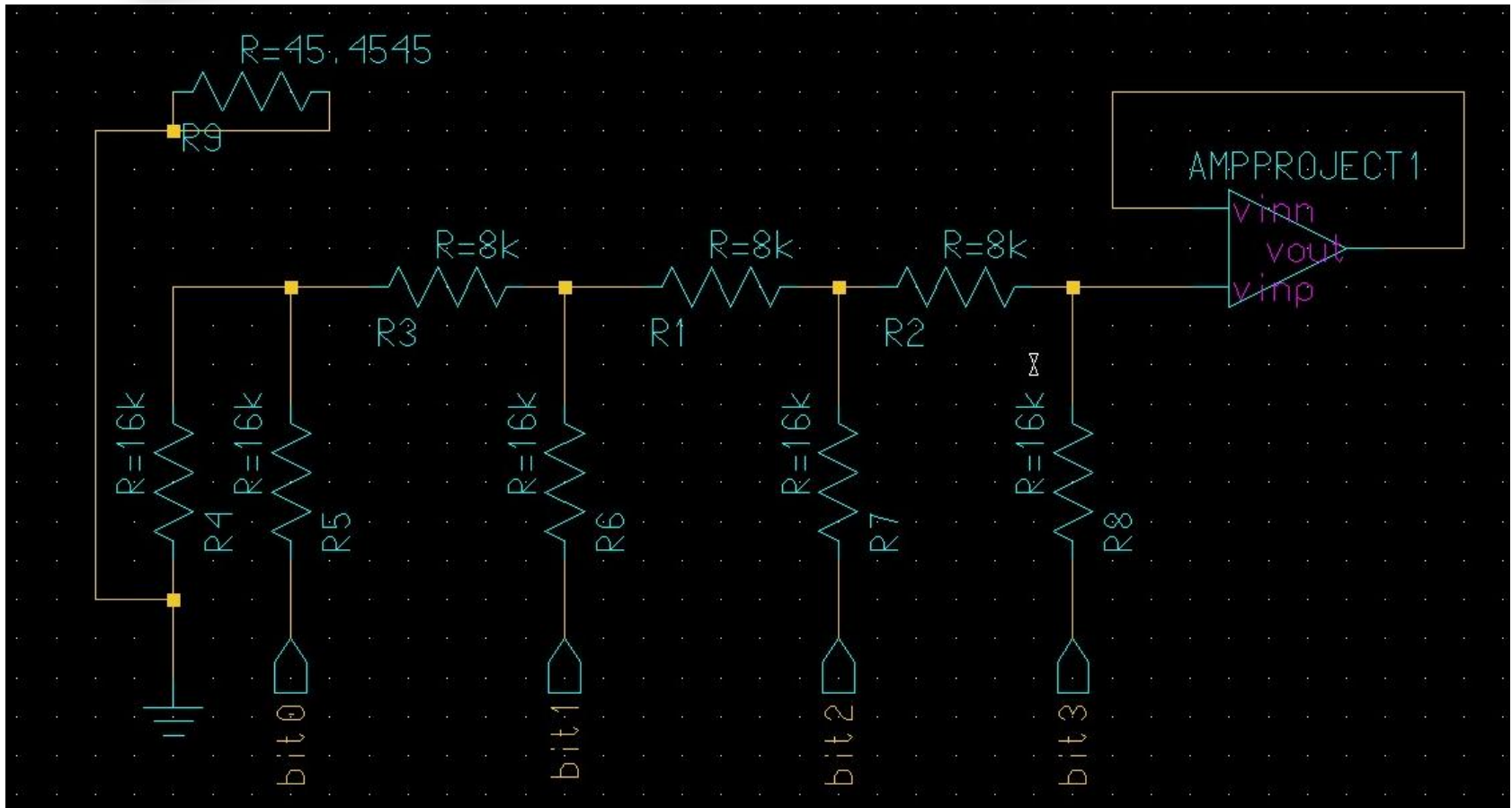
DAC Implementation

- Block Diagram



DAC Implementation

- R-2R DAC



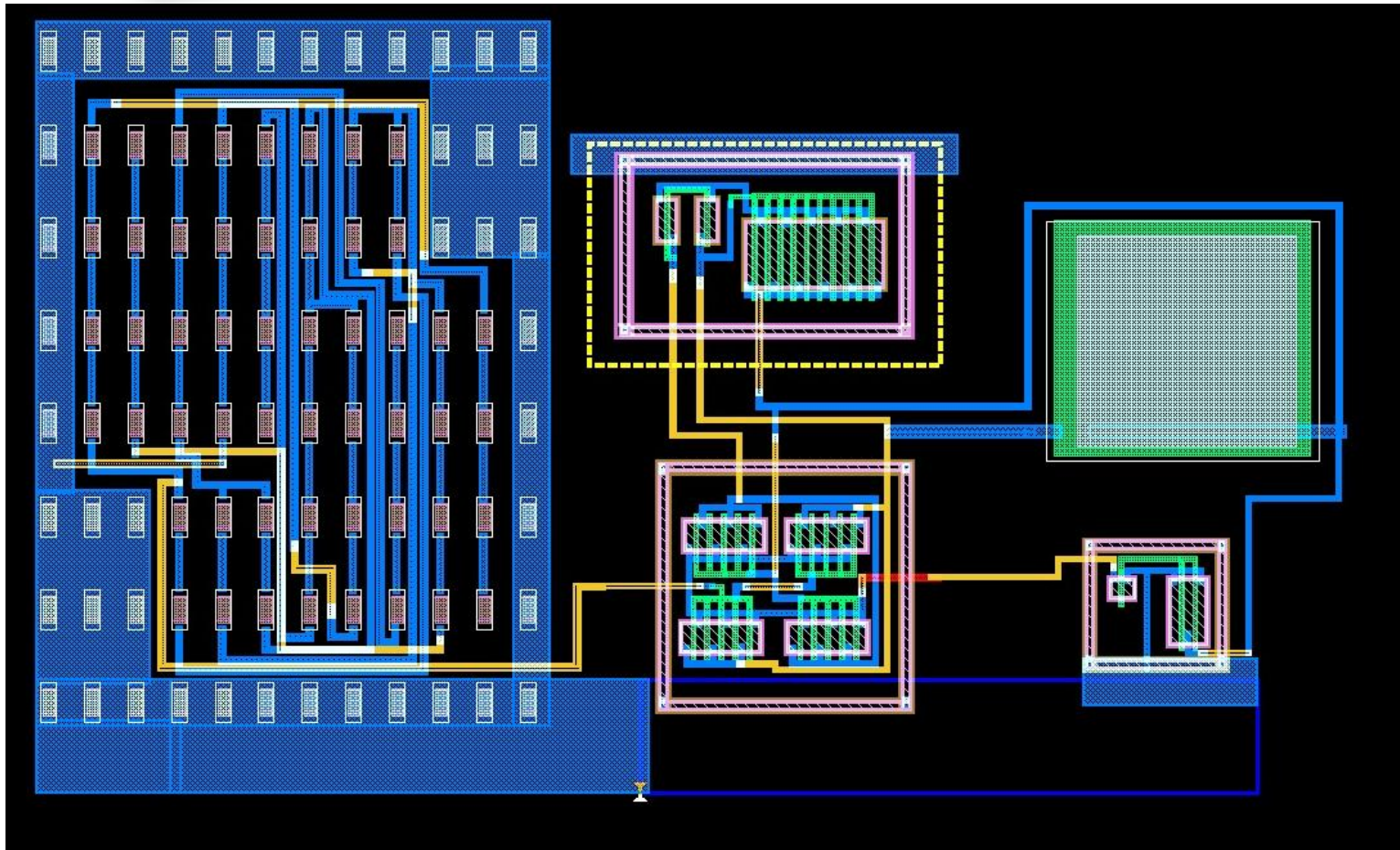
DAC Implementation

- R-2R DAC Simulation:



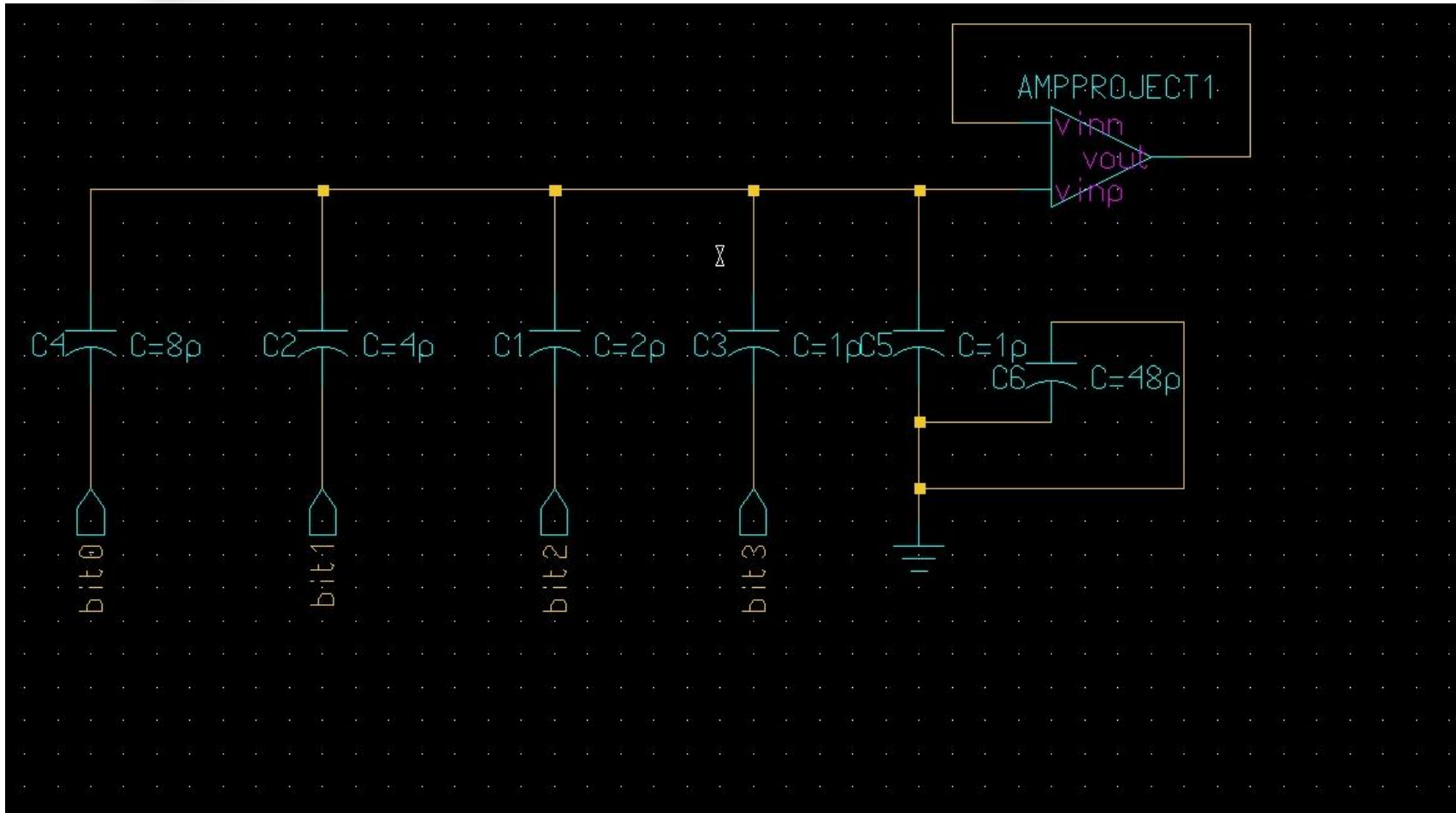
DAC Implementation

- R-2R DAC Layout:



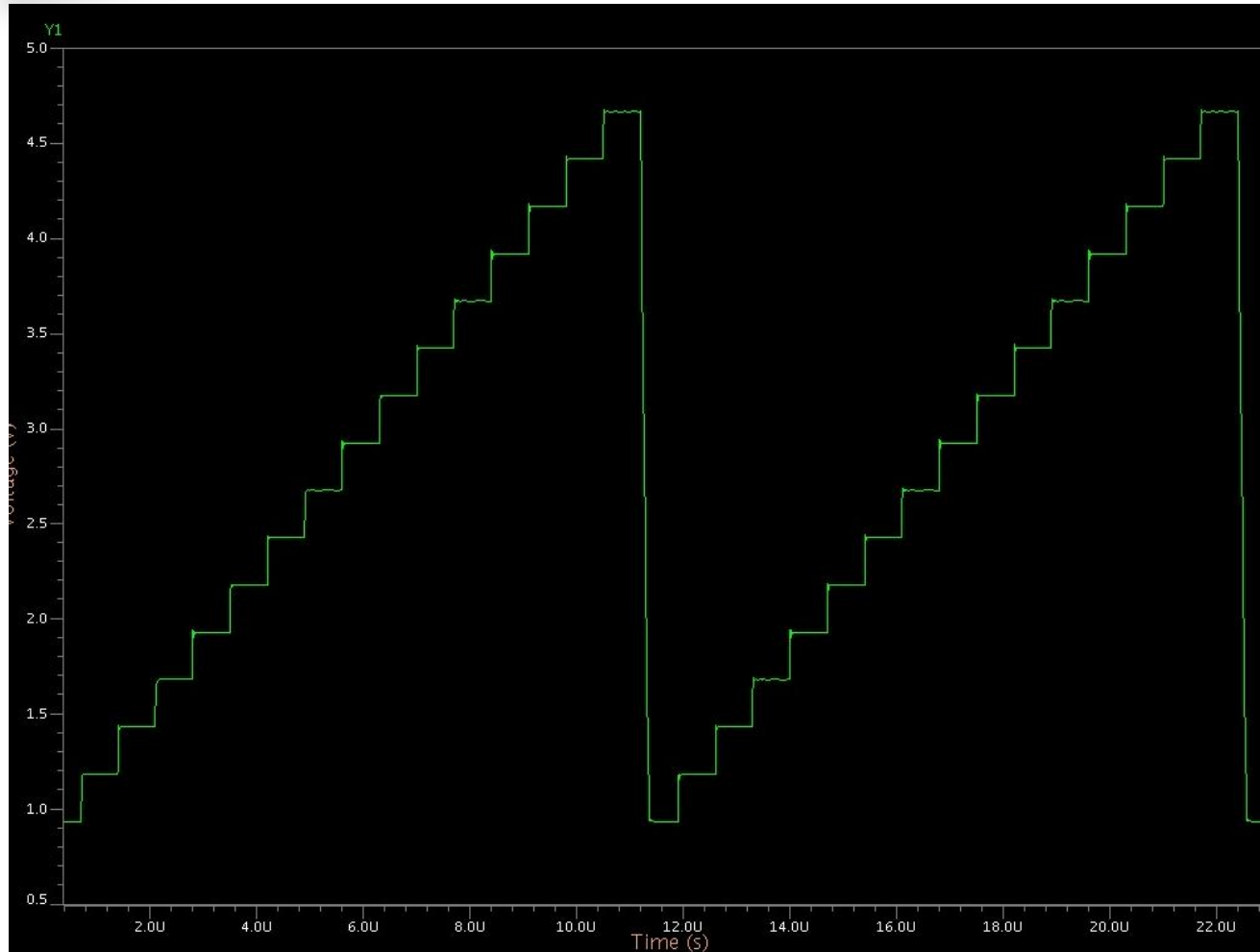
DAC Implementation

- Charge Scaling DAC



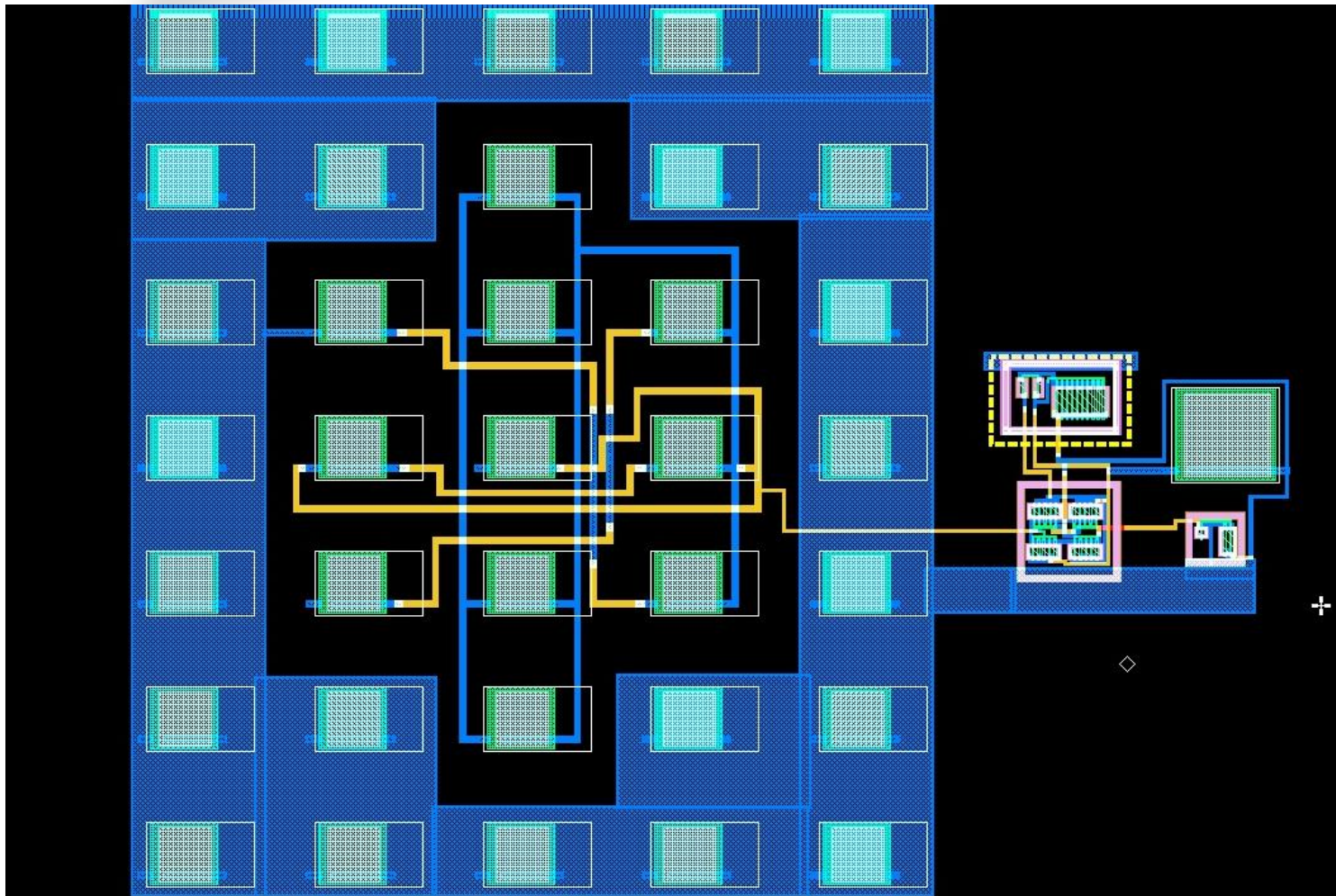
DAC Implementation

- Charge Scaling DAC Simulation:



DAC Implementation

- Charge Scaling DAC Layout:



DAC Implementation

- DAC Specification:

- R-2R DAC:

- 7 transistors

- 10 resistors

- 1 capacitor

- Area of layout = $300\mu\text{m} \times 500\mu\text{m} = 0.15(\text{mm})^2$

- Charge Scaling DAC:

- 7 transistors

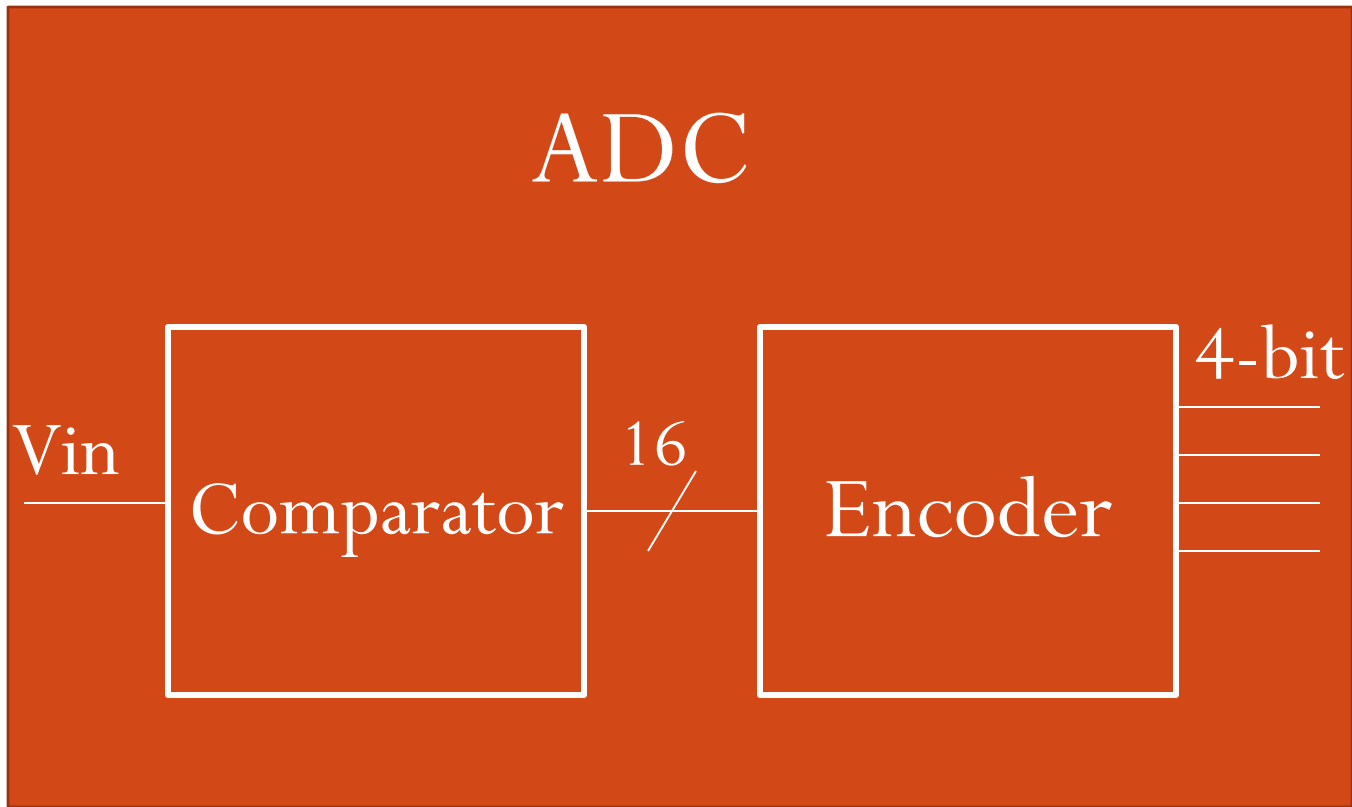
- 1 resistor

- 7 capacitors

- Area of layout = $1100\mu\text{m} \times 840\mu\text{m} = 0.924(\text{mm})^2$

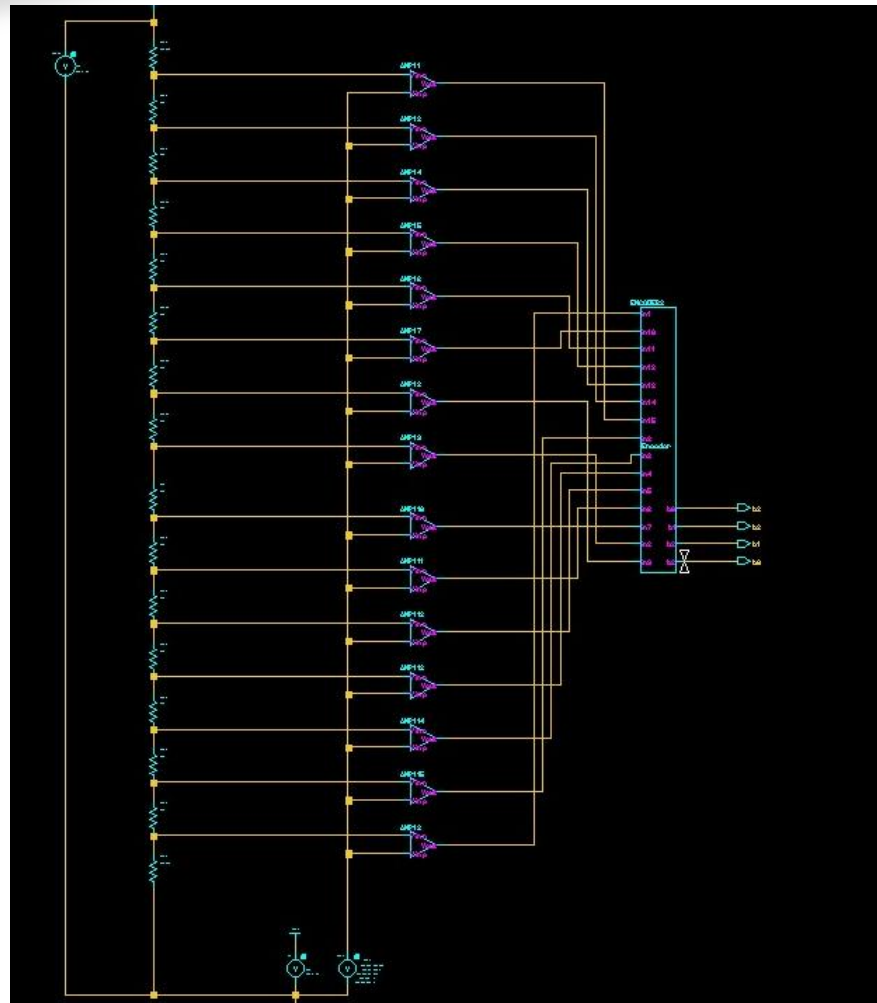
ADC Implementation

- Block Diagram



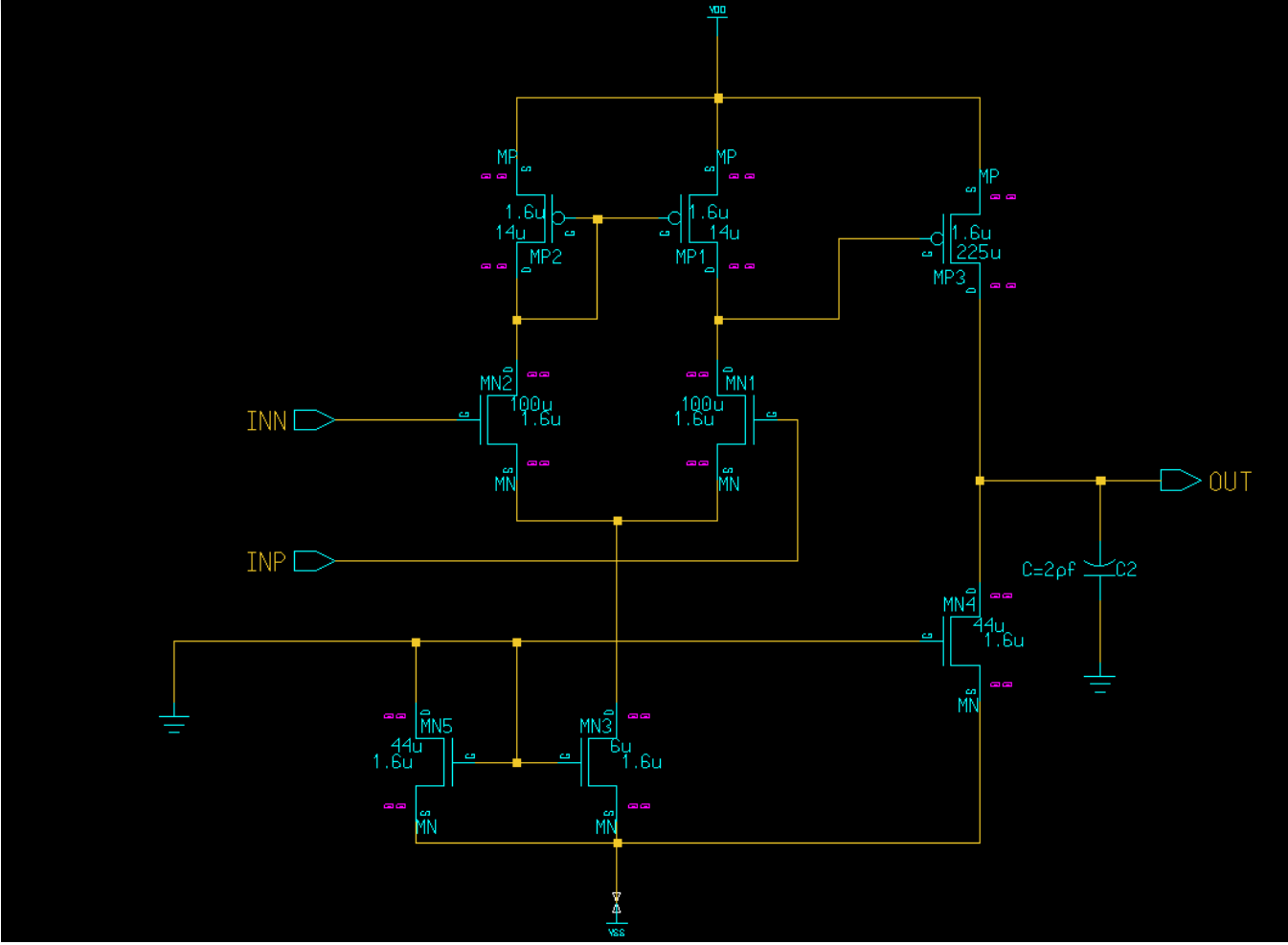
ADC Implementation

- Top View



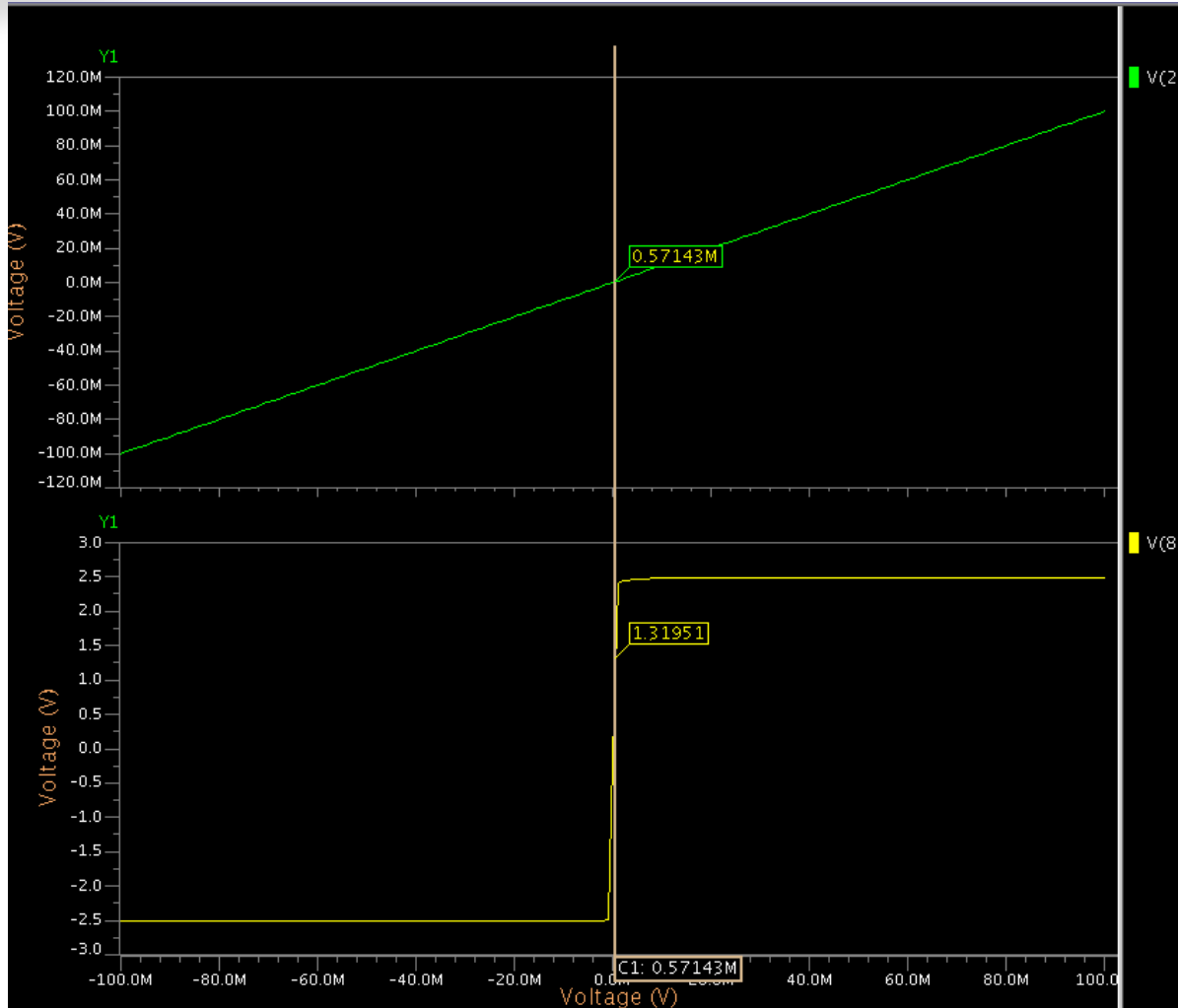
ADC Implementation

- op amp for ADC



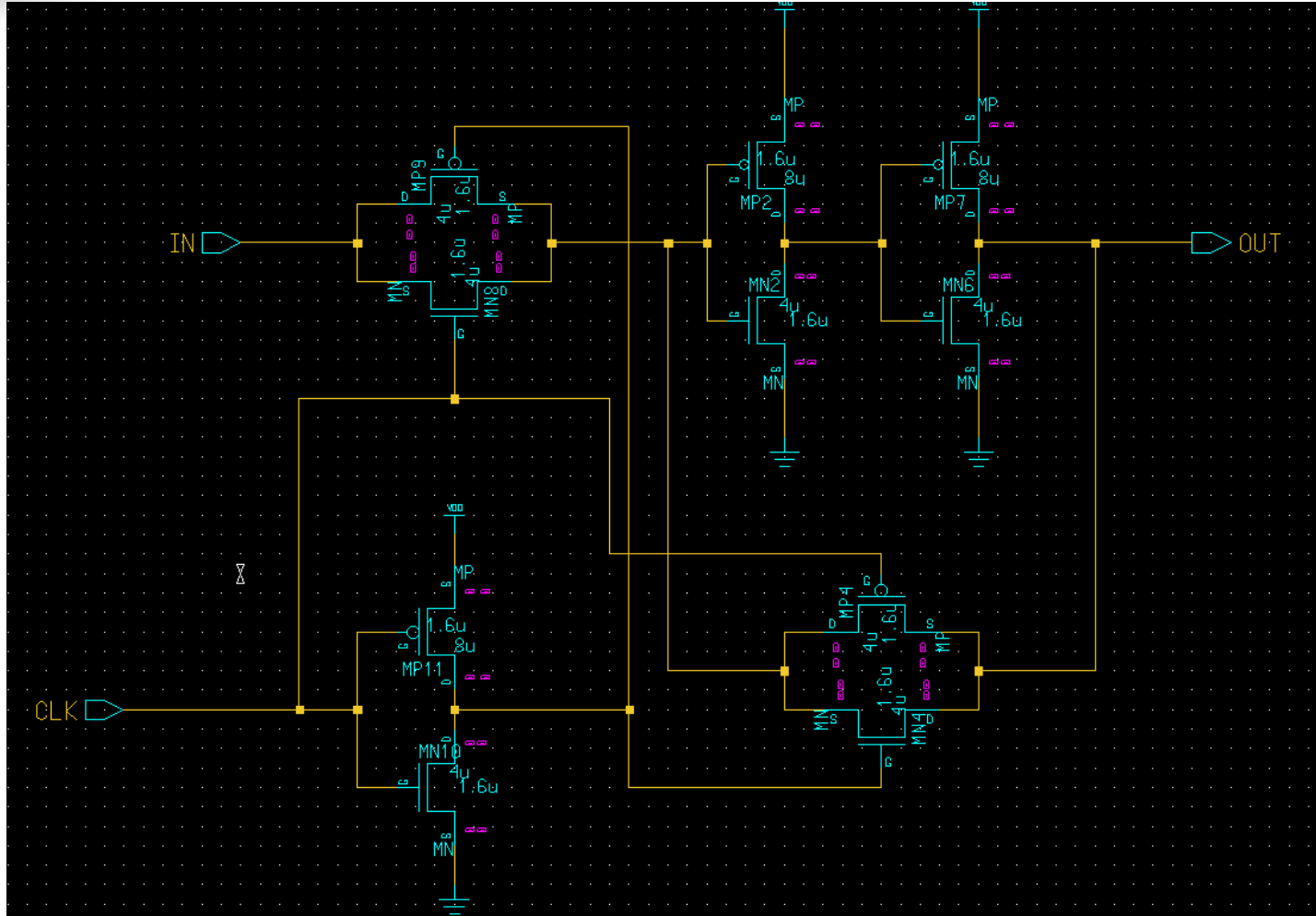
ADC Implementation

- Simulation: op amp



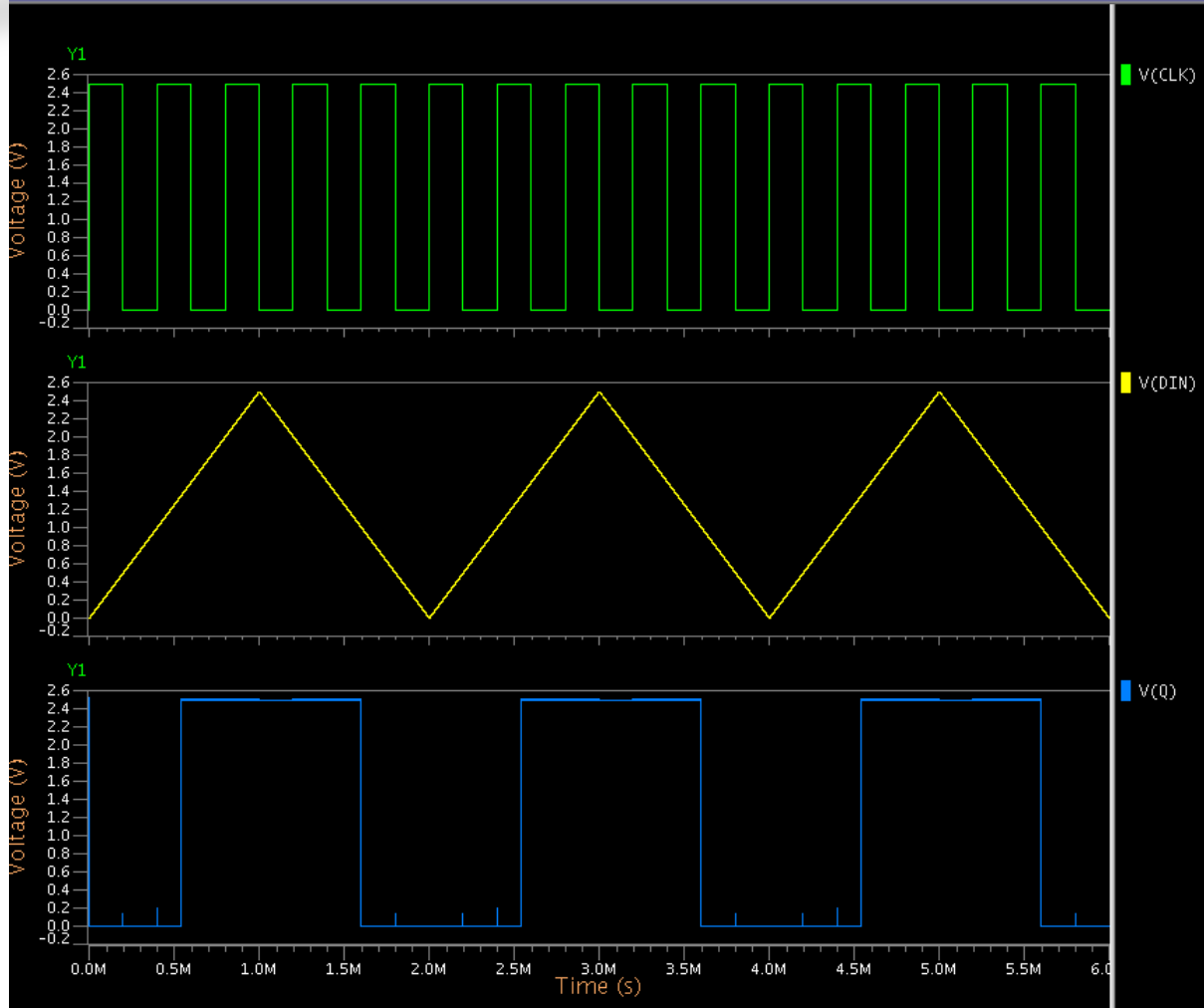
ADC Implementation

- Latch:



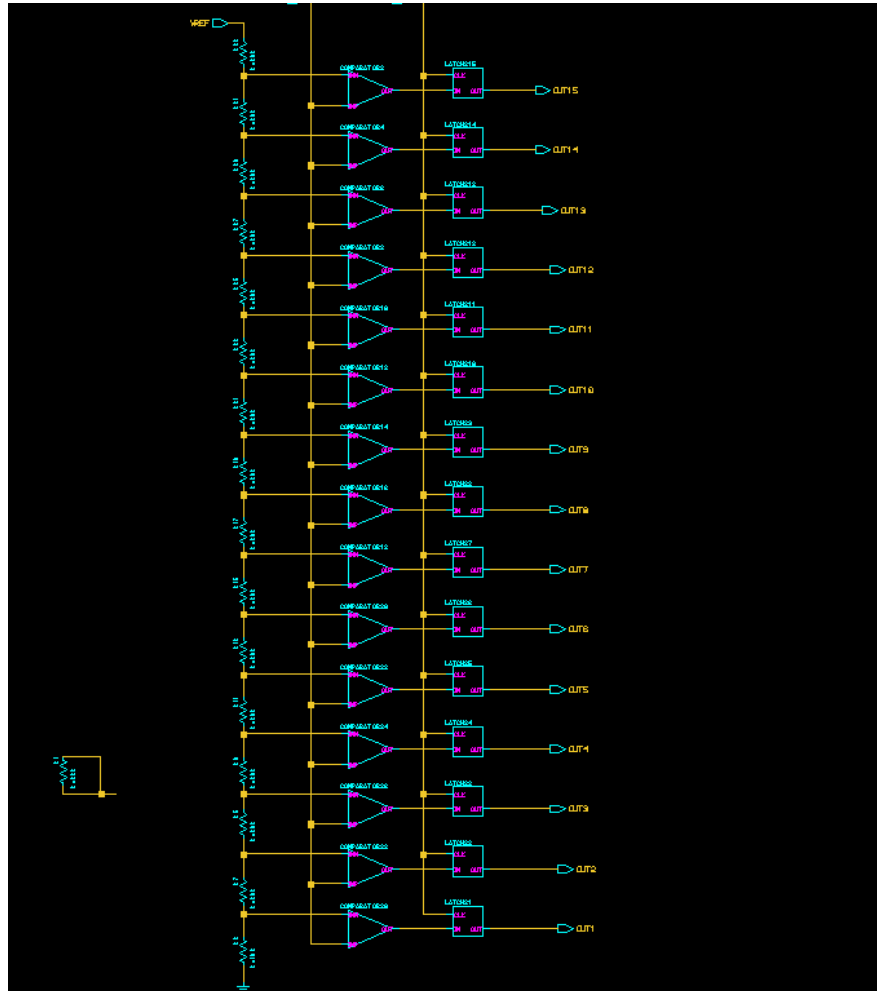
ADC Implementation

- Simulation: latch



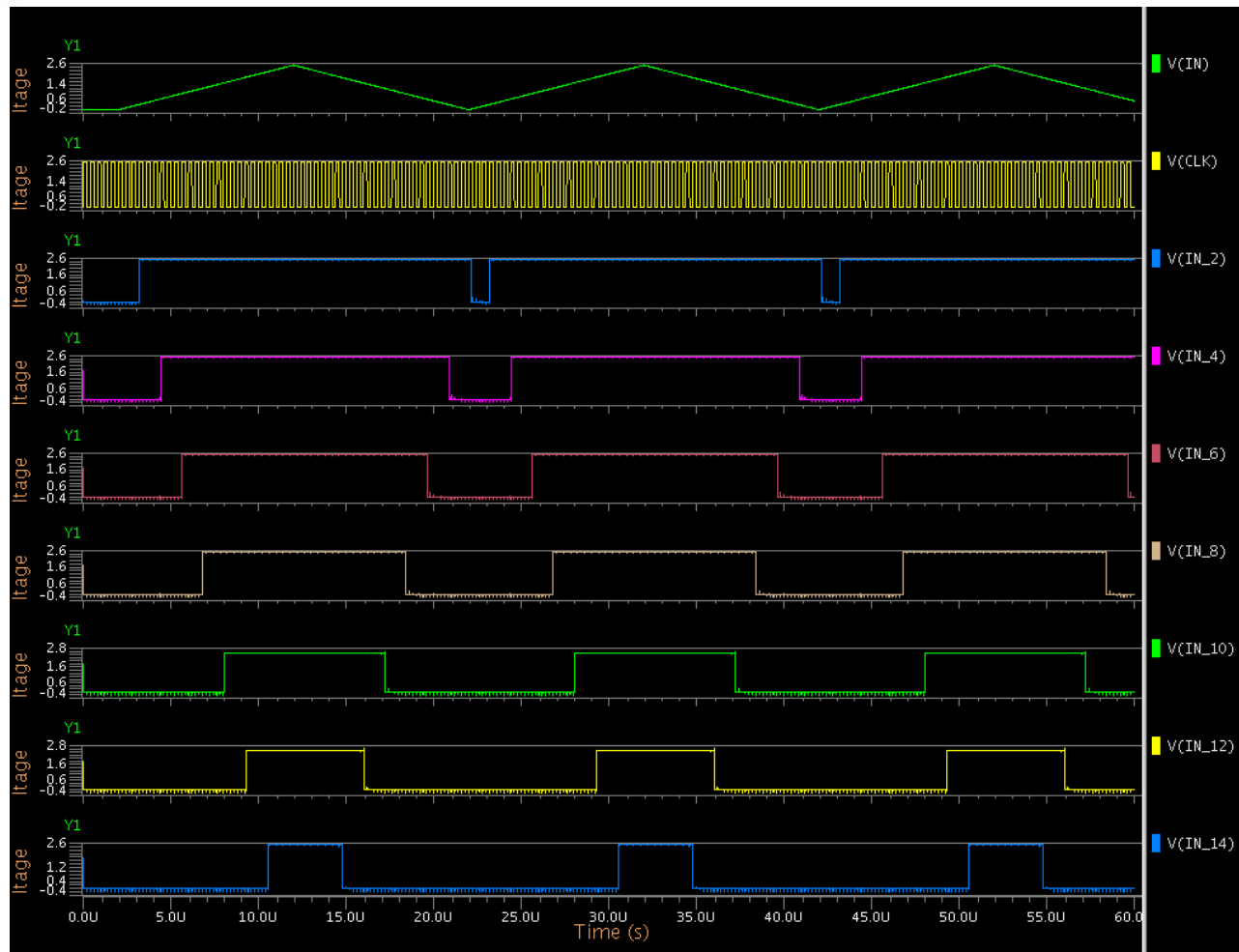
ADC Implementation

- Comparator: op amp + latch



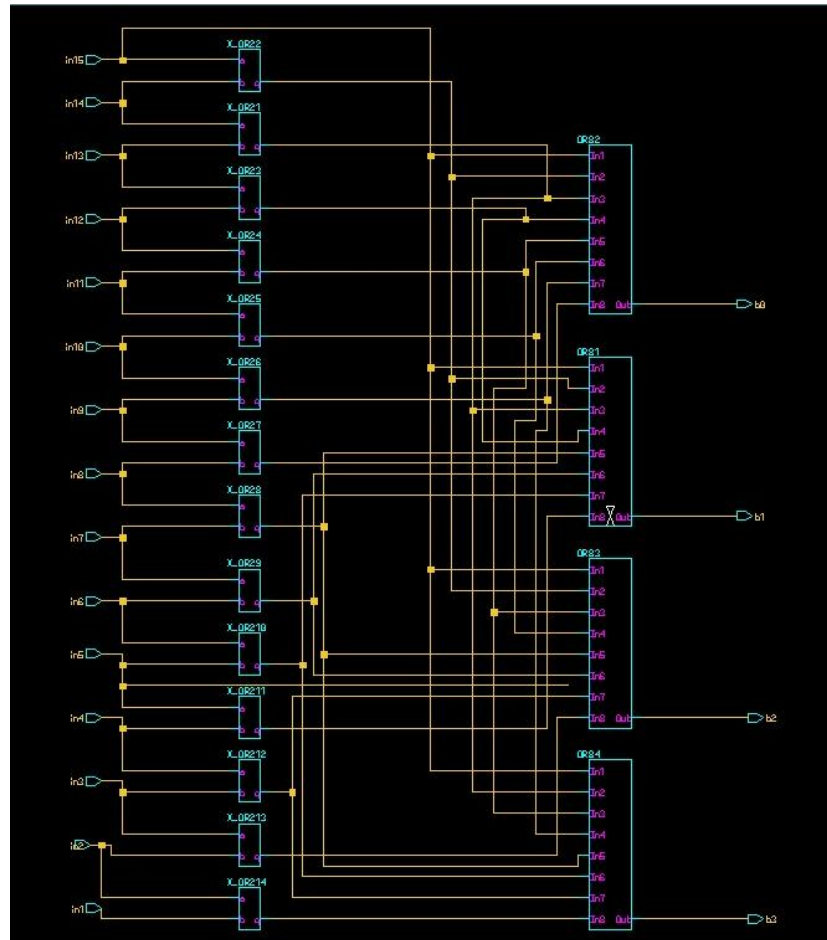
ADC Implementation

- Simulation: Comparator



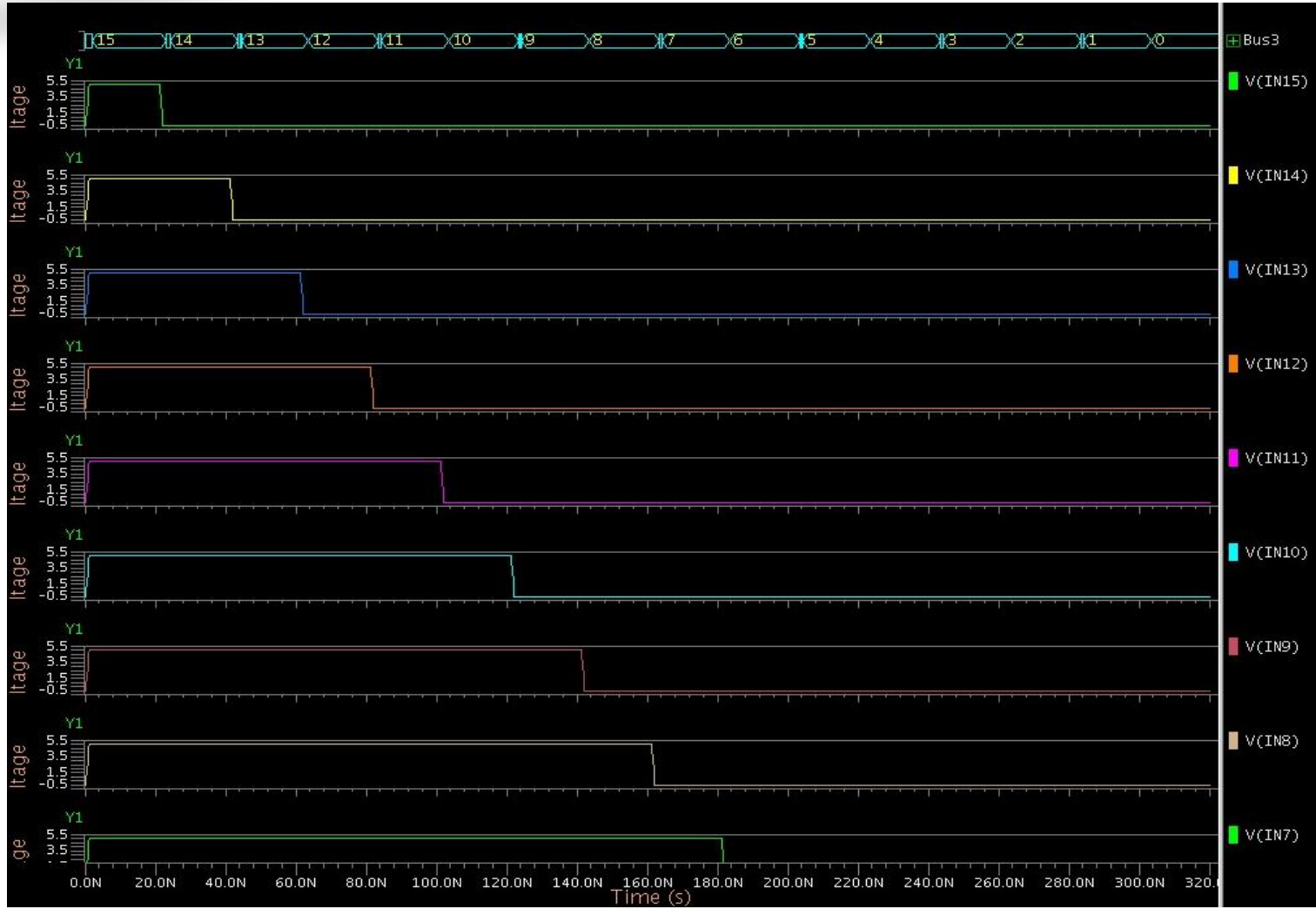
ADC Implementation

- Simulation: encoder



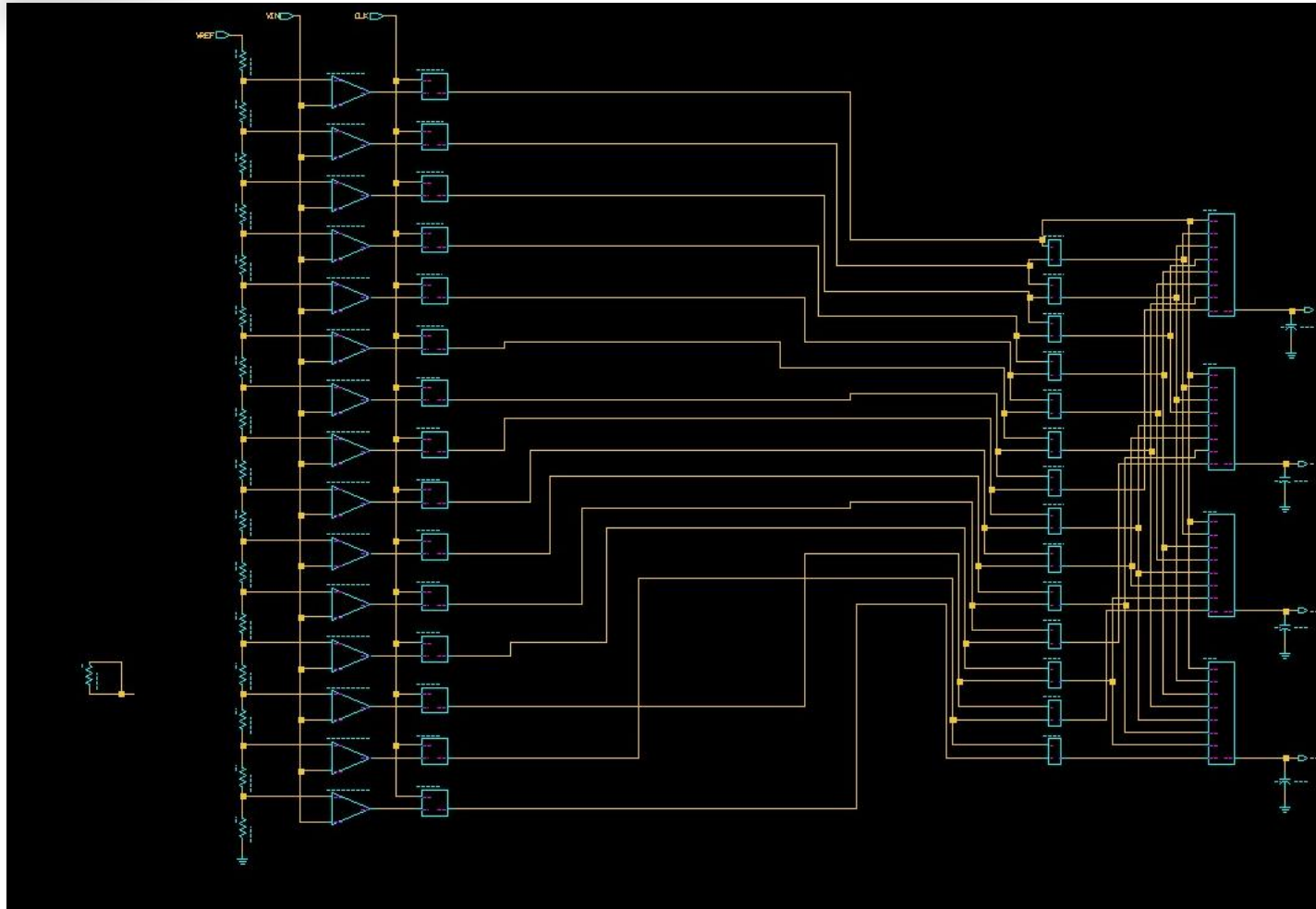
ADC Implementation

- Simulation: encoder



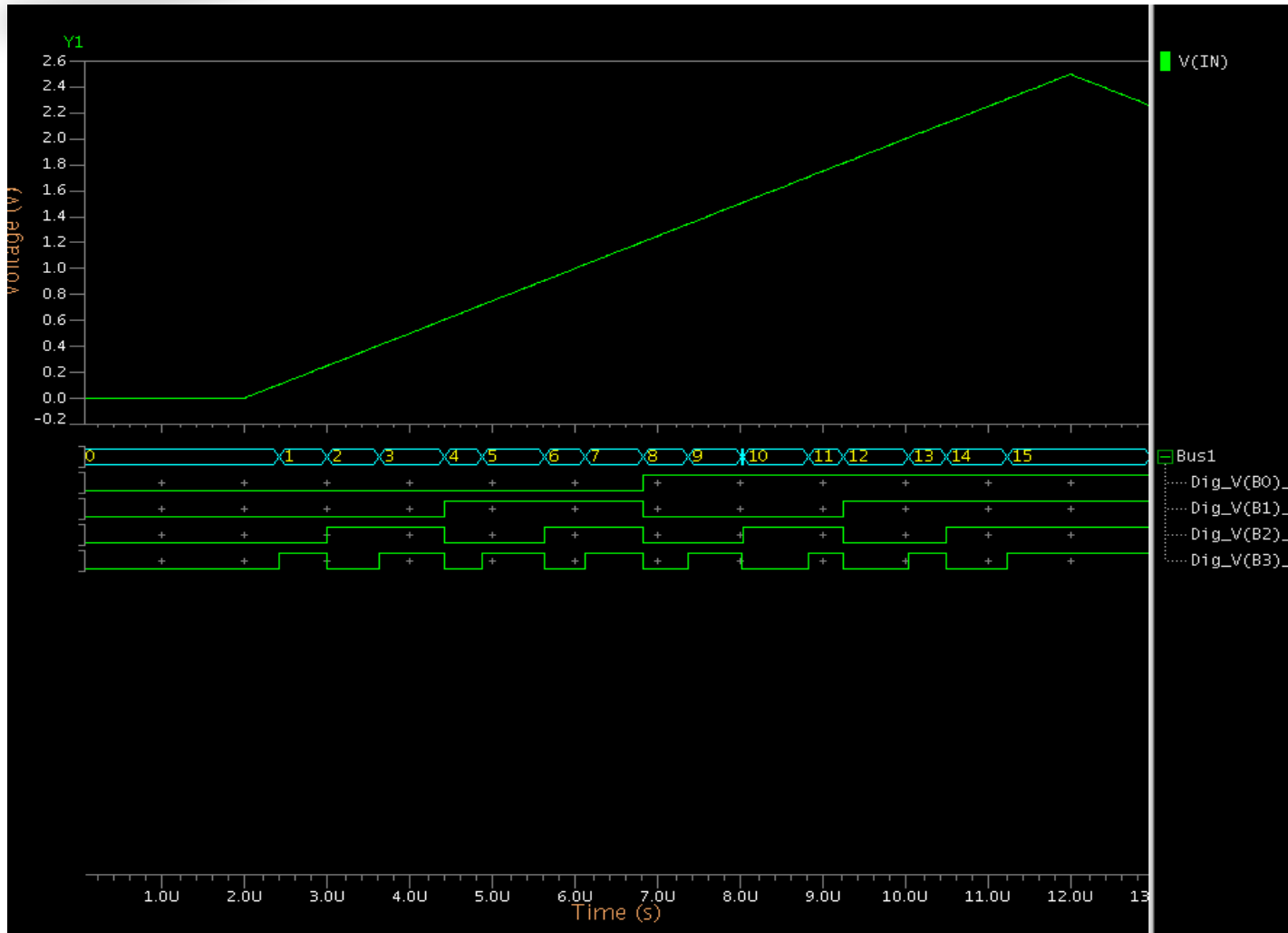
ADC Implementation

- 4-bit ADC



ADC Implementation

- 4-bit ADC Simulation:



ADC Implementation

- 4-bit ADC Layout:

The image shows a PCB layout software interface. The main window displays a complex circuit board layout with various components and routing paths. A Notepad window is open in the foreground, showing the output of a Design Rule Check (DRC). The Notepad window title is "Notepad - /home/grad2/tf30/mentor/1vs.rep (R)". The text in the Notepad window is as follows:

```
#####  
# CORRECT #  
#####  
nced smashed mosfets were matched.  
-----  
OBJECTS  
-----  
yout Source Component Type  
-----  
9 9  
452 267 *  
590 290 * MN (3 pins)  
395 260 * MP (3 pins)  
19 19 c (2 pins)
```

Note : DRC RuleCheck DRC_OFGRID_POLY completed. Result count: 0.
Note : DRC RuleCheck DRC_OFFGRID_ELECTNODE completed. Result count: 0.
Note : DRC completed. Total RuleChecks: 120; Total Results: 0; Total Original Geometries: 56609; CPU Time: 0.84, REAL Time: 0.905858.

ADC Implementation

- ADC Specification:

- Comparator-stage:

- $8 \times 15 = 120$ transistors

- 19 resistors

- 15 capacitors

- Latch: $8 \times 15 = 120$ transistors

- Encoder-stage: $28 \times 3 + 12 \times 14 = 252$ transistors

- ADC (total):

- 492 transistors

- 19 resistors

- 15 capacitors

- Area of layout = $4.1 \text{mm} \times 2.6 \text{mm} = 10.66 (\text{mm})^2$

A 3D-style orange button with the text "Thank you" in white. The button is rectangular with rounded corners and a slight shadow, giving it a three-dimensional appearance. The text is centered on the button and is written in a clean, sans-serif font.

Thank you