Parallel Amplifiers for 3D Ultrasonic Imaging

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April 29, 2009
Overview

• Highly parallel low-noise preamps
• First level of amplification seen by transformed voltage (mV)
• Output stage matches $Z_{in}$ of scanner
Block diagram

$V_r$

Op amp

Buffer

Protection circuit

To scanner front end

Common mode noise rejection

Source follower (common drain)

$Z_{out}$ to match front end of scanner

Protect against reverse bias due to shared elements

128 channel
Amplifier Design

- Two-stage OTA design
- Design procedure of Allen and Holberg
  - Diff. pair with output stage, negative feedback
- Design specs include:
  - 100 $\mu$A tail current on M5
  - GB = 25 MHz
  - Drive output buffer (2 pF)
  - Gain of 9-12 dB
  - Phase margin $60^\circ$-$80^\circ$
Single-channel amplifier schematic
DC and Transient Analyses

**DC**
- Reveals all devices in sat.
- Produces desired tail current

**Transient**
- 11.9 dB gain
- Input signal:
  - amplitude at 1 mV, 5 mV, 10 mV
  - 2.5 MHz
- Approximate real-world input as sine wave
Measured input signal

Measured output voltage from single piezoelectric element in pitch-catch experiment
AC Analysis

- Parameters
  - Everything driven at 2.5 MHz, but transducers exhibit broadband response
  - Imaging system drops off beyond 3.0 MHz
  - Achieving even higher BW desirable for other apps, but not necessary here
    - Decreasing $C_C$
    - Increase W/L of M1, M2 (n-devices of diff. pair)
AC Analysis

Gain margin: -19.4°
Phase margin: 78.8°
Complete 1-channel schematic

Drive scanner front-end (20 kΩ, 3pF)
Output buffer (Source follower)
Design results

- 11.8 dB gain
- 96 $\mu$A diff. pair tail current
- GB = 29 MHz
- Gain margin: -19.4°
- Phase margin: 78.8°
- Drive scanner front-end impedance
- Handles desired voltage ranges
- Power dissipated 18.3 mW (Eldo sim)
Layout considerations

• Low noise extremely important
  – Ground traces between signal traces
• Folding, multifinger transistors
• Estimated 1-channel area 5340 $\mu m^2$
  – Based on known W/L ratios and min. gate length, known R and C values
  – Estimated area for spacing and ground traces
  – Suggests adequate room for multi-channel
• Create replicable unit cell
Primitive floorplan

GND

NMOS

C

PMOS

VDD
Completed Layout

- Individual project
- From-scratch layout
- Common centroid resistors, capacitors
- Multifinger transistors
- Some potential for area reduction remains
DRC and LVS

DRC clean

Note: DRC RuleCheck DRC_OFFGRID_POLY completed. Result count: 0.
Note: DRC RuleCheck DRC_OFFGRID_ELECTRODE completed. Result count: 0.
**Note: DRC completed. Total Rule Checks: 120, Total Results: 0.** Total Original Geometries: 3633; CPU Time: 0.11, REAL Time: 0.133072.

LVS, 0% tolerance

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<th>LAYOUT</th>
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<th>ERROR</th>
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LVS, 1% tolerance

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DUKE ECE

DUKE BME
Duke 3DUS preamp

GND

VDD

LVS

INITIAL NUMBERS OF OBJECTS

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NUMBERS OF OBJECTS AFTER TRANSFORMATION

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* = Number of objects in layout different from number in source
16 channel spread
16 channel spread

- Replicated of single channel module
- Ground planes between each channel
- 8 of these for desired amp
- DRC clean
Chip area, 16 channels

- $1493.6 \text{ \mu m} \times 1935.2 \text{ \mu m}$
- $2.89 \text{ mm}^2$
- Quite large (1 chan: $180,650 \text{ \mu m}^2$)
Remaining Improvements

• Additional simulation/analog design preferred before fabrication
• Subsequent layout
• Protection circuit design
  – Simulations run modeled on protection circuit (diode-based) implemented in ultrasound scanner
• Perform detailed loaded/unloaded scanner impedance measurements
  – Piezocad matching network simulations
Conclusions, abilities

• Layout under control
• Design and simulation improving
• Modular layout exhibited
• Still room for improvement on combining analog design elements
• Capable of executing design/layout process