Phase-Locked Loop (PLL)

Yang ZHAO

ECE262
April 29, 2009
Block Diagram

- Phase Locking: aligning the output phase of the VCO with the reference phase;
  \[ \omega_{\text{out}} = \omega_{\text{in}}; \frac{d \Phi_{\text{out}}}{dt} - \frac{d \Phi_{\text{in}}}{dt} = 0 \]
- Phase detector; Charge Pump; VCO
Block Diagram

- Phase Detector: average output $V_{out}$ is linearly proportional to phase difference $\Delta \Phi$ between two inputs;

- VCO: output frequency is a linear function of control voltage

$$\omega_{out} = \omega_0 + K_{vco} V_{control}$$
Phase Detector & Charge Pump & Loop Filter

- Dual D flip-flop PD; low pass filter
Phase Detector

- Full schematic
Phase Detector

- DFF schematic
Phase Detector

- Simulation: $V(REF)$ is ahead of $V(OUR)$
Phase detector

- Full Layout
- DFF Layout
Phase Detector

- LVS clean
VCO

- Full schematic
VCO

- Delay unit schematic
VCO Frequency Sweep
Conclusions & Challenges

- Finish the schematic and simulation for phase detector and VCO (two core device in PLL)
- Finish layout for phase detector (DRC and LVS clean)
- The challenge is to obtain correct simulation for VCO