ECE 262 Analog Integrated Circuit Design

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Project Report

“Fully differential Opamp using Replica Amplifier Method”

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**Abstract:** In this project, we have designed a fully differential Opamp using a replica amplifier method. The design consists of two amplifiers namely the Main Amplifier and the Replica Amplifier, which is essentially the same as the main amplifier. The main amplifier is designed using a cascade stage coupled with a Common Source stage. The purpose of using this method is to achieve high bandwidth, high gain without compromising on the output voltage swing. The main amplifier is designed to obtain a high bandwidth without bothering about the gain achieved. In comparison, the replica amplifier is designed to achieve a high gain output. This design is essentially beneficial for low voltage operation. Traditional methods of have made use of cascade design to achieve high gain by increasing output resistance. However it was not applicable for low voltage applications due to the limited rail to rail supply present. This design benefits from no reduction in output swing and still manages to achieve high gain.

**SPECIFICATIONS:**

**OPAMP Performance**

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.5u CMOS</th>
</tr>
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<tbody>
<tr>
<td>Power Supply</td>
<td>5V</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>80.36</td>
</tr>
<tr>
<td>Output swing</td>
<td>~1V from either rail</td>
</tr>
<tr>
<td>Bandwidth (3dB)</td>
<td>7.73 Mhz</td>
</tr>
<tr>
<td>Power dissipated</td>
<td>46.3176 mW</td>
</tr>
</tbody>
</table>
The above figure shows the fully differential OPAMP including the main amplifier and the replica amplifier. The output from the common source of the main amplifier is used as the input for the differential pair of the replica amplifier.
Figure 2 shows the details of the main amplifier design which is also common to the replica amplifier. The design includes an input differential stage to the cascade. The cascade stage is fed to a common source stage. The W/L of the various MOSs of the cascade are as follows.

MP1, MP3 (W/L): 20

MP2, MP4 (W/L): 10

MN1, MN3 (W/L): 5

MN2, MN4 (W/L): 15
The differential pair is fed a biased DC voltage of 3V and the W/L is 30 for the MOS pair and 20 for the tail MOS.

The CS stage has W/L for PMOS as 35 and for NMOS as 20. The bias voltages are as follows:

MP1, MP3: 2.5V

MP2, MP4: 2V

MN1, MN3: 2V

MN2, MN4: 1.2V

LAYOUT:

Fig. Layout of the main and replica amplifier
Fig. Layout of the main amplifier

The layouts have successfully passed the DRC test.
SIMULATIONS:

Using only the main amplifier we achieved a gain of 37dB and a bandwidth of 11MHz for a load of 93.4fF. After using the replica amplifier we have seen a gain of 80.38dB and a bandwidth of 7.733 MHz.
Fig. Transient simulations

The transient simulation shows a high output swing of around 1V which is better than the expected value.
**Currents and Voltages:** (Devices labeled as Fig 2 from Schematic Section)

The following screen shots show the currents and voltages across the various MOS devices being used.

![Diagram of MOS devices](image)

**Fig1.** Devices MP3 and MP4
Fig. 2 Devices MP1 and MP2
Fig3. Devices MN1 and differential pair NMOS.
Fig4. Devices MN3 and diff pair NMOS.
Fig5. Device NMOS from tail region
Fig6. Devices NMOS and PMOS from Common Source region
Conclusion to Design Challenges:

1. The biggest challenge was to achieve a high bandwidth as was expected from this design. It was difficult to design the main amplifier parameters to give a high bandwidth. Designing for a high gain was relatively easier and replica amplifier was close to the expected value in this regard.

2. Also the design was intended to give a high output swing, which is a major challenge for low voltage applications. The original design was intended to work for 0.35u MOS technology and work on a lower voltage. However we have worked on 0.5u MOS technology and a higher voltage of 5V. Although we have managed to achieve a high output swing its benefits are for low voltage applications.

3. Determining the widths and lengths for transistors, especially when theoretical values did not produce the desired currents and node voltages. Balancing the current in the differential input stage and the folded cascade stage was crucial to achieving the amplification.

References:

- “Low voltage fully differential OPAMP with high gain, wide bandwidth suitable for switched capacitor applications” Sherif Hammouda, Mohamed Tawfik, Hani Ragaie, IEEE 2002

- “Design of Analog CMOS Integrated Circuits”, Behzad Razavi