

## **ECE262: Integrated Analog Circuit Design**

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Class Hours: Tues, Thurs 11:40-12:55: Instructor Office hours: Thurs 12:55-1:55

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Prerequisites: ECE261, ECE163 (or based on instructor's consent)

### **Textbooks/References**

B. Razavi, "**Design of Analog CMOS Integrated Circuits**," McGraw Hill, 2001.

P. Allen and D. Holberg, "*CMOS Analog Circuit Design*" Oxford University Press, 1987.

"*STAR-HSPICE User's Manual*" Avant!, Release 1998.2, July 1998(Available in pdf format).

### **Course Objectives**

This course covers the design and layout of cmos integrated analog circuits. Lectures begin with a short review qualitative theory of pn junctions, bipolar and mos devices. and large and small signal models with emphasis on mos. A variety of analog circuits are then described focusing on continuous time operational amplifiers. Frequency response, stability and compensation of the amplifier circuits will also be addressed. Lectures will conclude with special topics lectures on complex analog subsystems such as phase lock loops and A/D and D/A converters, switch capacitor circuits, and active filters. Emphasis of sub-circuit design will include HSpice simulation, layout, extraction and verification and Matlab modeling. All students will use the mixed-signal, full custom VLSI CAD software in the dsil lab for homeworks assignments and projects.

### **Analog Project Design**

Student are required to be involved with the design and layout of a custom analog VLSI device using a .5um analog CMOS process technology for their project. Students will work in project teams of one to three depending on the complexity of their circuit macros and functionality. There will be many checkpoints during the semester to verify the progression of each of your analog macro design. Meeting and passing these checkpoints is crucial in order to successfully complete the project. Completion of the design is an important aspect of the project. Students will have the opportunity to fabricate and test their integrated analog design project over the summer and fall of 2009 using MOSIS instructional accounts. An instructor design review and approval are required for all student projects prior to the project tapeout to MOSIS on 6/5/2009. Individually packaged parts will be received in September. Test reports need to be submitted to MOSIS by December 2009

### **Homeworks and Exams**

There will be 5 homeworks in analog circuit design, analysis and layout using the VLSI CAD tools in the dsil lab. There will be a midterm exam in March and a comprehensive final exam in May.

### **Grading**

Project Design: 20%

Homeworks: 25%

Midterm Exam: 25%

Final Exam: 25%

### **ECE262 Project Information**

A analog macro design project will collectively be decided on prior to individual work groups are set up. You will work in groups of one to three to specify, design, verify, and layout your custom macro on the device. The complexity and functionality of the design is more important than the number of transistors. All projects will take advantage of hierarchy of the sub-macros so that these individual sub-macros can be first implemented and completed for partial credit. Thus, you will have at a minimum, complete sub-macros, rather than an incomplete top level system if time becomes a problem. Your group should discuss your project with the TA (the Teaching Assistant) and myself to check the magnitude and scope of the project, and give any required design assistance if needed. I will require a single project directory containing your macro design at the end of the semester.

There will be several checkpoints during the semester to verify the progress of the design. For each checkpoint, write up a small report describing the project and giving the state of the design and verification. The report should be expanded as progress is made. The final report should discuss 1) the function of the macro, 2) the architecture of the macro, 3) relevant cell designs, 4) the pin map, 5) the size of the macro, 6) meaningful results of testing the design and how the final macro will be tested, and 7) the status of the design. The first checkpoint is to verify that you have a good idea of what you will design, and have a vague idea of how you will design and test it.

For the second checkpoint you should have high-level design complete use Matlab. You should simulate this high-level design to verify the functionality of your design. Also, try to estimate the size of various aspects of the design. The third checkpoint is to verify that the design has progressed to a more detailed level. You must have a more detailed (such as device level) design implemented and tested using Hspice. The detailed operation of your macro must be complete. You should have begun the layout of some cells. The fourth checkpoint is to verify that the design of the circuit modules is complete. The Hspice and netlist tools will be used to simulated the circuits. They should also be simulated thoroughly. The final checkpoint is when the project is due. The entire layout should be complete and tested. All verification tools must have been run(DRC and LVS). The report should be complete and the design should be ready to send in to be fabricated. Note that going from checkpoint 4 to checkpoint 5 is usually not easy. Sometimes cells do not fit together in the proposed floorplan, routine is very complex, or module interfaces are incompatible. Each group will give oral presentations of their project during the last week of school.

**ECE262 Project Checkpoints for 2009****Table 1: Student Design Project Checkpoint**

Date	Task
2/1	analog macro function - what is your team's macro project high-level outline - what functional units are required - how will the design be tested
3/1	detail analog macro specification function high-level system description using Matlab high level design complete; high level simulation initial macro sizing complete: Area, Power, testing of the high-level design
3/15	analog macro specification and floorplan complete - detailed function complete device level design - Mentor schematic complete device simulation complete - Hspice simulation complete macro layout begin - Analog layout of primitive cells
4/10	macro layout and module design complete module testing complete: simulation, static verification
5/1	static verification complete - timing, wells, connectivity project report complete, finish design report submitted with class presentations
5/15*	Embed project into Mini Chip layout and have initial design review
6/1*	Complete Final Design Review of project
8/1*	Complete wirebonding diagram and tapeout device to MOSIS
10/15*	Setup proto test board and create test plan for device
11/1*	Receive packaged devices at Duke University
12/1*	Submit On-line test report to MOSIS

\*Required for ECE262 students who plan to fabricate and test their design projects

Some analog project ideas:

Low power clock generation circuit using off chip crystal.  
High Order Active Filters; Analog Phase Lock Loop (PLL)  
5-bit Flash A/D converter 100Mhz, or D/A converter; 10-bit Audio A/D converter  
Switch Capacitor Bandpass Filters; DC-DC Converter  
High Gain Audio Amplifier with analog selector  
10 MS/s Modem Transceiver; Sigma Delta A/D converter

ECE262 Course Outline

Section 1: Integrated Analog CMOS Fundamentals

Week 1) Introduction

Overview of Integrated Analog Circuits  
Effects VLSI Technology Evolution on Analog Circuit Design  
BJT/MOS Physics, CMOS Device Models, Small Signal Model,  
CMOS Current Mirror/Source Follower Amplifier  
Common-sources Amplifier

Week 2) Analog CMOS Process and Layout Techniques

.5uM Process Specifications, CMOS Processing Steps  
Passive Components (Resistors, Capacitors, Inductors)  
Layout Matching and Common Centroid Techniques  
Parasitic Extraction  
Mixed Signal Guard Rings

Week 3) Basic OPamp Design and Compensation

Two-Stage Operational Amplifier  
Feedback and Compensation

Week 4-5) Advanced Current Mirrors and Opamps

Folded Cascode  
Fully Differential Opamp  
Rail to Rail  
Class AB  
Common Mode Feedback Circuits

Week 6) Noise Sources

Thermal, Flicker, Shot, Substrate, Power Supply, etc.  
Modeling Techniques  
Noise Analysis Examples

Week 7) Midterm and Project Presentations

## Section II: Analog Subsystems and Circuits

### Week 8) Comparators and Voltage Reference Circuits

Simple Opamp Comparator, Latched Comparators  
Bias Generators and BandGaps

### Week 9) Switched Capacitor Circuits

Operation and Analysis  
First Order Integrators and Gain Circuits  
Biquad Filters

### Week 10-11) A/D Conversion Techniques

Ideal A/D converter, Quantization Noise  
Nyquist Rate Sampling A/Ds  
Integrating, Successive Approximation  
Flash A/Ds, Interpolating, Folding, Time-Interleaved  
Pipeline A/Ds  
Oversampling Conversion  
Noise Shaping and Sigma Delta A/Ds  
Multi-Bit, Hybrid, Cascoded Architectures

### Week 12) D/A Conversion Techniques

Ideal D/A converter  
Binary Scaled D/As  
Decoder Based Converters  
Hybrid and Oversampling D/As

### Week 13) PLLs and Frequency Synthesizers

Digital PLLs versus Analog  
Phase/Frequency Detector, Charge Pumps and VCO circuits  
1st order and 2nd Order Loop Filters, Linear Modeling

### Week 14) Miscellaneous

Charge Pumps  
Receiver/Transmitter

Final Exam, Final Project Presentation