Dynamic Combinational Circuits

- Dynamic circuits
  - Charge sharing, charge redistribution
- Domino logic
- np-CMOS (zipper CMOS)
Dynamic Logic

- *Dynamic* gates use a clocked pMOS pullup
- Two modes: *precharge* and *evaluate*

![Diagram](image-url)

James Morizio
The Foot

- What if pulldown network is ON during precharge?
- Use series evaluation transistor to prevent fight.
Dynamic Logic

2 phase operation:
- Precharge
- Evaluation

Φn network

Φp network
Logical Effort

Inverter

unfooted

footed

NAND2

NOR2

$g_d = 1/3, p_d = 2/3$

$g_d = 2/3, p_d = 3/3$

$g_d = 2/3, p_d = 3/3$

$g_d = 3/3, p_d = 4/3$

$g_d = 3/3, p_d = 4/3$

$g_d = 1/3, p_d = 3/3$

$g_d = 1/3, p_d = 3/3$

$g_d = 2/3, p_d = 5/3$
Dynamic Logic

- N+2 transistors for N-input function
  - Better than 2N transistors for complementary static CMOS
  - Comparable to N+1 for ratio-ed logic
- No static power dissipation
  - Better than ratio-ed logic
- Careful design, clock signal $\Phi$ needed
Dynamic Logic: Principles

**Precharge**

\[ \Phi = 0, \text{Out is precharged to } V_{DD} \text{ by } M_p. \]
\[ M_e \text{ is turned off, no dc current flows} \]
(regardless of input values)

**Evaluation**

\[ \Phi = 1, M_e \text{ is turned on, } M_p \text{ is turned off.} \]
Output is pulled down to zero depending on the values on the inputs. If not, precharged value remains on \( C_L \).

**Important:** Once Out is discharged, it cannot be charged again!
Gate input can make only one transition during evaluation

- Minimum clock frequency must be maintained
- Can \( M_e \) be eliminated?
Example

- Ratioless
- No Static Power Consumption
- Noise Margins small (NM_L)
- Requires Clock
Dynamic 4 Input NAND Gate

V_{DD}

Out

In_1

In_2

In_3

In_4

\phi

GND

V_{DD}

\phi

Out

In_1

In_2

In_3

In_4

\phi
Cascading Dynamic Gates

Internal nodes can only make 0-1 transitions during evaluation period
Monotonicity

• Dynamic gates require *monotonically rising* inputs during evaluation
  – 0 -> 0
  – 0 -> 1
  – 1 -> 1
  – But not 1 -> 0
Monotonicity Woes

- But dynamic gates produce monotonically falling outputs during evaluation
- Illegal for one dynamic gate to drive another!
Reliability Problems — Charge Leakage

(a) Leakage sources

(1) Leakage through reverse-biased diode of the diffusion area
(2) Subthreshold current from drain to source

Minimum Clock Frequency: > 1 MHz
Leakage

• Dynamic node floats high during evaluation
  – Transistors are leaky ($I_{OFF} \neq 0$)
  – Dynamic value will leak away over time
  – Formerly milliseconds, now nanoseconds!

• Use keeper to hold dynamic node
  – Must be weak enough not to fight evaluation
Charge Sharing (redistribution)

- Assume: during precharge, A and B are 0, $C_a$ is discharged
- During evaluation, B remains 0 and A rises to 1
- Charge stored on $C_L$ is now redistributed over $C_L$ and $C_a$

\[ CL \cdot V_{DD} = CL \cdot V_{out(t)} + C_a \cdot V_X \]

\[ V_X = V_{DD} - V_t \text{, therefore} \]

\[ \delta V_{out(t)} = V_{out(t)} - V_{DD} = -\frac{C_a}{C_L} (V_{DD} - V_t) \]

Desirable to keep the voltage drop below threshold of pMOS transistor (why?) $\Rightarrow \frac{C_a}{C_L} < 0.2$
Charge Sharing

- Dynamic gates suffer from charge sharing

\[ V_x = V_Y = \frac{C_Y}{C_x + C_Y} V_{DD} \]
Charge Redistribution - Solutions

(a) Static bleeder

(b) Precharge of internal nodes
Secondary Precharge

• Solution: add secondary precharge transistors
  – Typically need to precharge every other node
• Big load capacitance $C_Y$ helps as well
Domino Logic

Static inverters between dynamic stages

Static Inverter with Level Restorer

$V_{DD}$

$M_p$

$M_e$

$In_1$

$In_2$

$In_3$

$Out1$

$Out2$

$V_{DD}$

$M_p$

$Mr$

$V_{DD}$

$In_4$
Domino Gates

- Follow dynamic stage with inverting static gate
  - Dynamic / static pair is called domino gate
  - Produces monotonic outputs
Domino Logic - Characteristics

• Only non-inverting logic
• Very fast - Only 1->0 transitions at input of inverter
  • Precharging makes pull-up very fast
• Adding level restorer reduces leakage and charge redistribution problems
• Optimize inverter for fan-out
Domino Optimizations

- Each domino gate triggers next one, like a string of dominos toppling over
- Gates evaluate sequentially but precharge in parallel
- Thus evaluation is more critical than precharge
- HI-skewed static stages can perform logic
Dual-Rail Domino

- Domino only performs noninverting functions:
  - AND, OR but not NAND, NOR, or XOR
- Dual-rail domino solves this problem
  - Takes true and complementary inputs
  - Produces true and complementary outputs

<table>
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<tr>
<th>sig_h</th>
<th>sig_l</th>
<th>Meaning</th>
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<td>0</td>
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</tr>
<tr>
<td>1</td>
<td>0</td>
<td>‘1’</td>
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<tr>
<td>1</td>
<td>1</td>
<td>invalid</td>
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Example: AND/NAND

- Given $A_h, A_l, B_h, B_l$
- Compute $Y_h = A \cdot B$, $Y_l = \sim(A \cdot B)$
- Pulldown networks are conduction complements
Example: XOR/XNOR

- Sometimes possible to share transistors

\[ Y_L = A \text{xnor} B \]

\[ Y_H = A \text{xor} B \]
Domino Summary

- Domino logic is attractive for high-speed circuits
  - 1.5 – 2x faster than static CMOS
  - But many challenges:
    - Monotonicity
    - Leakage
    - Charge sharing
    - Noise
- Widely used in high-performance microprocessors
np-CMOS (Zipper CMOS)

- Only 1-0 transitions allowed at inputs of PUN
- Used a lot in the Alpha design
np CMOS Adder

Carry Path
# CMOS Circuit Styles - Summary

<table>
<thead>
<tr>
<th>Style</th>
<th>Ratioed</th>
<th>Static Power</th>
<th># transistors</th>
<th>Area ($\mu$m$^2$)</th>
<th>Propagation Delay (nsec)</th>
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<tbody>
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*4-input NAND Gate*