Interconnects

- Wire Resistance
- Wire Capacitance
- Wire RC Delay
- Crosstalk
- Wire Engineering
- Repeaters
Introduction

• Chips are mostly made of wires called *interconnect*
  – In stick diagram, wires set size
  – Transistors are little things under the wires
  – Many layers of wires

• Wires are as important as transistors
  – Speed
  – Power
  – Noise

• Alternating layers run orthogonally
Wire Geometry

• Pitch = w + s
• Aspect ratio: AR = t/w
  – Old processes had AR << 1
  – Modern processes have AR ≈ 2
  • Pack in many skinny wires
Layer Stack

• AMI 0.6 μm process has 3 metal layers
• Modern processes use 6-10+ metal layers
• Example:
  Intel 180 nm process
  • M1: thin, narrow (< 3λ)
    – High density cells
  • M2-M4: thicker
    – For longer wires
  • M5-M6: thickest
    – For V_{DD}, GND, clk

<table>
<thead>
<tr>
<th>Layer</th>
<th>T (nm)</th>
<th>W (nm)</th>
<th>S (nm)</th>
<th>AR</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>1720</td>
<td>860</td>
<td>860</td>
<td>2.0</td>
</tr>
<tr>
<td>5</td>
<td>1600</td>
<td>800</td>
<td>800</td>
<td>2.0</td>
</tr>
<tr>
<td>4</td>
<td>1080</td>
<td>540</td>
<td>540</td>
<td>2.0</td>
</tr>
<tr>
<td>3</td>
<td>700</td>
<td>320</td>
<td>320</td>
<td>2.2</td>
</tr>
<tr>
<td>2</td>
<td>700</td>
<td>320</td>
<td>320</td>
<td>2.2</td>
</tr>
<tr>
<td>1</td>
<td>480</td>
<td>250</td>
<td>250</td>
<td>1.9</td>
</tr>
</tbody>
</table>

Substrate
Wire Resistance

\[ \rho = \text{resistivity} \ (\Omega \cdot \text{m}) \]

\[ R = \frac{\rho}{t \cdot w} = R_\square \frac{l}{w} \]

- \( R_\square \) = \textit{sheet resistance} \ (\Omega/\square)
  - \( \square \) is a dimensionless unit(!)
- Count number of squares
  - \( R = R_\square \ast \text{(\# of squares)} \)
Choice of Metals

- Until 180 nm generation, most wires were aluminum
- Modern processes often use copper
  - Cu atoms diffuse into silicon and damage FETs
  - Must be surrounded by a diffusion barrier

<table>
<thead>
<tr>
<th>Metal</th>
<th>Bulk resistivity (μΩ*cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silver (Ag)</td>
<td>1.6</td>
</tr>
<tr>
<td>Copper (Cu)</td>
<td>1.7</td>
</tr>
<tr>
<td>Gold (Au)</td>
<td>2.2</td>
</tr>
<tr>
<td>Aluminum (Al)</td>
<td>2.8</td>
</tr>
<tr>
<td>Tungsten (W)</td>
<td>5.3</td>
</tr>
<tr>
<td>Molybdenum (Mo)</td>
<td>5.3</td>
</tr>
</tbody>
</table>
### Sheet Resistance

- Typical sheet resistances in 180 nm process

<table>
<thead>
<tr>
<th>Layer</th>
<th>Sheet Resistance ($\Omega/\square$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffusion (silicided)</td>
<td>3-10</td>
</tr>
<tr>
<td>Diffusion (no silicide)</td>
<td>50-200</td>
</tr>
<tr>
<td>Polysilicon (silicided)</td>
<td>3-10</td>
</tr>
<tr>
<td>Polysilicon (no silicide)</td>
<td>50-400</td>
</tr>
<tr>
<td>Metal1</td>
<td>0.08</td>
</tr>
<tr>
<td>Metal2</td>
<td>0.05</td>
</tr>
<tr>
<td>Metal3</td>
<td>0.05</td>
</tr>
<tr>
<td>Metal4</td>
<td>0.03</td>
</tr>
<tr>
<td>Metal5</td>
<td>0.02</td>
</tr>
<tr>
<td>Metal6</td>
<td>0.02</td>
</tr>
</tbody>
</table>
Contacts Resistance

- Contacts and vias also have 2-20 Ω
- Use many contacts for lower R
  - Many small contacts for current crowding around periphery
Wire Capacitance

- Wire has capacitance per unit length
  - To neighbors
  - To layers above and below

- $C_{\text{total}} = C_{\text{top}} + C_{\text{bot}} + 2C_{\text{adj}}$
Capacitance Trends

- Parallel plate equation: \( C = \varepsilon A/d \)
  - Wires are not parallel plates, but obey trends
  - Increasing area \((W, t)\) increases capacitance
  - Increasing distance \((s, h)\) decreases capacitance

- Dielectric constant
  - \( \varepsilon = k\varepsilon_0 \)

- \( \varepsilon_0 = 8.85 \times 10^{-14} \text{ F/cm} \)
- \( k = 3.9 \) for \( \text{SiO}_2 \)
- Processes are starting to use low-k dielectrics
  - \( k \approx 3 \) (or less) as dielectrics use air pockets

- Typical (M2) wires have \( \sim 0.2 \text{ fF/\mu m} \)
  - Compare to \( 2 \text{ fF/\mu m} \) for gate capacitance
Diffusion & Polysilicon

• Diffusion capacitance is very high (about 2 fF/μm)
  – Comparable to gate capacitance
  – Diffusion also has high resistance
  – Avoid using diffusion *runners* for wires!

• Polysilicon has lower C but high R
  – Use for transistor gates
  – Occasionally for very short wires between gates
Lumped Element Models

- Wires are a distributed system
  - Approximate with lumped element models

\[ \frac{R}{N} - \frac{C}{N} - \frac{R}{N} \ldots - \frac{R}{N} - \frac{C}{N} \]

\[ \frac{R}{2} - \frac{C}{2} - \frac{R}{2} \]

\[ \frac{R}{2} - \frac{C}{2} \]

- 3-segment \( \pi \)-model is accurate to 3% in simulation
- L-model needs 100 segments for same accuracy!
- Use single segment \( \pi \)-model for Elmore delay
Example

- Metal2 wire in 180 nm process
  - 5 mm long
  - 0.32 μm wide
  - Number of squares = 5000/0.32 = 15625

- Construct a 3-segment π-model
  - $R_{\square} = 0.05 \, \Omega/\square$  \quad \Rightarrow R = 15625 \times 0.05 = 781 \, \Omega$
  - $C_{\text{permicron}} = 0.2 \, \text{fF}/\mu\text{m}$  \quad \Rightarrow C = 0.2 \, \text{fF}/\mu\text{m} \times 5000 \, \mu\text{m} = 1 \, \text{pF}$

\[
\begin{array}{c}
260 \, \Omega \\
\downarrow \\
167 \, \text{fF} \\
\downarrow \\
260 \, \Omega \\
\downarrow \\
167 \, \text{fF} \\
\downarrow \\
260 \, \Omega \\
\downarrow \\
167 \, \text{fF} \\
\downarrow \\
260 \, \Omega \\
\downarrow \\
167 \, \text{fF}
\end{array}
\]
Wire RC Delay

- Estimate the delay of a 10x inverter driving a 2x inverter at the end of the 5mm wire from the previous example.
  - \( R = 2.5 \, \text{k}\Omega \cdot \mu\text{m} \) for gates
  - Unit inverter: 0.36 \( \mu \text{m} \) nMOS, 0.72 \( \mu \text{m} \) pMOS
  - Unit inverter has 4\( \lambda = 0.36\mu\text{m} \) wide nMOS, 8\( \lambda = 0.72\mu\text{m} \) wide pMOS
  - Unit inverter: effective resistance of \( (2.5 \, \text{k}\Omega \cdot \mu\text{m})/(0.36\mu\text{m}) = 6.9 \, \text{k}\Omega \)
  - Capacitance: \( (0.36\mu\text{m} + 0.72 \, \mu\text{m}) \times (2fF/\mu\text{m}) = 2fF \)
  - \( t_{pd} = 1.1 \, \text{ns} \)

\[
\begin{align*}
\text{Driver} & \quad 690 \, \Omega \\
\text{Wire} & \quad 781 \, \Omega \\
\text{Load} & \quad 500 \, fF \\
& \quad 500 \, fF \\
& \quad 4 \, fF
\end{align*}
\]
Crosstalk

• A capacitor does not like to change its voltage instantaneously.

• A wire has high capacitance to its neighbor.
  – When the neighbor switches from 1->0 or 0->1, the wire tends to switch too.
  – Called capacitive coupling or crosstalk.

• Crosstalk effects
  – Noise on non-switching wires
  – Increased delay on switching wires
Crosstalk Delay

- Assume layers above and below on average are quiet
  - Second terminal of capacitor can be ignored
  - Model as $C_{\text{gnd}} = C_{\text{top}} + C_{\text{bot}}$
- Effective $C_{\text{adj}}$ depends on behavior of neighbors
  - *Miller effect*

<table>
<thead>
<tr>
<th>B</th>
<th>$\Delta V$</th>
<th>$C_{\text{eff(A)}}$</th>
<th>MCF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constant</td>
<td>$V_{\text{DD}}$</td>
<td>$C_{\text{gnd}} + C_{\text{adj}}$</td>
<td>1</td>
</tr>
<tr>
<td>Switching with A</td>
<td>0</td>
<td>$C_{\text{gnd}}$</td>
<td>0</td>
</tr>
<tr>
<td>Switching opposite A</td>
<td>$2V_{\text{DD}}$</td>
<td>$C_{\text{gnd}} + 2C_{\text{adj}}$</td>
<td>2</td>
</tr>
</tbody>
</table>
Crosstalk Noise

• Crosstalk causes noise on non-switching wires
• If victim is floating:
  – model as capacitive voltage divider

\[
\Delta V_{\text{victim}} = \frac{C_{\text{adj}}}{C_{\text{gnd-v}} + C_{\text{adj}}} \Delta V_{\text{aggressor}}
\]
Coupling Waveforms

- Simulated coupling for $C_{adj} = C_{victim}$
Noise Implications

• *So what* if we have noise?
• If the noise is less than the noise margin, nothing happens
• Static CMOS logic will eventually settle to correct output even if disturbed by large noise spikes
  – But glitches cause extra delay
  – Also cause extra power from false transitions
• Dynamic logic never recovers from glitches
• Memories and other sensitive circuits also can produce the wrong answer
Wire Engineering

• Goal: achieve delay, area, power goals with acceptable noise

• Degrees of freedom:
  – Width
  – Spacing
  – Layer
  – Shielding
Repeaters

- R and C are proportional to $l$
- RC delay is proportional to $l^2$
  - Unacceptably great for long wires
Repeaters

- R and C are proportional to $l$
- RC delay is proportional to $l^2$
  - Unacceptably great for long wires
- Break long wires into N shorter segments
  - Drive each one with an inverter or buffer
Repeater Design

• How many repeaters should we use?
• How large should each one be?
• Equivalent circuit
  – Wire length $l$
    • Wire Capacitance $C_w*l$, Resistance $R_w*l$
  – Inverter width $W$ (nMOS = $W$, pMOS = $2W$)
    • Gate Capacitance $C’*W$, Resistance $R/W$
    • ..........................
Repeater Results

• Write equation for Elmore Delay
  – Differentiate with respect to W and N
  – Set equal to 0, solve

\[ \frac{l}{N} = \sqrt{\frac{2RC'}{R_w C_w}} \]

\[ \frac{t_{pd}}{l} = \left(2 + \sqrt{2}\right) \sqrt{RC'R_w C_w} \quad \text{~60-80 ps/mm} \]

\[ W = \sqrt{\frac{RC_w}{R_w C'}} \]

in 180 nm process