Circuit Pitfalls

On how to avoid bad circuit design!
Outline

• Circuit Pitfalls
  – Detective puzzle
  – Given circuit and symptom, diagnose cause and recommend solution
  – All these pitfalls have caused failures in real chips
• Noise Budgets
• Reliability
Bad Circuit 1

- Circuit
  - 2:1 multiplexer

  \[\text{Principle:}\]

- Symptom
  - Mux works when selected D is 0 but not 1.
  - Or fails at low $V_{DD}$.

- Solution:
Bad Circuit 1

- Circuit
  - 2:1 multiplexer

- Symptom
  - Mux works when selected
    D is 0 but not 1.
  - Or fails at low $V_{DD}$.

Principle: Threshold drop
X never rises above $V_{DD} - V_t$
$V_t$ is raised by the body effect
The threshold drop is most serious as $V_t$ becomes a greater fraction of $V_{DD}$.

Solution:
Bad Circuit 1

• Circuit
  – 2:1 multiplexer

• Symptom
  – Mux works when selected
    D is 0 but not 1.
  – Or fails at low $V_{DD}$.
  – Or fails in SFSF corner.

Principle: Threshold drop
  X never rises above $V_{DD} - V_t$
  $V_t$ is raised by the body effect
  The threshold drop is most serious as $V_t$ becomes a
  greater fraction of $V_{DD}$.

Solution: Use transmission gates, not pass transistors
Bad Circuit 2

• Circuit
  – Latch

\[ \begin{align*}
D & \quad \phi \\
\quad & \quad \phi
\end{align*} \]

Principle:

Solution:

• Symptom
  – Load a 0 into Q
  – Set $\phi = 0$
  – Eventually Q spontaneously flips to 1
Bad Circuit 2

- **Circuit**
  - Latch

  ![Latch Diagram]

- **Symptom**
  - Load a 0 into Q
  - Set \( \phi = 0 \)
  - Eventually Q spontaneously flips to 1

**Principle: Leakage**

\( X \) is a dynamic node holding value as charge on the node
Eventually subthreshold leakage may disturb charge

**Solution:**
Bad Circuit 2

- Circuit
  - Latch

- Symptom
  - Load a 0 into Q
  - Set $\phi = 0$
  - Eventually Q spontaneously flips to 1

Principle: Leakage

$X$ is a dynamic node holding value as charge on the node
Eventually subthreshold leakage may disturb charge

Solution: Staticize node with feedback
Or periodically refresh node (requires fast clock, not practical for processes with big leakage)
Bad Circuit 3

• Circuit
  – Domino AND gate

\[ \begin{array}{c}
\phi \\
0 \\
1 \\
\end{array} \quad \begin{array}{c}
X \\
\rightarrow \\
Y
\end{array} \]

Principle:

Solution:

• Symptom
  – Precharge gate (Y=0)
  – Then evaluate
  – Eventually Y spontaneously flips to 1
Bad Circuit 3

• Circuit
  – Domino AND gate

Principle: Leakage
  X is a dynamic node holding value as charge on the node
  Eventually subthreshold leakage may disturb charge

• Symptom
  – Precharge gate (Y=0)
  – Then evaluate
  – Eventually Y spontaneously flips to 1

Solution:
Bad Circuit 3

- **Circuit**
  - Domino AND gate

- **Symptom**
  - Precharge gate ($Y=0$)
  - Then evaluate
  - Eventually $Y$ spontaneously flips to 1

Principle: Leakage

- $X$ is a dynamic node holding value as charge on the node
- Eventually subthreshold leakage may disturb charge

Solution: Keeper
Bad Circuit 4

- Circuit
  - Pseudo-nMOS OR

Principle:

Solution:

- Symptom
  - When only one input is true, $Y = 0$. 
Bad Circuit 4

• Circuit
  – Pseudo-nMOS OR

\[
\begin{array}{c}
\text{A} \\
\downarrow
\end{array} \quad \begin{array}{c}
\text{B} \\
\downarrow
\end{array} \quad \text{X} \quad \begin{array}{c}
\uparrow
\end{array} \quad \begin{array}{c}
\text{Y}
\end{array}
\]

• Symptom
  – When only one input is true, \( Y = 0 \).

Principle: Ratio Failure
nMOS and pMOS fight each other.
If the pMOS is too strong, nMOS cannot pull X low enough.
Solution:
Bad Circuit 4

- Circuit
  - Pseudo-nMOS OR

- Symptom
  - When only one input is true, $Y = 0$.

Principle: Ratio Failure

nMOS and pMOS fight each other.
If the pMOS is too strong, nMOS cannot pull X low enough.

Solution: Check that ratio is satisfied in all corners
Bad Circuit 5

- Circuit
  - Latch

Principle:

- Symptom
  - Q stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.

Solutions:
Bad Circuit 5

- Circuit
  - Latch

Principle: Ratio Failure (again)
  Series resistance of D driver, wire resistance, and $t_{\text{gate}}$ must be much less than weak feedback inverter.

Solutions:

- Symptom
  - Q stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.
Bad Circuit 5

- Circuit
  - Latch

- Symptom
  - $Q$ stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.

Principle: Ratio Failure (again)
Series resistance of $D$ driver, wire resistance, and $t_{gate}$ must be much less than weak feedback inverter.

Solutions: Check relative strengths
Avoid unbuffered diffusion inputs where driver is unknown
Bad Circuit 6

- Circuit
  - Domino AND gate

Principle:

Solutions:

- Symptom
  - Precharge gate while
    \( A = B = 0, \text{ so } Z = 0 \)
  - Set \( \phi = 1 \)
  - \( A \) rises
  - \( Z \) is observed to sometimes rise
Bad Circuit 6

- Circuit
  - Domino AND gate

  ![Circuit Diagram]

  Principle: Charge Sharing
  If X was low, it shares charge with Y

- Symptom
  - Precharge gate while
    A = B = 0, so Z = 0
  - Set \( \phi = 1 \)
  - A rises
  - Z is observed to sometimes rise

  ![Symptom Diagram]
Bad Circuit 6

• Circuit
  – Domino AND gate

Principle: Charge Sharing
  If X was low, it shares charge with Y
Solutions: Limit charge sharing

\[ V_x = V_y = \frac{C_y}{C_x + C_y} V_{DD} \]
Safe if \( C_Y \gg C_X \)
Or precharge node X too

• Symptom
  – Precharge gate while
    \( A = B = 0 \), so \( Z = 0 \)
  – Set \( \phi = 1 \)
  – A rises
  – \( Z \) is observed to sometimes rise
Bad Circuit 7

• Circuit
  – Dynamic gate + latch

• Symptom
  – Precharge gate while transmission gate latch is opaque
  – Evaluate
  – When latch becomes transparent, X falls

Principle:

Solution:
Bad Circuit 7

• Circuit
  – Dynamic gate + latch

![Circuit Diagram]

• Symptom
  – Precharge gate while transmission gate latch is opaque
  – Evaluate
  – When latch becomes transparent, X falls

Principle: Charge Sharing
  If Y was low, it shares charge with X

Solution:
Bad Circuit 7

- Circuit
  - Dynamic gate + latch

- Symptom
  - Precharge gate while transmission gate latch is opaque
  - Evaluate
  - When latch becomes transparent, X falls

Principle: Charge Sharing
If Y was low, it shares charge with X
Solution: Buffer dynamic nodes before driving transmission gate
Bad Circuit 8

• Circuit
  – Latch

Principle:

Solution:

• Symptom
  – Q changes while latch is opaque
  – Especially if D comes from a far-away driver
Bad Circuit 8

• Circuit
  - Latch

Principle: Diffusion Input Noise Sensitivity
  If $D < -V_t$, transmission gate turns on
  Most likely because of power supply noise or coupling on $D$

• Symptom
  - Q changes while latch is opaque
  - Especially if D comes from a far-away driver

Solution:
Bad Circuit 8

- Circuit
  - Latch

\[
\begin{array}{c}
D \\
\text{weak} \\
V_{DD}
\end{array}
\quad \begin{array}{c}
GND \\
V_{DD}
\end{array}
\quad Q
\]

- Symptom
  - Q changes while latch is opaque
  - Especially if D comes from a far-away driver

Principle: Diffusion Input Noise Sensitivity
  - If D < -V_t, transmission gate turns on
  - Most likely because of power supply noise or coupling on D

Solution: Buffer D locally

\[
\begin{array}{c}
D \\
\text{weak} \\
V_{DD}
\end{array}
\quad 0 \\
\begin{array}{c}
V_{DD} \\
\text{weak}
\end{array}
\quad Q
\]
Bad Circuit 9

- Circuit
  - Anything

- Symptom
  - Some gates are slower than expected

Principle:
Bad Circuit 9

- **Circuit**
  - Anything

- **Symptom**
  - Some gates are slower than expected

**Principle: Hot Spots and Power Supply Noise**
Noise

• Sources
  – Power supply noise / ground bounce
  – Capacitive coupling
  – Charge sharing
  – Leakage
  – Noise feedthrough

• Consequences
  – Increased delay (for noise to settle out)
  – Or incorrect computations
Reliability

- Hard Errors
- Soft Errors

<table>
<thead>
<tr>
<th>Time</th>
<th>Failure Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Infant Mortality</td>
<td></td>
</tr>
<tr>
<td>Useful Operating Life</td>
<td></td>
</tr>
<tr>
<td>Wear Out</td>
<td></td>
</tr>
</tbody>
</table>
Electromigration

- “Electron wind” causes movement of metal atoms along wires
- Excessive electromigration leads to open circuits
- Most significant for unidirectional (DC) current
  - Depends on current density $J_{dc}$ (current / area)
  - Exponential dependence on temperature
  - Black’s Equation:
    $$MTTF \propto \frac{e^{\frac{E_a}{kT}}}{J_{dc}^n}$$
  - Typical limits: $J_{dc} < 1 – 2$ mA / $\mu$m$^2$
Self-Heating

• Current through wire resistance generates heat
  – Oxide surrounding wires is a thermal insulator
  – Heat tends to build up in wires
  – Hotter wires are more resistive, slower

• Self-heating limits AC current densities for reliability
  \[ I_{\text{rms}} = \sqrt{\frac{\int_{0}^{T} I(t)^2 \, dt}{T}} \]
  – Typical limits: \( J_{\text{rms}} < 15 \text{ mA/μm}^2 \)
Hot Carriers

• Electric fields across channel impart high energies to some carriers
  – These “hot” carriers may be blasted into the gate oxide where they become trapped
  – Accumulation of charge in oxide causes shift in $V_t$ over time
  – Eventually $V_t$ shifts too far for devices to operate correctly

• Choose $V_{DD}$ to achieve reasonable product lifetime
  – Worst problems for inverters and NORs with slow input rise time and long propagation delays
Latchup

- Latchup: positive feedback leading to $V_{DD} - GND$ short
  - Major problem for 1970’s CMOS processes before it was well understood

- Avoid by minimizing resistance of body to GND / $V_{DD}$
  - Use plenty of substrate and well taps
Guard Rings

- Latchup risk greatest when diffusion-to-substrate diodes could become forward-biased
- Surround sensitive region with guard ring to collect injected charge
Overvoltage

• High voltages can damage transistors
  – Electrostatic discharge
  – Oxide arcing
  – Punchthrough
  – Time-dependent dielectric breakdown (TDDB)
    • Accumulated wear from tunneling currents
• Requires low $V_{DD}$ for thin oxides and short channels
• Use ESD protection structures where chip meets real world
Summary

• Static CMOS gates are very robust
  – Will settle to correct value if you wait long enough
• Other circuits suffer from a variety of pitfalls
  – Tradeoff between performance & robustness
• Very important to check circuits for pitfalls
  – For large chips, you need an automatic checker.
  – Design rules aren’t worth the paper they are printed on unless you back them up with a tool.
Soft Errors

• In 1970’s, DRAMs were observed to occasionally flip bits for no apparent reason
  – Ultimately linked to alpha particles and cosmic rays
• Collisions with particles create electron-hole pairs in substrate
  – These carriers are collected on dynamic nodes, disturbing the voltage
• Minimize soft errors by having plenty of charge on dynamic nodes
• Tolerate errors through ECC, redundancy
• Soft errors are now a problem for logic too!