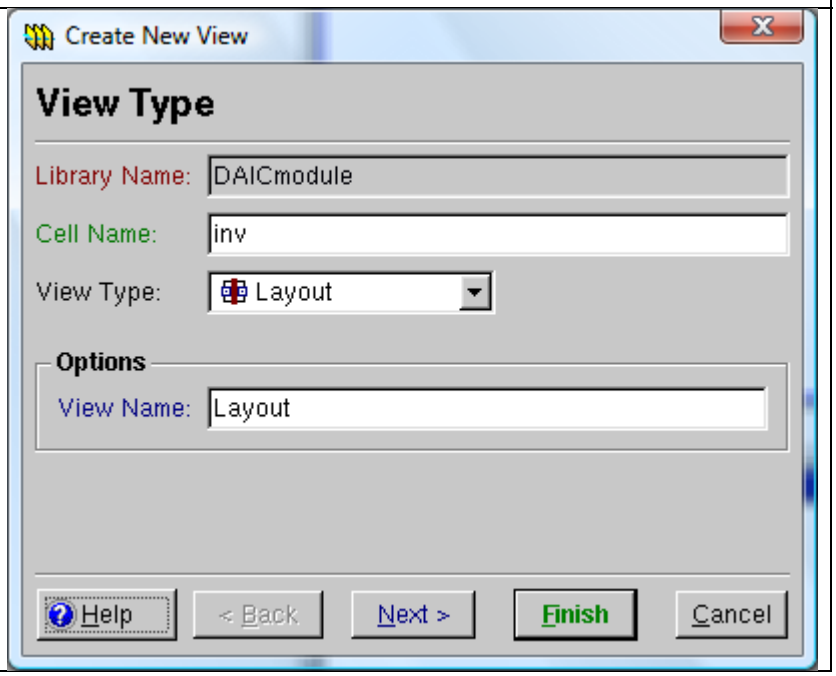
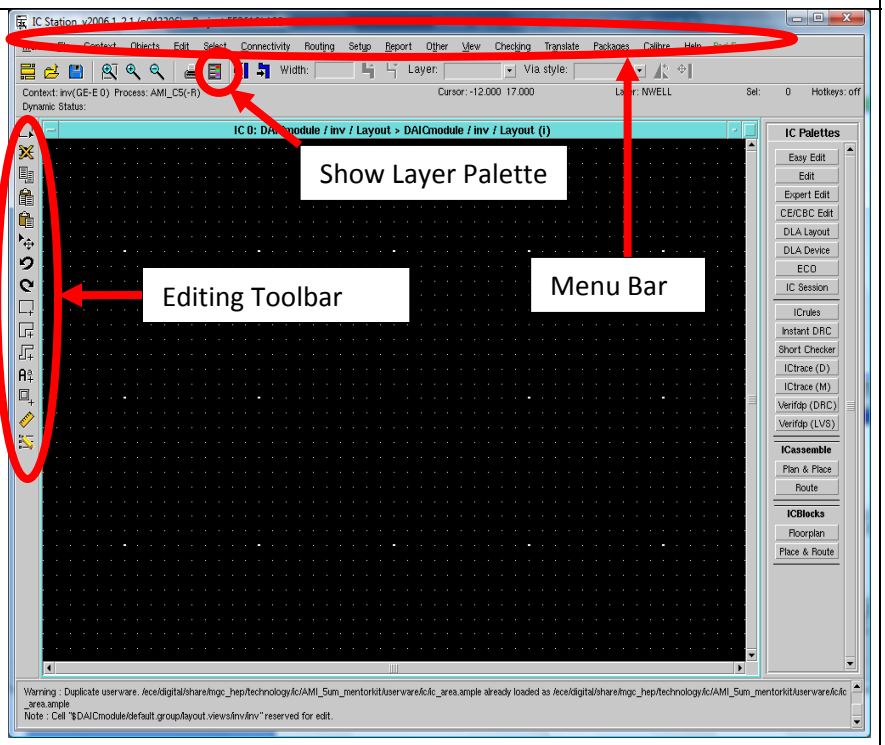
Inverter Layout example with ICstation

This exercise will show you how to draw the layout for an inverter.

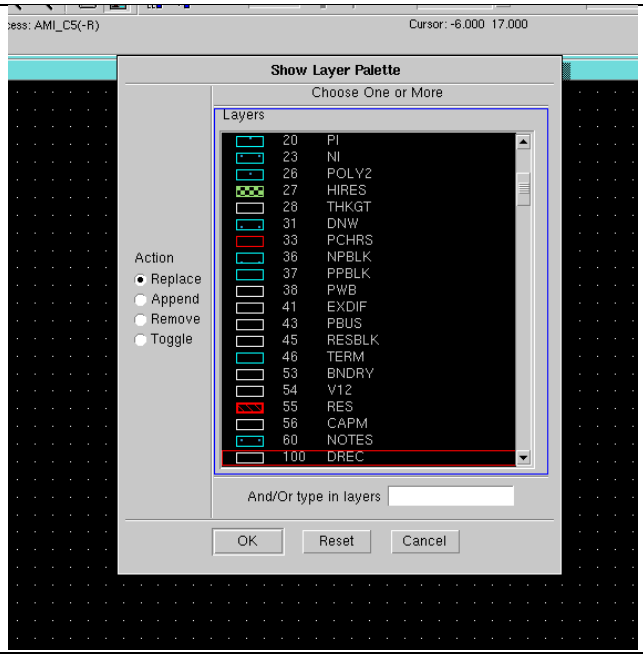
Step 1:

Description	Screenshot
1. Start ICstudio 2. Select the DAICmodule library 3. Right click on the view-pane and select “New View” 4. Enter the following: Cell Name – inv View Type – Layout View Name – Layout 5. Click “Finish”	

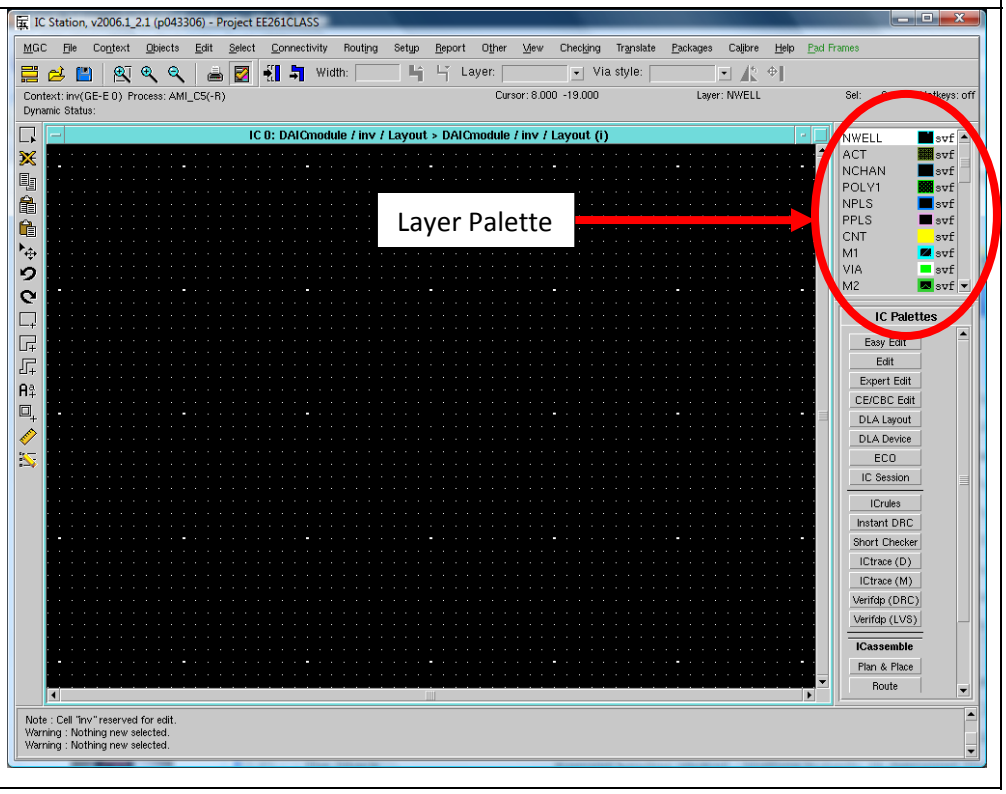
Step 2:

Description	Screenshot
1. An ICStation window will be opened. 2. You will see the Editing Toolbar on the left and the menu bar above. I will refer to these spots in the rest of the example. 3. Click the “Show Layer Palette” button.	

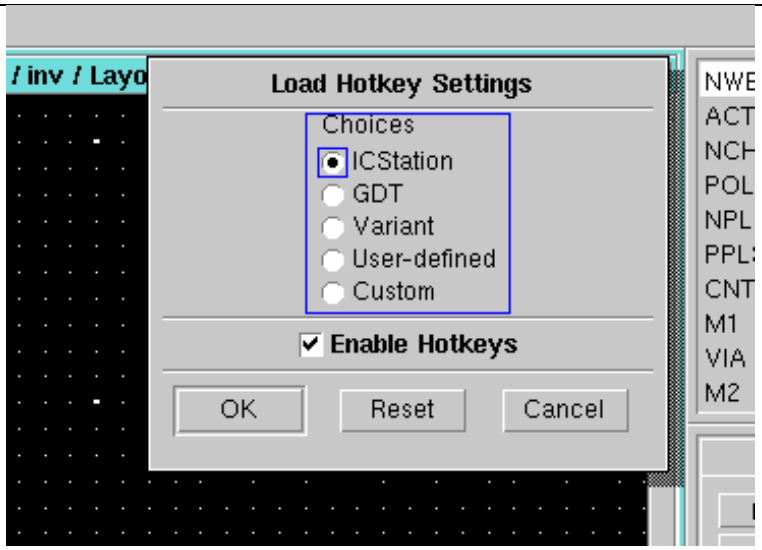
Step 3:

Description	Screenshot
1. Click on Layer 1 2. Hold down "shift" while scrolling down to layer 100 and click on that layer. 3. Click OK	

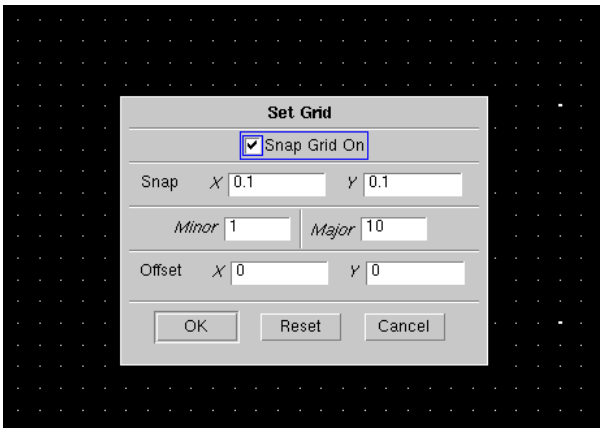
Step 4:

Description	Screenshot
1. You should now see the layer palette to the right. 2. Go to Other→ Hotkeys→ Load in the Menu Bar to set up the hotkeys.	

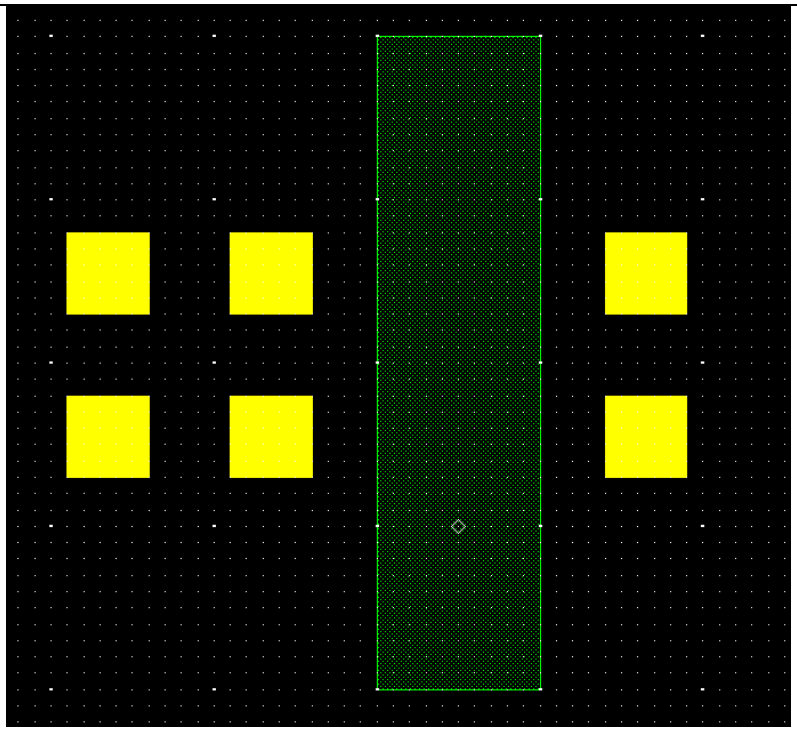
Step 5:

Description	Screenshot
1. Select ICStation and "Enable Hotkeys" in the next Window. 2. Click OK **3. Check the appendix at the end of this document for a list of important hotkeys.**	

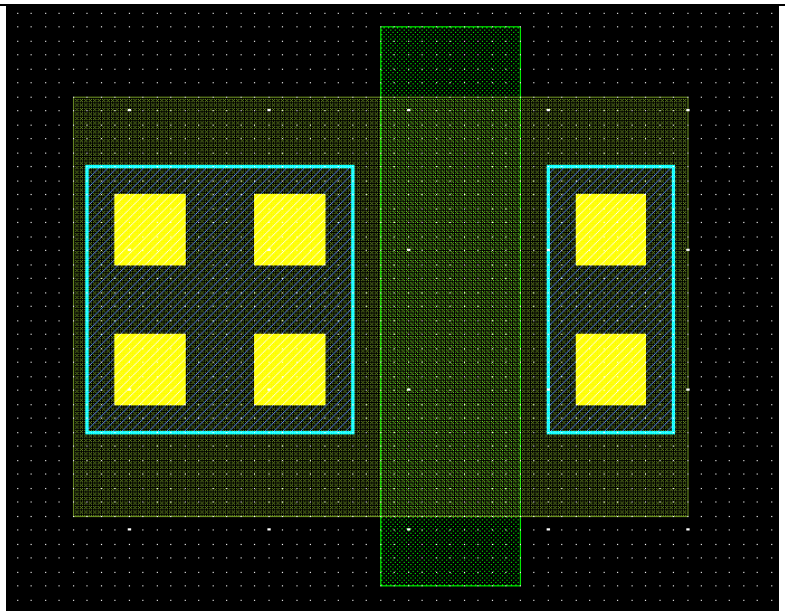
Step 6:

Description	Screenshot
1. Press Enter and type set grid in the command window. 2. On the next screen, select "Snap Grid On" and enter 0.1 for the X and Y snap values. 3. Now, the larger white dots on the screen will be 1 micron apart and the small white dots on the screen will each be 0.1 microns apart.	 

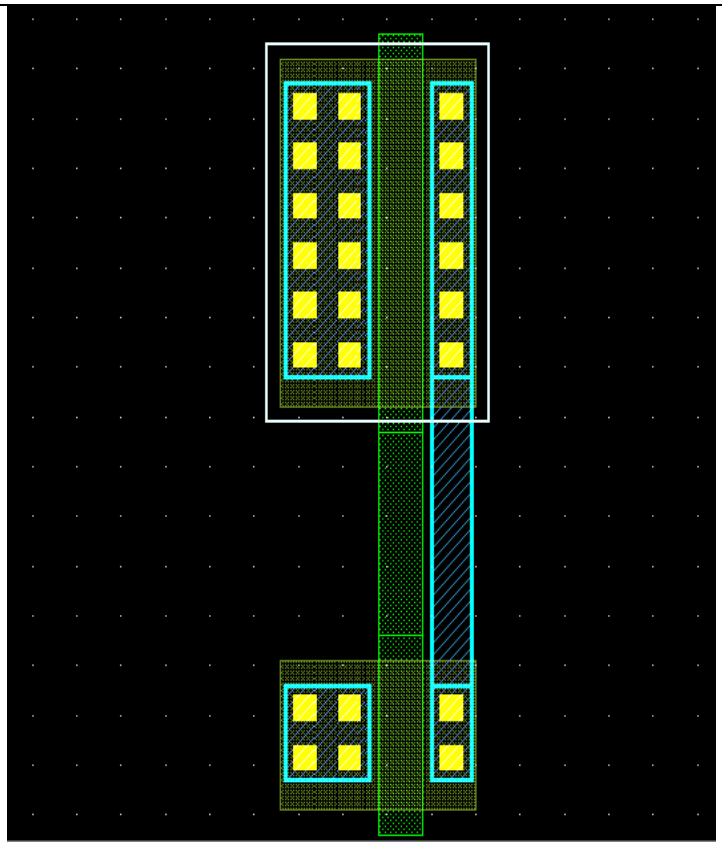
Step 7: Note (Use the hotkey “E” to select and extend edges if you need to edit the spacing in your layout. Use “M” to move selected objects and “C” to copy selected objects.)

Description	Screenshot
1. Draw a poly1 rectangle by clicking poly1 on the right and clicking the rectangle icon in the editing toolbar. 2. Click somewhere to start drawing the path and double click to complete the drawing. Make sure it is at least 1 micron x 4 microns. 3. Place 2 0.5 micron x 0.5 micron contacts (Layer CNT) on one side and 4 on the other side. Separate the Contacts by 0.5 microns and separate the contacts from the poly layer by 0.4 microns.	

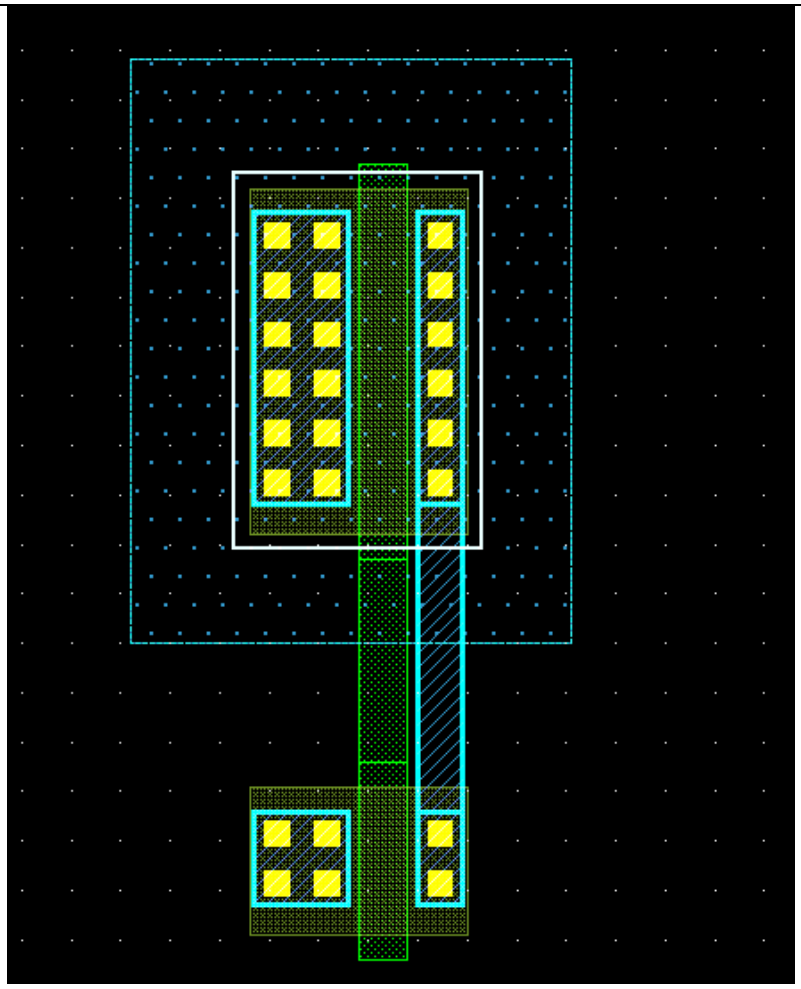
Step 8:

Description	Screenshot
1. Add an active layer (ACT) around the contacts so the poly shape extends 0.5 microns past it on top and bottom and the contacts are 0.3 microns away from the sides (ACT layer represents diffusion areas). 2. Draw a layer of metal1 (M1) that extends 0.2 microns around each side of the Contacts. 3. Run a DRC check to make sure the device is acceptable.	

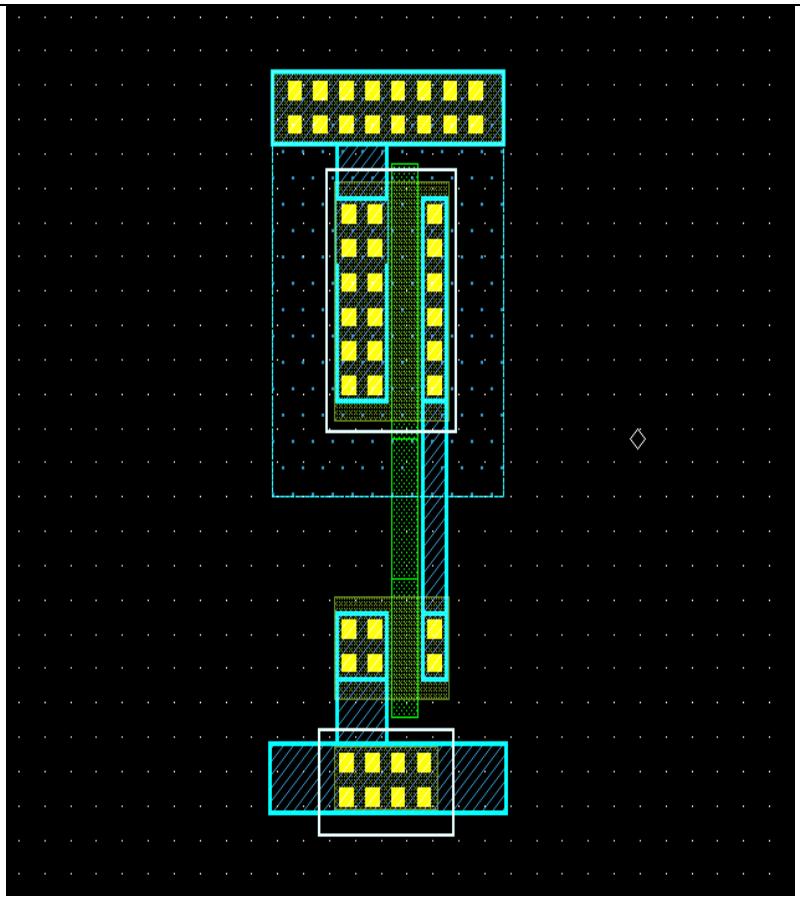
Step 9:

Description	Screenshot
1. Press enter and type “sel all” to select the entire transistor. Press “c” to copy it and move the new transistor up so that the ACT layers are at least 4 microns from each other. 2. Use the “E” hotkey to stretch the transistor so that the ACT layer is 7 microns wide (The width of the ACT region controls the width of the transistor). **Remember that the Poly extension must remain the same.** 3. Make sure you have 12 contacts on the left and 6 on the right. 4. Connect the poly rectangles in the middle and the metal rectangles on the right side. 4. Draw an N-plus (NPLS) and p-plus (PPLS) layer that overlap each other and extend 0.3 microns around each side of the ACT layer on the upper transistor. 5. Run a DRC check	

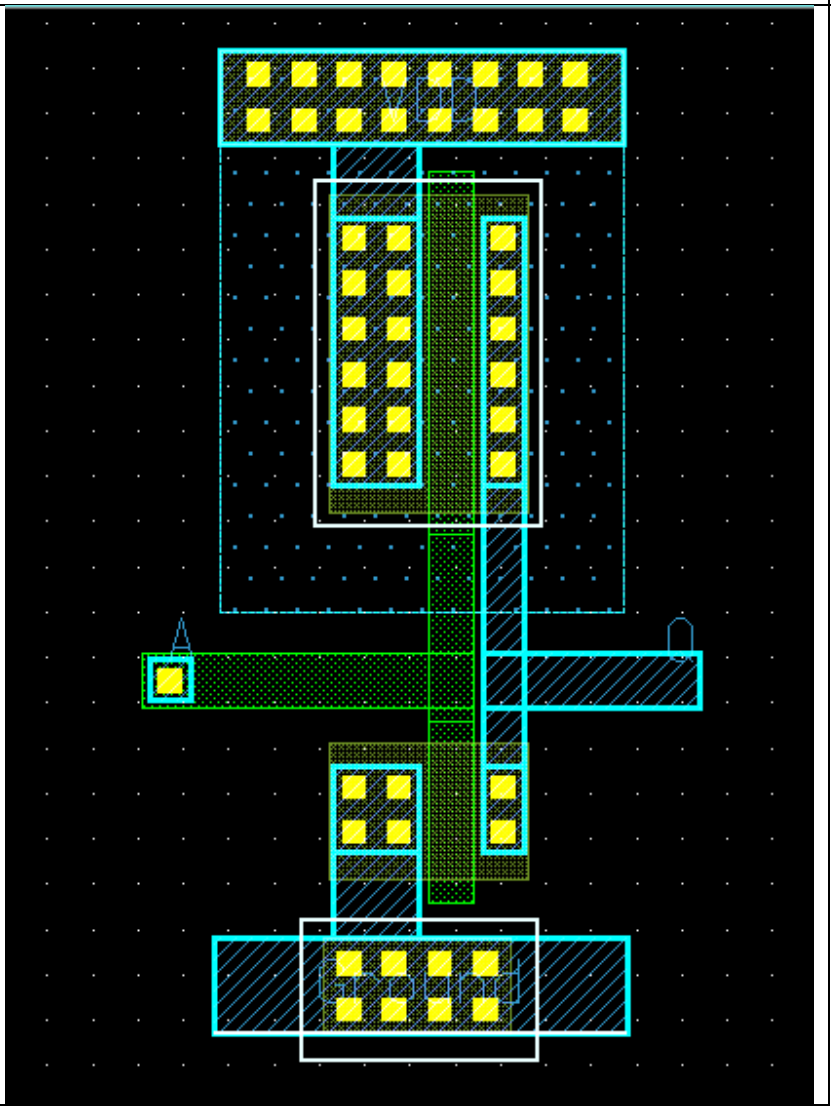
Step 10:

Description	Screenshot
1. Add an NWELL layer that surrounds the top transistor by 1.5 microns minimum on each side. 2. Add an NCHAN layer that overlaps the NWELL layer. 3. You now have a P-channel transistor on top and an N-channel transistor on bottom. 4. The metal connecting the 2 is the inverter output and the poly connecting the 2 is the input.	

Step 11:

Description	Screenshot
1. Make a well contact for the nwell around the p-device by adding a layer of ACT in the NWELL outside the NPLS and PPLS layers. Add 16 contacts and an overlapping metal 1 layer. Connect this area to the left side of the p-transistor with more metal1. 2. Make a substrate contact for the p-substrate by adding an ACT layer, 8 contacts and a strip of metal below the n-transistor. Surround the ACT layer with a PPLS and NPLS layer like you did for the p-transistor. 3. The substrate contact is where the inverter connects to ground and the well contact is where the inverter connects to VDD.	

Step 12:

Description	Screenshot
1. Add a strip of poly at the input and a strip of metal at the output. Add a contact to the input using the 'v' key. (Select the poly1/m1 contact) 2. Add text to all the ports using the 't' key. Make sure you set the layer on the right side of the screen to M1 (Text has layer properties just like any other shape.) 3. Label the VDD and Ground ports as shown. Label the input A and the output Q. Make sure all text is touching what it is labeling (Otherwise this will give an LVS error). 4. Run a DRC check. 5. Exit ICstation and set the connectivity source for the Layout to the schematic in ICstudio 6. Run an LVS check to finalize your inverter layout design.	

Appendix B – Important Icstudio commands (Type enter to see the command window)

1. “sel all”: Selects the entire layout
2. “peek 5”: Makes every layout layer visible
3. “cha lay xxx”: Changes the layer of the selected object to xxx
4. “set grid”: Brings up the set-grid window
5. “slice”: Slice the selected object with a line
6. “set basepoint”: Changes the basepoint of the selected object.