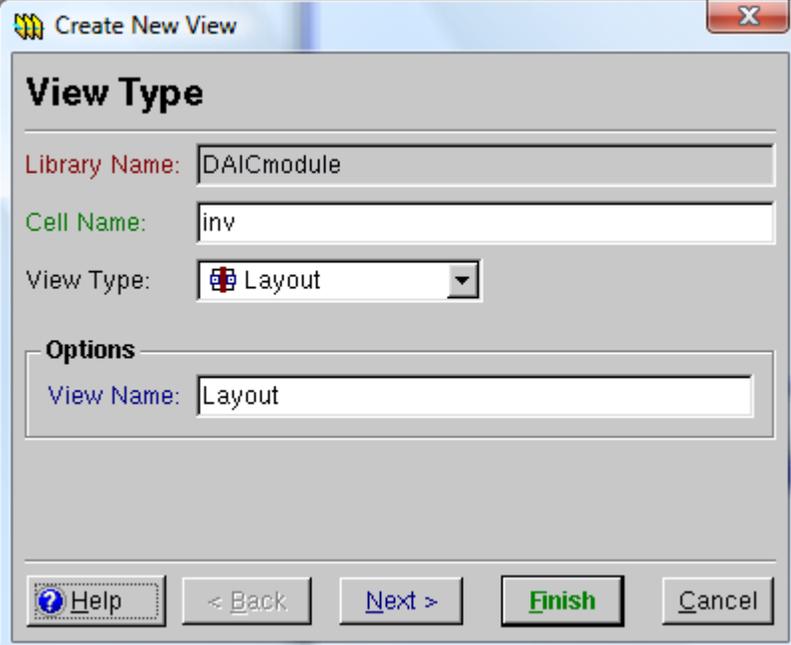


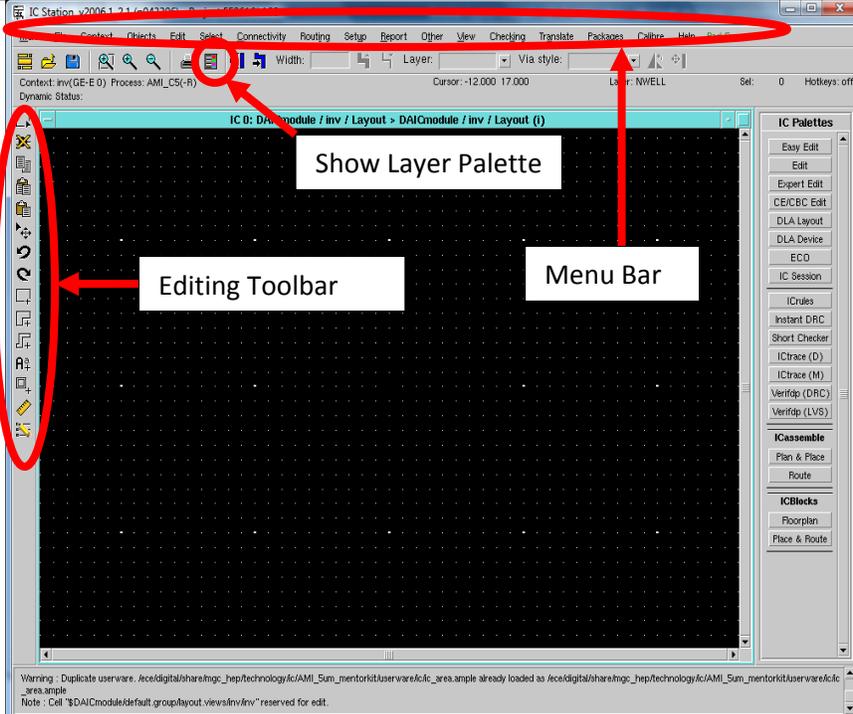
Inverter Layout example with ICstation

This exercise will show you how to draw the layout for an inverter.

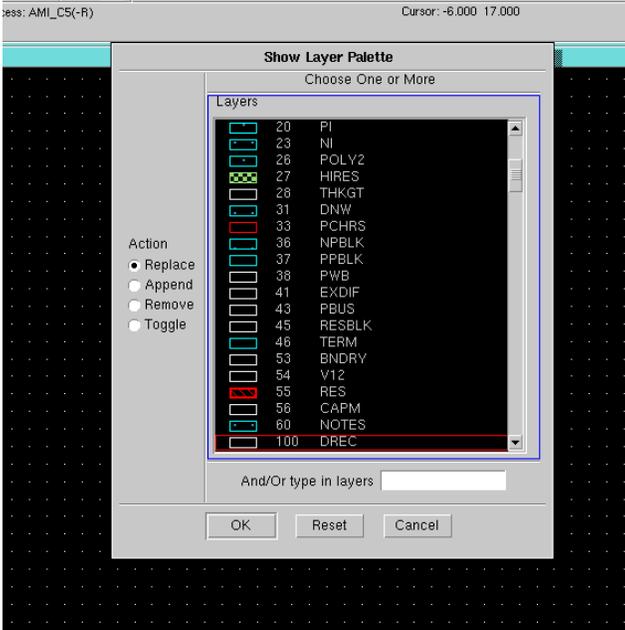
Step 1:

Description	Screenshot
<ol style="list-style-type: none">1. Start ICstudio2. Select the DAICmodule library3. Right click on the view-pane and select “New View”4. Enter the following: Cell Name – inv View Type – Layout View Name – Layout5. Click “Finish”	 <p>The screenshot shows a 'Create New View' dialog box. The 'View Type' section contains the following fields: Library Name: DAICmodule Cell Name: inv View Type: Layout (selected in a dropdown menu) Options section: View Name: Layout At the bottom, there are five buttons: Help, < Back, Next >, Finish (highlighted in green), and Cancel.</p>

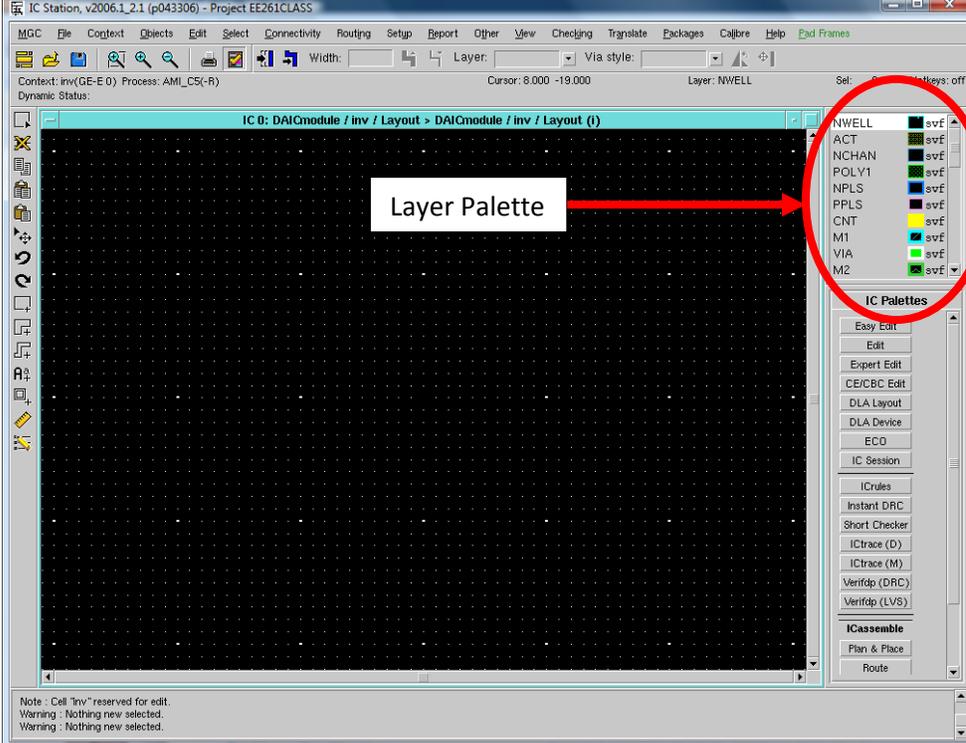
Step 2:

Description	Screenshot
<ol style="list-style-type: none">1. An ICStation window will be opened.2. You will see the Editing Toolbar on the left and the menu bar above. I will refer to these spots in the rest of the example.3. Click the "Show Layer Palette" button.	 <p>The screenshot shows the ICStation software interface. A red oval highlights the menu bar at the top, which includes options like File, Edit, Select, Connectivity, Routing, Setup, Report, Other, View, Checking, Translate, Packages, Calibra, and Help. Another red oval highlights the editing toolbar on the left side, which contains various icons for editing and design. A red arrow points from the text 'Show Layer Palette' to a button in the menu bar. Another red arrow points from the text 'Editing Toolbar' to the toolbar. A third red arrow points from the text 'Menu Bar' to the menu bar. The main workspace is a dark grid. On the right side, there is an 'IC Palettes' panel with various options like Easy Edit, Edit, Expert Edit, CE/CBC Edit, DLA Layout, DLA Device, ECO, IC Session, ICrules, Instant DRC, Short Checker, ITrace (D), ITrace (M), Verifap (DRC), and Verifap (LVIS). Below the workspace, there is a warning and note about duplicate userware and reserved cells.</p>

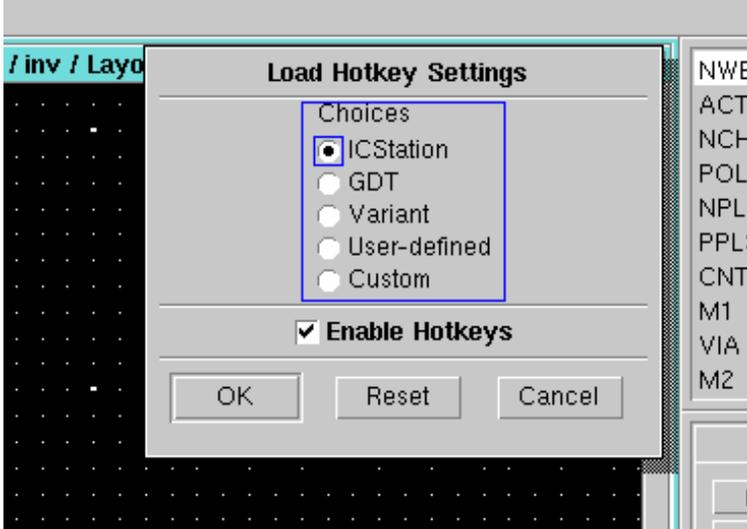
Step 3:

Description	Screenshot
<ol style="list-style-type: none">1. Click on Layer 12. Hold down "shift" while scrolling down to layer 100 and click on that layer.3. Click OK	

Step 4:

Description	Screenshot
<ol style="list-style-type: none">1. You should now see the layer palette to the right.2. Go to Other → Hotkeys → Load in the Menu Bar to set up the hotkeys.	

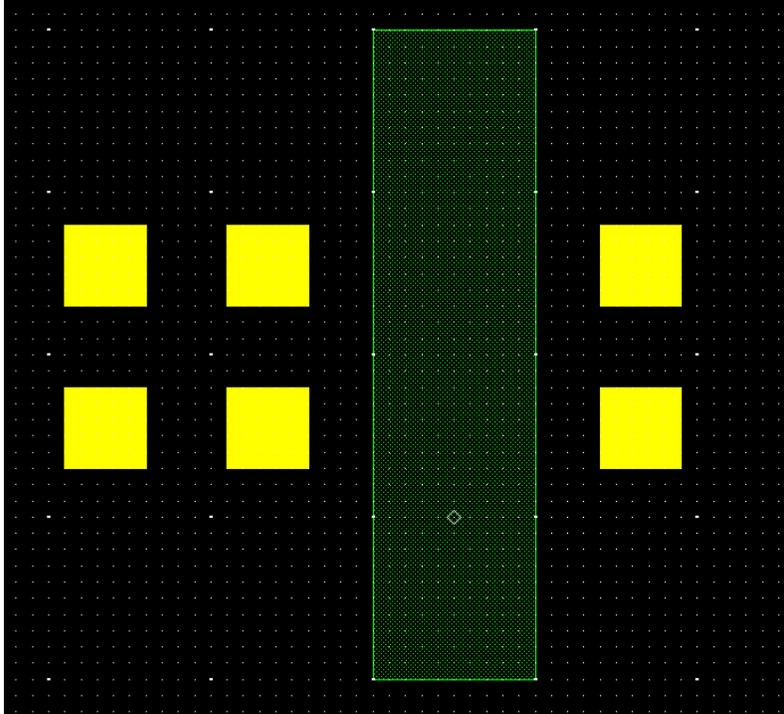
Step 5:

Description	Screenshot
<ol style="list-style-type: none">1. Select ICStation and "Enable Hotkeys" in the next Window.2. Click OK3. Check the appendix at the end of this document for a list of important hotkeys.	

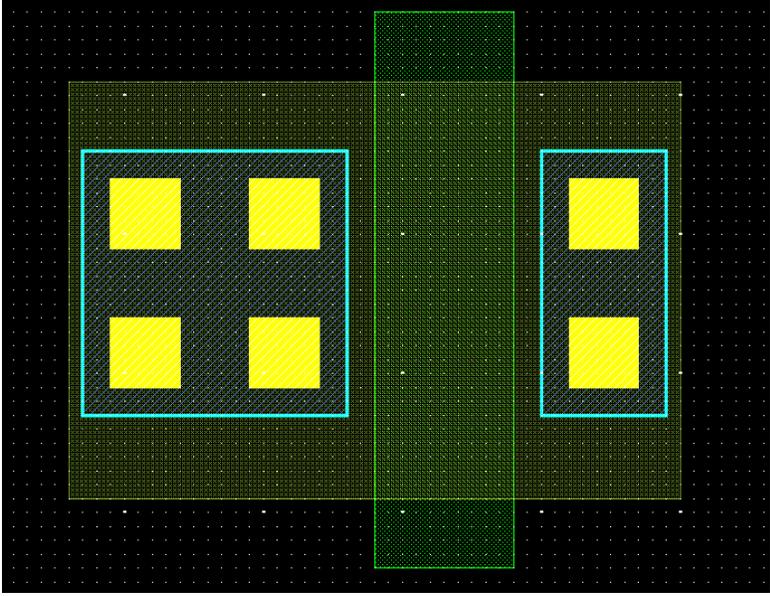
Step 6:

Description	Screenshot
<ol style="list-style-type: none">1. Press Enter and type set grid in the command window.2. On the next screen, select "Snap Grid On" and enter 0.1 for the X and Y snap values.3. Now, the larger white dots on the screen will be 1 micron apart and the small white dots on the screen will each be 0.1 microns apart.	

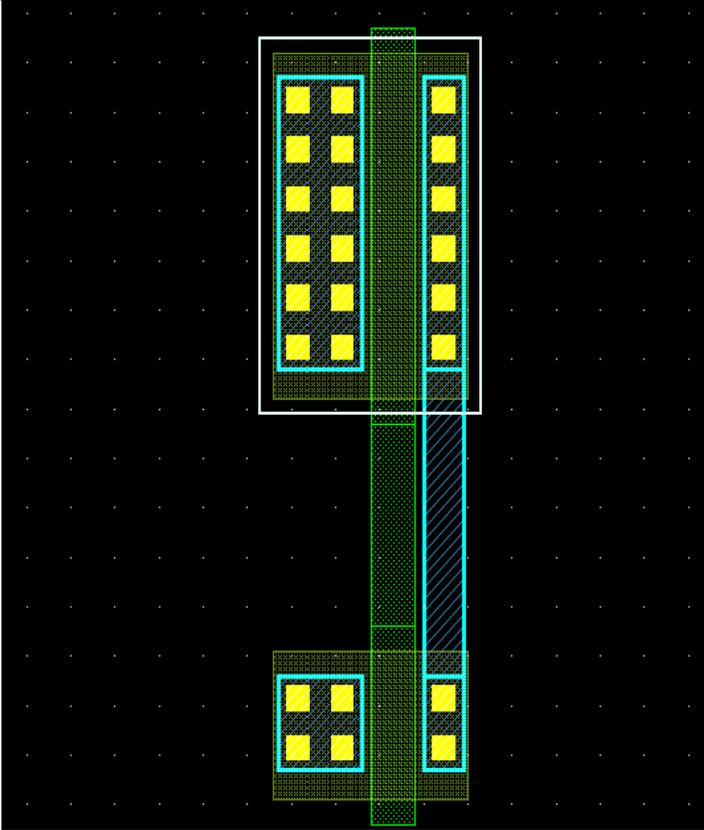
Step 7: Note (Use the hotkey “E” to select and extend edges if you need to edit the spacing in your layout. Use “M” to move selected objects and “C” to copy selected objects.)

Description	Screenshot
<ol style="list-style-type: none">1. Draw a poly1 rectangle by clicking poly1 on the right and clicking the rectangle icon in the editing toolbar.2. Click somewhere to start drawing the path and double click to complete the drawing. Make sure it is at least 1 micron x 4 microns.3. Place 2 0.5 micron x 0.5 micron contacts (Layer CNT) on one side and 4 on the other side. Separate the Contacts by 0.5 microns and separate the contacts from the poly layer by 0.4 microns.	 A screenshot of a layout editor interface. The background is black with a white grid. A large green rectangle is positioned vertically in the center-right. To its left, there are six yellow squares arranged in two rows of three. A small white diamond cursor is visible near the bottom center of the green rectangle.

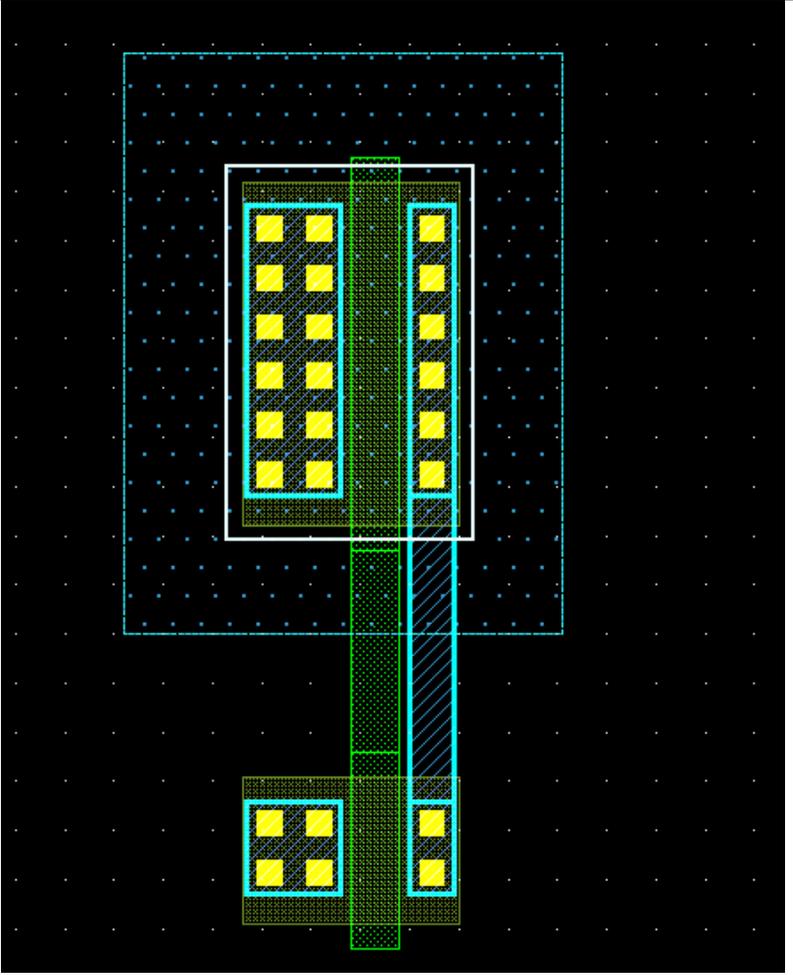
Step 8:

Description	Screenshot
<ol style="list-style-type: none"><li data-bbox="237 298 578 646">1. Add an active layer (ACT) around the contacts so the poly shape extends 0.5 microns past it on top and bottom and the contacts are 0.3 microns away from the sides (ACT layer represents diffusion areas).<li data-bbox="237 655 558 785">2. Draw a layer of metal1 (M1) that extends 0.2 microns around each side of the Contacts.<li data-bbox="237 793 565 894">3. Run a DRC check to make sure the device is acceptable.	 <p>The screenshot displays a PCB layout on a black background with a fine grid. On the left, there is a 2x2 grid of four yellow squares, each representing a contact. On the right, there is a vertical column of two yellow squares. A green rectangular area highlights a metal1 layer that extends around the contacts. The green area covers the four yellow squares on the left and the two on the right, with a slight overlap between the two groups. The green area is wider than the yellow squares, indicating the metal1 extension.</p>

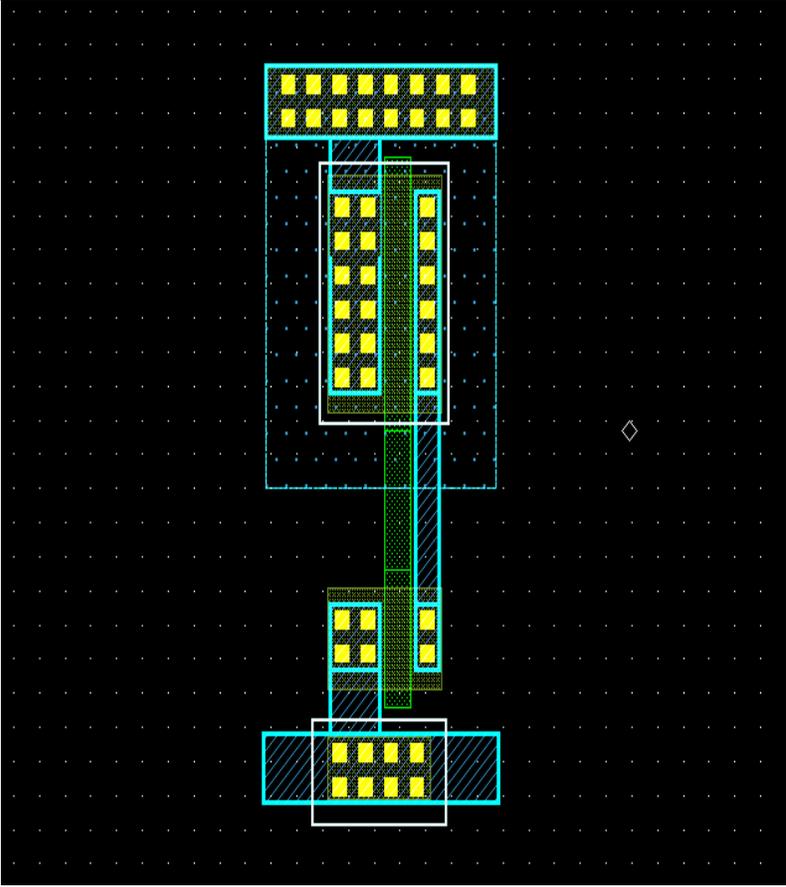
Step 9:

Description	Screenshot
<ol style="list-style-type: none">1. Press enter and type "sel all" to select the entire transistor. Press "c" to copy it and move the new transistor up so that the ACT layers are at least 4 microns from each other.2. Use the "E" hotkey to stretch the transistor so that the ACT layer is 7 microns wide (The width of the ACT region controls the width of the transistor). Remember that the Poly extension must remain the same.3. Make sure you have 12 contacts on the left and 6 on the right.4. Connect the poly rectangles in the middle and the metal rectangles on the right side.4. Draw an N-plus (NPLS) and p-plus (PPLS) layer that overlap each other and extend 0.3 microns around each side of the ACT layer on the upper transistor.5. Run a DRC check	 <p>The screenshot displays a PCB layout on a black background with a white grid. A central vertical structure is highlighted with a cyan border. This structure consists of a central green ACT layer, a blue poly layer, and a hatched metal layer. On the left side, there are 12 yellow square contacts arranged in two vertical columns of six. On the right side, there are 6 yellow square contacts arranged in a single vertical column of six. The structure is connected to a horizontal base at the bottom, which also features yellow contacts. The overall layout is symmetrical and precise.</p>

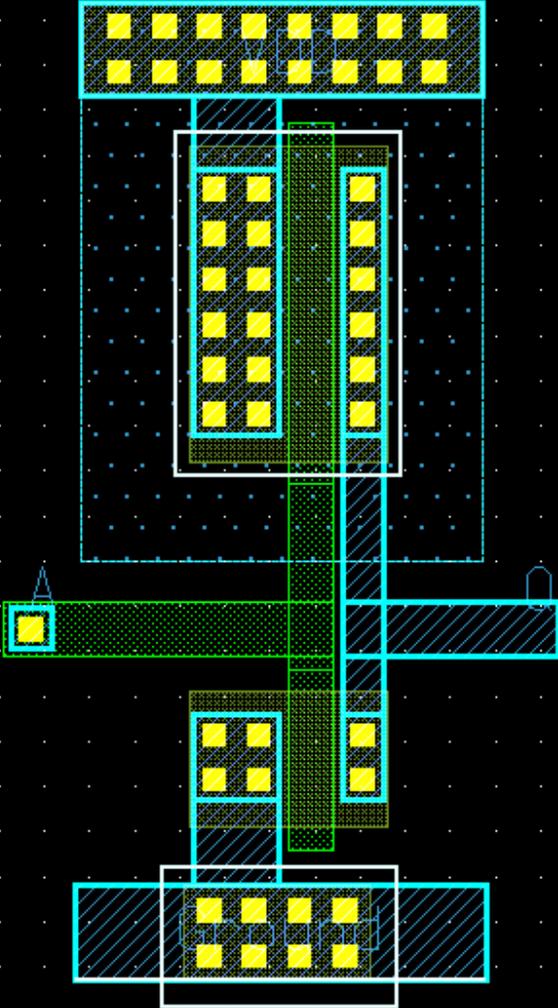
Step 10:

Description	Screenshot
<ol style="list-style-type: none"><li data-bbox="237 298 584 428">1. Add an NWELL layer that surrounds the top transistor by 1.5 microns minimum on each side.<li data-bbox="237 436 584 533">2. Add an NCHAN layer that overlaps the NWELL layer.<li data-bbox="237 541 584 672">3. You now have a P-channel transistor on top and an N-channel transistor on bottom.<li data-bbox="237 680 584 810">4. The metal connecting the 2 is the inverter output and the poly connecting the 2 is the input.	 <p>The screenshot displays a circuit layout on a black background with a grid of small blue dots. A large cyan rectangle outlines the main area. Inside, a white rectangle highlights a central structure. This structure consists of a top P-channel transistor (represented by a grid of yellow squares) and a bottom N-channel transistor (represented by a grid of yellow squares). A vertical green line represents the poly gate, connecting the two transistors. A vertical blue line represents the metal connection, which is the inverter output. A vertical red line represents the poly connection, which is the input. The layout is surrounded by a cyan border, indicating the NWELL layer.</p>

Step 11:

Description	Screenshot
<ol style="list-style-type: none"><li data-bbox="237 296 605 642">1. Make a well contact for the nwell around the p-device by adding a layer of ACT in the NWELL outside the NPLS and PPLS layers. Add 16 contacts and an overlapping metal 1 layer. Connect this area to the left side of the p-transistor with more metal1.<li data-bbox="237 648 605 961">2. Make a substrate contact for the p-substrate by adding an ACT layer, 8 contacts and a strip of metal below the n-transistor. Surround the ACT layer with a PPLS and NPLS layer like you did for the p-transistor.<li data-bbox="237 968 605 1171">3. The substrate contact is where the inverter connects to ground and the well contact is where the inverter connects to VDD.	 <p>The screenshot displays a layout editor interface with a black background and a light blue grid. A central vertical structure represents an inverter. At the top, a horizontal bar contains 16 yellow squares arranged in two rows of eight, representing a well contact. Below this, a vertical green strip represents the n-well. At the bottom, another horizontal bar contains 8 yellow squares in a single row, representing a substrate contact. The layout is surrounded by various colored regions (blue, green, yellow) representing different semiconductor layers and metal connections.</p>

Step 12:

Description	Screenshot
<ol style="list-style-type: none">1. Add a strip of poly at the input and a strip of metal at the output. Add a contact to the input using the 'v' key. (Select the poly1/m1 contact)2. Add text to all the ports using the 't' key. Make sure you set the layer on the right side of the screen to M1 (Text has layer properties just like any other shape.)3. Label the VDD and Ground ports as shown. Label the input A and the output Q. Make sure all text is touching what it is labeling (Otherwise this will give an LVS error).4. Run a DRC check.5. Exit ICStation and set the connectivity source for the Layout to the schematic in ICStudio6. Run an LVS check to finalize your inverter layout design.	

Appendix B – Important Icstudio commands (Type enter to see the command window)

1. “sel all”: Selects the entire layout
2. “peek 5”: Makes every layout layer visible
3. “cha lay xxx”: Changes the layer of the selected object to xxx
4. “set grid”: Brings up the set-grid window
5. “slice”: Slice the selected object with a line
6. “set basepoint”: Changes the basepoint of the selected object.