AMI 0.5μm Process Design Rules

Summary

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1 General Rules

- Minimum transistor width is 0.8μm
- NCHAN and NWELL layers should be identical and overlapping
- PPLS and NPLS layers should be identical and overlapping
- Minimum NWELL to PPLS spacing is 1.5μm
- Minimum diffusion width is 0.5μm
- Minimum diffusion spacing is 0.9μm
- Contacts (CNT) should be used to connect NWELL and PWELL to METAL1 (M1) layer. Otherwise, floating NWELL or floating PWELL errors will be shown.

2 POLY Layer Rules

- Minimum POLY width is 0.6μm
- Minimum POLY spacing is 0.6μm
- Minimum ACTIVE (ACT) extension beyond POLY is 0.65μm
- Min POLY extension beyond ACT is 0.5μm
- Minimum POLY to ACT spacing is 0.2μm

3 Metal Layers Rules

- Minimum M1 width is 0.6μm
- Minimum M1 spacing is 0.6μm
- Minimum Wide-M1 to M1 spacing is 1.2μm
- Minimum M2 width is 0.7μm
• Minimum M2 spacing is 0.7μm
• Minimum Wide-M2 to M2 spacing is 1.2μm
• Minimum M3 width is 0.8μm
• Minimum M3 spacing is 0.7μm
• Minimum Wide-M3 to M3 spacing is 1.2μm

4 VIA Rules
• VIA should be 0.5μm by 0.5μm
• VIA should be covered by M1 and M2
• Minimum VIA spacing is 0.6μm
• Minimum M1 enclosure of VIA is 0.2μm
• Minimum M2 enclosure of VIA is 0.2μm

5 VIA2 Rules
• VIA2 should be 0.5μm by 0.5μm
• VIA2 should be covered by M2 and M3
• Minimum VIA2 spacing is 0.8μm
• Minimum M2 enclosure of VIA2 is 0.2μm
• Minimum M3 enclosure of VIA2 is 0.2μm

6 Contact (CNT) Rules
• CNT should be 0.5μm by 0.5μm
• Minimum CNT spacing is 0.5μm
• CNT should be covered by M1 (CNT without M1 will give the error: CTNOM1)
• Minimum ACT enclosure of CNT is 0.3μm
• Minimum CNT to any POLY spacing is 0.4μm
• Minimum POLY enclosure of CNT is 0.2μm
• Minimum POLY2 enclosure of CNT is 0.2μm
• Minimum POLY-CONTACTS to ACT spacing is 0.4μm
7 N+ Implant Rules

- Minimum PPLS to ACT spacing is 0.3\(\mu m\)
- Minimum PPLS enclosure of ACT is 0.3\(\mu m\)
- Minimum PPLS to NWELL spacing is 1.5\(\mu m\)
- Minimum PPLS width is 0.7\(\mu m\)
- Minimum PPLS spacing is 0.7\(\mu m\)
- Minimum N-Diffusion enclosure of Gate is 0.65\(\mu m\)
- Minimum P-Diffusion enclosure of Gate is 0.65\(\mu m\)