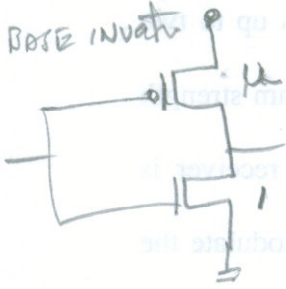


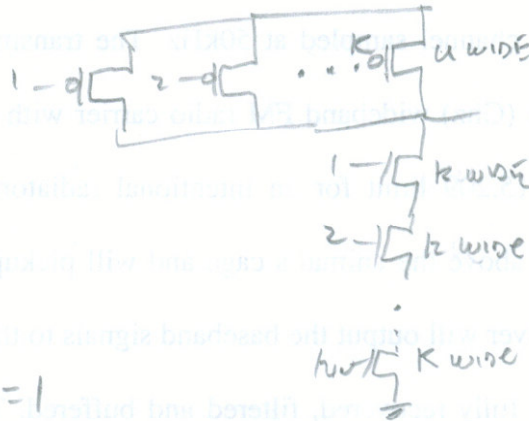
HW2

2b PROB 4.20



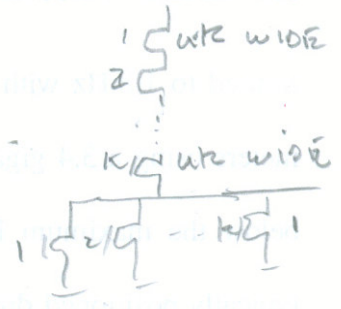
logical effort of inverter =  $\frac{u+1}{u+1} = 1$

2 INPUT NAND



logical effort =  $\frac{u+k}{u+1}$   
NAND

2 INPUT NOR



logical effort =  $\frac{u+k+1}{u+1}$   
NOR

AS  $u \uparrow$  logic effort of NAND  $\approx 1$   
 " " " NOR =  $k$  hence NAND is better

HW2

2c PROB 4.27

$V_{DD} = .9V$

$Freq = 450 MHz$

ACTIVITY FACTOR  $\alpha = .1$

switching cap =  $150PF/mm^2$

TOTAL CAPACITANCE =  $150PF/mm^2 \cdot .70 mm^2 = 10500 pF$

$P = \alpha C_{TOT} V_{DD}^2 (Freq) = .1 (10.5 \times 10^{-9}) (.9)^2 (450 \times 10^6)$

$P = 382.725 mWatts$