DESIGN OF 8-POINT FFT

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For DFT:

To illustrate the savings of a FFT, we use the butterfly figure as below:
Fig 2  Block Diagram of a 8-point FFT structure
Current Work

- FIFO Implementation
- 8-bit Ripple Carry Adder Implementation
- 8-bit Subtractor Implementation
- Partial work of Complex Multiplier
FIFO Implementation
schematic
FIFO Implementation
layout
FIFO Implementation simulation
8-bit Ripple Carry Adder Implementation

Half Adder schematic
8-bit Ripple Carry Adder Implementation
Half Adder layout
8-bit Ripple Carry Adder Implementation
Half Adder digital simulation

Work Accomplished
8-bit Ripple Carry Adder Implementation
Half Adder analog simulation
8-bit Ripple Carry Adder Implementation
Full Adder schematic
8-bit Ripple Carry Adder Implementation
Full Adder layout
8-bit Ripple Carry Adder Implementation

Full Adder digital simulation
8-bit Ripple Carry Adder Implementation

Half Adder analog simulation
8-bit Ripple Carry Adder Implementation

8-bit Adder schematic
8-bit Ripple Carry Adder Implementation
8-bit Adder schematic
8-bit Ripple Carry Adder Implementation
8-bit Adder layout
8-bit Ripple Carry Adder Implementation
8-bit Adder simulation
8-bit Subtractor Implementation
Half Subtractor schematic
8-bit Subtractor Implementation
Half Subtractor layout
8-bit Subtractor Implementation
Half Subtractor digital simulation
8-bit Subtractor Implementation

Full Subtractor schematic
8-bit Subtractor Implementation
Full Subtractor layout
8-bit Subtractor Implementation
Full Subtractor digital simulation
8-bit Subtractor Implementation
8-bit Subtractor schematic
8-bit Subtractor Implementation
8-bit Subtractor schematic
8-bit Subtractor Implementation
8-bit Subtractor layout
8-bit Subtractor Implementation
8-bit Subtractor simulation
4-bit Multiplier Implementation schematic
4-bit Multiplier Implementation simulation
### Table 1: Estimation of Transistors

<table>
<thead>
<tr>
<th>Device</th>
<th>Number of device</th>
<th>Number of transistors per device</th>
<th>Total transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 bit Ripple Carry Adder</td>
<td>7</td>
<td>252</td>
<td>1764</td>
</tr>
<tr>
<td>8 bit Subtractor</td>
<td>4</td>
<td>252</td>
<td>1008</td>
</tr>
<tr>
<td>Multiplier</td>
<td>1</td>
<td>434</td>
<td>434</td>
</tr>
<tr>
<td>FIFO</td>
<td>17</td>
<td>172</td>
<td>2924</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
<td>6130</td>
</tr>
</tbody>
</table>
Area (mm$^2$)

$$3.8265 \times 4.832 = 18.4896$$

Power Consumption

$$P = 2CV^2f = 0.1 \times [6130 \times (12\lambda) \times (0.8\text{um}/2\lambda) \times (2f \text{F/um})] \times 5^2 \times 10^6$$
$$= 0.1471 \text{ mW/MHz}$$
Feature Estimation

FIFO\_latency=1.45833\text{ns}

Multiplier\_latency=4.06742\text{ns}

Adder\_latency=0.933838\text{ns}

So, total latency=1.45833+4.06742+0.933838
=6.459588\text{(ns)}

The Maximum frequency is
\[ f = \frac{1}{\text{total latency}} = \frac{1}{6.459588\text{ns}} = 155 \text{ (MHz)} \]

Then, \[ P = 0.1471\text{mW/MHz} \times 155 \text{ MHz} \]
= 22.801 mW
Feature Estimation

Fig 3 Top view of layout

- FIFO
- Sub
- Sum
- FIFO
- Sub
- Sum
- FIFO
- Sub
- Sum
- FIFO
- Sub
- Sum
- FIFO
- Sub
- Sum
- Multiplier
Next Plan

- Complete the Complex Multiplier
- Circuit connection
- Verify FFT function with selected samples
- Optimize the design
That’s all

Thank you