Modified
Booth
Encoding
Radix-4 8-bit
Multiplier

Final Project Report

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Abstract:

In this project, we are building up a Modified Booth Encoding Radix-4 8-bit Multiplier using 0.5um CMOS technology. Booth multiplication allows for smaller, faster multiplication circuits through encoding the signed numbers to 2’s complement, which is also a standard technique used in chip design, and provides significant improvements by reducing the number of partial product to half over “long multiplication” techniques. In this project, we demonstrate an extendable system diagram for 8-bit radix-4 MBE algorithm. Encoder, decoder and Carry Look Ahead Adder (CLA) are presented in this system.

System Diagram:

We applied three basic unit cells in this design: Encoder, Decoder, and 12-bit Adder. Each unit schematic is shown below:

For 8-bit Multiplicand, we have the following structure:
12-bit Adder

We use 3 4-bit CLA units to build up our 12-bit adder circuit. The diagram is shown below.

4-bit CLA Adder:
Performance Estimation:

Transistor number and Area estimation

<table>
<thead>
<tr>
<th>Type of Gate</th>
<th>Num of Transistor</th>
<th>Number needed</th>
<th>Transistor Est.</th>
<th>Area for Gate(um²)</th>
<th>Area Est.</th>
</tr>
</thead>
<tbody>
<tr>
<td>And2</td>
<td>6</td>
<td>134</td>
<td>804</td>
<td>595</td>
<td>79730</td>
</tr>
<tr>
<td>OR2</td>
<td>6</td>
<td>62</td>
<td>372</td>
<td>577.5</td>
<td>35805</td>
</tr>
<tr>
<td>NOR2</td>
<td>4</td>
<td>32</td>
<td>128</td>
<td>315</td>
<td>10080</td>
</tr>
<tr>
<td>XNOR2</td>
<td>8</td>
<td>32</td>
<td>256</td>
<td>1147.5</td>
<td>36720</td>
</tr>
<tr>
<td>XOR2</td>
<td>8</td>
<td>30</td>
<td>240</td>
<td>885</td>
<td>26550</td>
</tr>
<tr>
<td>OR3</td>
<td>8</td>
<td>18</td>
<td>144</td>
<td>612.5</td>
<td>11025</td>
</tr>
<tr>
<td>AND3</td>
<td>8</td>
<td>30</td>
<td>240</td>
<td>707.25</td>
<td>21217.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Transistor</td>
<td></td>
<td>2184</td>
<td></td>
<td></td>
<td>0.265 mm²</td>
</tr>
<tr>
<td>Total Area</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Time Delay:

From the system diagram, we can see the critical path is as below:

For the 12-bit adder, each adder will give a 10 gate delay time. Including the encoder, decoder and 3 adder, we have 38 gate delay.

Power Consumption:

\[ P_{\text{total}} = P_{\text{static}} + P_{\text{dynamic}} = 1.887 \, mW / MHz + 0.205 mW = 0.2092 mW \quad (f = 100 MHz) \]
Project Floor plane:

Floor Plane
Sub circuit Design

Encoder Block

The encoder block generates the selector signals for each 3 bits of multiplicand. This is the logic for the encoder block:

- $M_i = X_i$;
- $X = X_0 \oplus X_{-1}$;
- $X_2 = X_{1}X_{0}X_{-1} + X_{1}X_{0}X_{-1}$

Here the schematic and the layout of the encoder.

Decoder Block

The decoder block generates the partial product from the selector signals that they are generated in encoder block.

This is the logic for the 1bit decoder that generates 1 bit of the partial product:

$PP_{ij} = (Y_jX_{-1} + Y_{j+1}X_{2}) \oplus M_i$

Fig.1 shows the schematic and the layout of 1 bit decoder block.

We design the 9 bit decoder using 9 blocks of 1bit decoder that their selector signals are the same and 9 blocks of half adder is used to make the partial product in the 2’s complement form in the negative cases. Fig.2 and 3 shows the schematic and the layout of 9 bit decoder block.
Fig. 1 1bit decoder block schematic and layout

Fig. 3 9bit Decoder Block schematic

Fig. 3 9bit Decoder Block layout
12 Bit Adder circuit

Logic

We use three 4bit Carry Look Ahead (CLA) Adder to make up the 12bit adder.
The 4bit CLA contains 4 PFA units and one CLL unit, which will increase the computation time.

Block Diagram:

Schematic

4bit Look Ahead ADDER
12bit Look ahead ADDER
Layout

4bit Look Ahead ADDER layout

12bit Look ahead ADDER
Full System Design

Logic

Here we will show how the signed multiplier works, and how to extend the sign bit. We get the 9bit output from Decoder, which is the 2’s complement result of partial products. Here is the sign extension for 16 bit x 16 bit.

\[ E_i = M_i \oplus PP[8] \]

This sign bit extension is different from the book and reference value, we apply the highest partial product bit rather than the multiplicand bit. This difference may come from we take a different approach to add sign bit. The book and reference paper all take the same way to put sign bit add at adder part. We finish this target at the generation partial product. Our 9bit decoder schematic carefully shows how this works.
Here is the schematic and layout of the multiplier:

**Schematic**
Encoder circuit:

Decoder and bit shift, sign extension:

We have sign extension on each partial product before they go into a 12-bit adder.
Connection between adder blocks.

For each output of 12 bit adder, the highest 10 bits go to next adder, and the lowest 2 bit goes to output directly.
Multiplier Layout
Here is our DRC and LVS check results:
Test Simulations:

Digital Simulation Result:

In order to make sure about the multiplication procedure we wrote the verilog code for all the blocks and check our multiplier with digital simulation. The table shows our simulation result:

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>00000001</td>
<td>00000001</td>
<td>0000000000000001</td>
</tr>
<tr>
<td>00001111</td>
<td>00000010</td>
<td>0000000000011110</td>
</tr>
<tr>
<td>00001111</td>
<td>00001000</td>
<td>0000000001110001</td>
</tr>
<tr>
<td>10000001</td>
<td>00000100</td>
<td>1111111000000100</td>
</tr>
<tr>
<td>10110111</td>
<td>01011010</td>
<td>1110011001010110</td>
</tr>
</tbody>
</table>

Eldo Simulation Result:

12 bit CLA adder Eldo Simulation Result:
Reference

[5]: Vojin G. Oklobdziji. High-Speed VLSI Arithmetic Units: Adders and Multipliers
[4]: Hsin-Lei Lin, Robert C. Chang, Ming-Tsai Chan. Design of a Novel Radix-4 Booth Multiplier